

# Multilayer Silicon Nitride-based Coupler Integrated into a Silicon Photonics Platform with <1 dB Coupling Loss to a Standard SMF over O, S, C and L optical bands

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**Abstract:** We experimentally demonstrate <1 dB coupling loss over O,S,C and L optical bands for both polarizations between an integrated silicon photonics platform and butt-coupled standard single mode fiber.

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## 1. Introduction

Silicon photonics is increasingly gaining commercial acceptance in the opto-electronics industry. Silicon-On-Insulator (SOI) has been the platform of choice for implementing various optical functionalities in silicon due to its high refractive index contrast and hence high modal confinement. However, to address the increasing bandwidth demands within the datacenters with rate requirements of 100G,400G and beyond while meeting stringent demands on lower cost, high efficiency/low power consumption means a fundamental lingering challenge to Silicon Photonics needs to be addressed. The tiny mode sizes of silicon waveguides (<1  $\mu\text{m}^2$ ) make it difficult to couple to and from a standard single mode fiber (SMF) which has much larger mode sizes (~100  $\mu\text{m}^2$ ). We present a new coupling approach that is both highly efficient and has been implemented in a volume CMOS manufacturing process.

Previous approaches to achieve efficient coupling between a silicon waveguide and a SMF include i) surface gratings and ii) edge coupling with mode transformers such as inverse nanotapers (NTs). Surface gratings suffer from narrow bandwidth range of operation and polarization sensitivity, limiting their use in WDM applications [1]. Edge couplers of which the inverse NT is the most popular[2], function by expanding the size of the waveguide mode. However, this modal expansion is limited by substrate leakage, due to the proximity of the Si substrate to a typical 2  $\mu\text{m}$  BOX layer (buried oxide) of photonic SOI wafers.

To address this issue, we have proposed[3] and implemented a novel spot size convertor that uses multiple silicon nitride-based nanotapers in a 3-D arrangement, in the form of a “prong”. A similar approach was also presented by others [4], but not integrated into a silicon photonics platform and used high-NA fiber instead of standard SMF.

## 2. Device Design and Implementation

Silicon nitride ( $\text{Si}_3\text{N}_4$ ) with a refractive index of  $n \approx 2.0$  in the O-band, intermediate to that of silicon ( $n \approx 3.45$ ) and silicon dioxide  $\text{SiO}_2$  ( $n \approx 1.44$ ), and also being CMOS compatible, is an ideal material for passive optical device functionalities in a silicon photonic platform.

To address the problem of coupling light in and out of a silicon photonic chip, we used silicon nitride and developed the device architecture shown in Fig.1(a). The prong coupler device consists of 3-D arrangement of silicon nitride NTs in an oxide cladding medium. The structure is designed to support only the fundamental TE and TM modes. By appropriately selecting the end widths of the NTs and the separation between them, a very high modal overlap integral (in excess of 97%) between the prong edge modes, shown in Fig. 1(b), and SMF modes can be achieved. Also, by appropriately tailoring the widths of the individual NTs along the length of the device (500  $\mu\text{m}$  in our case), the waveguide mode which is confined by all four NTs at the end interfacing with the abutted SMF can be made to adiabatically transform into a mode which is confined only in the top nitride layer with very low loss, thereby allowing broadband and efficient coupling between the silicon photonic chip and a standard SMF. The structure was optimized and simulated using FDTD and modal analysis tools [5]. Performing 3-D FDTD simulations indicated a minimum coupling loss of 0.37 dB for TE and 0.34 dB for TM modes at  $\lambda = 1310$  nm.

To integrate the prong coupler device into a silicon photonics platform, we distributed the nitride layers between the multiple metal layers used for electrical routing. The location and the separation between the nitride layers, along with their thicknesses, were to some degree, constrained by the back-end-of-line (BEOL) processes of our commercial CMOS foundry partner. Fig. 1(c) shows the relative locations of the three nitride layers and a cross-sectional TEM image of the prong coupler. The first nitride layer ( $\text{SiN1}$ ) is ~200 nm thick, and deposited using PECVD as part of the front-end-of-line (FEOL) process and is low loss (~0.3 dB/cm at  $\lambda = 1310$  nm). It is separated by ~290 nm of oxide

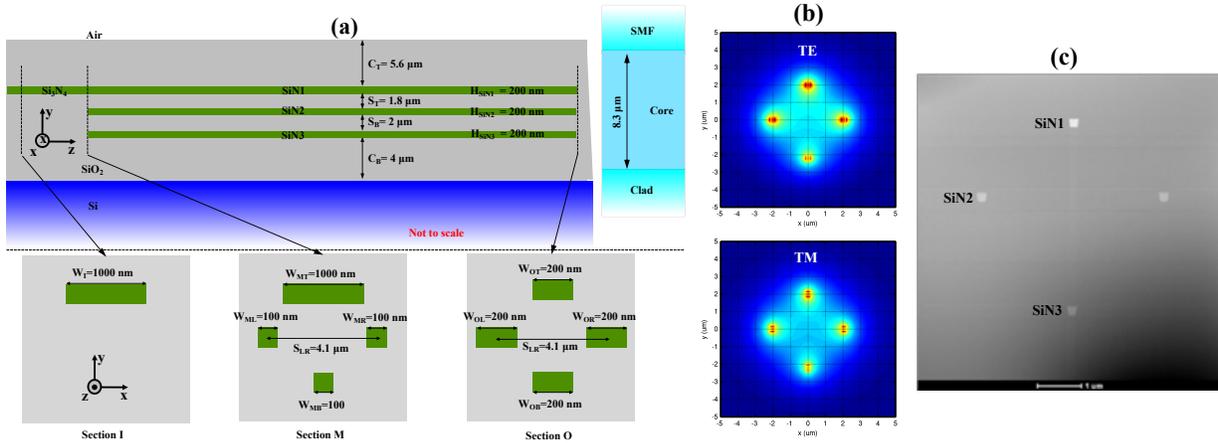


Fig. 1. (a) Targeted Prong coupler architecture with dimensions; (b) Fundamental TE and TM mode profiles corresponding to section O in (a) of the prong coupler; (c) The TEM cross section of our integrated prong coupler showing the relative location of the 3 nitride layers to section O

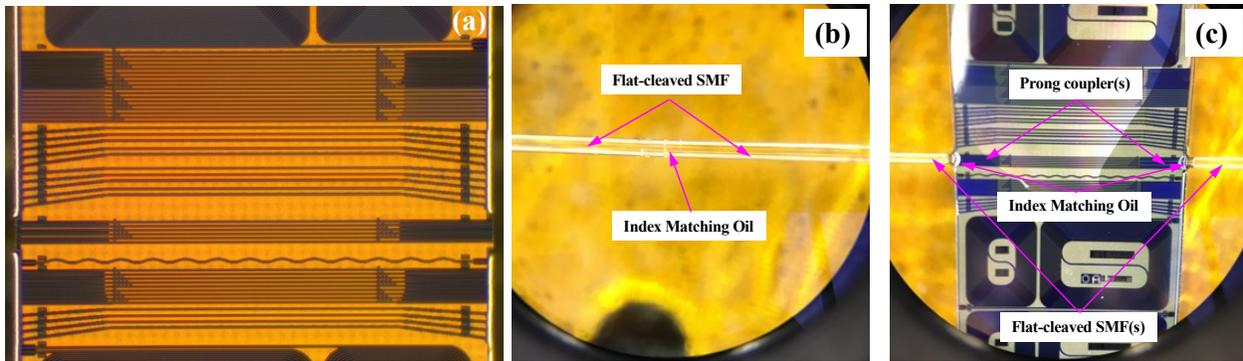


Fig. 2(a) Chip containing prong coupler test structures; (b) Flat cleaved SMFs alignment to characterize system losses; (c) Microscope view showing flat cleaved SMFs aligned to a Prong DUT

from the SOI crystalline Si film to allow highly efficient transmission of optical power between waveguides in the two layers using a vertical inverse taper adiabatic coupler [6] (not shown in Fig.1). The second (SiN2) and the third nitride (SiN3) layers, also each targeted at  $\sim 200\text{nm}$  thickness and deposited using PECVD, are interspersed with the metal layers M1 and M2 and are part of the BEOL process steps. Then, using a wafer bonding step, the whole structure is inverted and bonded to a silicon wafer with  $\sim 4\mu\text{m}$  of oxide using an oxide-oxide bonding process. The Si substrate of the primary active photonic wafer is removed followed by further BEOL processing. The stack up is so chosen as to allow efficient coupling between the prong coupler and a standard SMF for both TE and TM modes by also minimizing the substrate leakage losses.

### 3. Experimental Results

Fig. 2(a) shows a microscope picture of a portion of a fabricated die containing the prong coupler test structures. The test structure configuration was similar in all cases where a prong design variant is present on both ends of the die connected with a single mode waveguide in the SiN1 layer. Tunable lasers were used as the light source, together with a polarization controller to control the input polarization of the light launched into the input prong. Standard SMF flat cleaved fibers were used to couple light in and out of the prong couplers in the presence of refractive index matching oil (IMO) (Cargille Series AA,  $n \approx 1.45$ ) to suppress reflections. The configuration mimics the targeted design use with index matching epoxy. The SMF fibers in holders were mounted on piezo-controlled stages to precisely align the fibers to the prong couplers. The collected optical power by the output flat cleaved SMF fiber was read using an optical power meter. The system losses were characterized by peak aligning the fibers as shown in Fig. 2(b) in the presence of IMO, doing a wavelength sweep and reading the power collected as  $P_{\text{sys}}(\lambda)$ . It should be noted that this measurement was within 0.05dB of directly connecting the polarization controller output to the optical power meter. Next the fibers were peak aligned to the prong coupler device under test as shown in Fig. 2(c) and the optical power collected as  $P_{\text{DUT}}(\lambda)$ . The prong coupler to flat cleaved SMF coupling loss plus the prong coupler transmission loss is given by Eq.(1),

$$\alpha(\lambda) \text{ in dB} = 0.5 \cdot [P_{DUT}(\lambda) - P_{SYS}(\lambda) - \alpha_{WG}(\lambda) \cdot L_{WG}] \quad (1)$$

where  $\alpha_{WG}(\lambda)$  is SiN1 single mode waveguide loss in dB/cm and  $L_{WG}$  is the length in cm (0.2 cm for the chip shown in Fig.2(a)) of the SiN1 single mode waveguide interconnecting the two identical prongs on either end of the DUT.

Figure 3 shows the prong to flat cleaved SMF coupling loss as a function of wavelength (O, S, C and L bands) for TE and TM polarization mode launch conditions. The measurements consist of the same devices measured on 11 dies from 4 wafers. The wafers were processed in different lots in the CMOS fab and the measurements on different dies were also done time separated over the course of few weeks. Figures 3(a-c) show the coupling loss results for a particular prong device (structure A). Results indicate < 1 dB coupling loss over 230 nms of O,S,C and L bands for TE mode and over 100 nms of O band for TM. The same device over 130 nms of S, C and L bands in TM mode showed a loss of ~1.5 dB. However a slightly different prong device (structure B) which differs from structure A only in the profile of NT tapering in SiN1 layer showed a better coupling loss (<1 dB) to SMF in S,C,L bands for TM mode, results for which are shown in Figure 3(d). By appropriately selecting the right tapering parameters while accounting for the manufacturing bias, the authors believe it should be possible to achieve <0.5 dB coupling loss over entire O,S,C and L bands for both TE and TM polarizations using the same prong device.

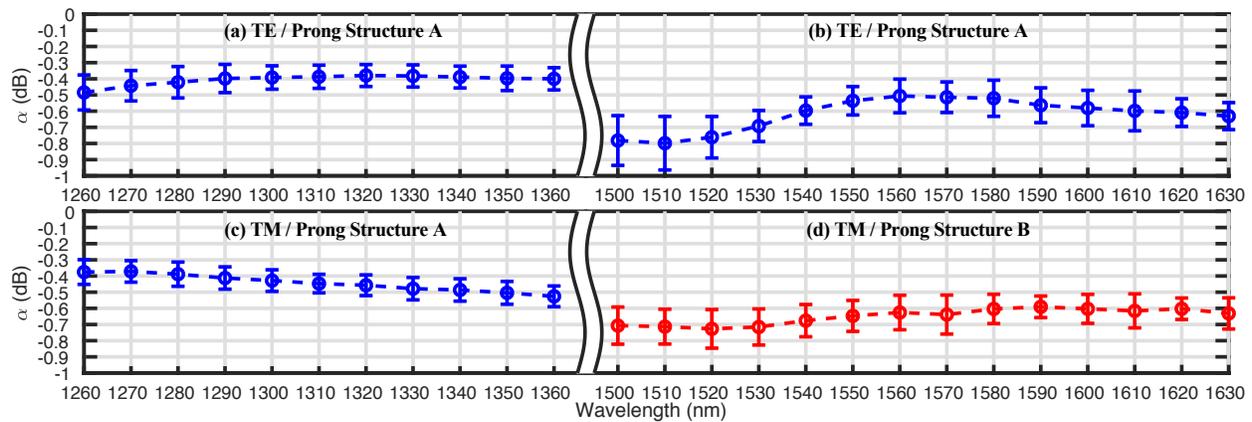


Fig. 3 Prong to Flat cleaved SMF coupling loss in the presence of index matching oil as a function of wavelength (O,S,C, and L bands) for TE and TM polarizations. SiN1 single mode waveguide losses were neglected in these plots.

#### 4. Conclusion

We have experimentally demonstrated coupling losses < 1dB between an integrated silicon photonics platform and a butt coupled flat cleaved standard single mode fiber over O,S,C and L bands. The approach uses a novel 3-D spot size converter in a prong configuration formed using multiple silicon nitride layers fully integrated into our silicon photonics platform. By virtue of its design and adiabatic operation, the prong coupler is fabrication tolerant, with very low wavelength and polarization dependence. It has best in class performance while simplifying the fiber coupling interface to the bare minimum of as-diced facet on the chip edge[7], hence it will further advance the field of silicon photonics by allowing standard semiconductor packaging for silicon photonic products.

#### 5. References

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