IEEE P802.3av™/D1.802, 6th June 2008
(Amendement of IEEE Std 802.3-2008)

IEEE P802.3™D1.802

Draft Standard for Information technology— Telecommunications and information exchange between systems— Local and metropolitan area networks— Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment: Physical Layer Specifications and Management Parameters for 10 Gb/s Passive Optical Networks

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is a amendement of IEEE Std 802.3-2008. provides physical layer specifications and management parameters for symmetric 10 Gb/s and asymmetric 10/1 Gb/s operation on point-to-multipoint passive optical networks. Draft D1.802 is prepared by the IEEE 802.3av 10 Gb/s PHY for EPON Task Force for Task Force Review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

Abstract: This amendment to IEEE Std 802.3–2008 provides INSERT YOUR PROJECT DESCRIPTION HERE.

Keywords: 802.3av, 10 Gb/s P2MP, PON, physical medium dependent, PMD

Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exceptions to IEEE style that is conciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecuively with arabic page numbers.

This introduction is not part of IEEE Std 802.3xx-200X, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: CSMA/CD Access Method and Physical Layer Specifications, Amendment: INSERT AMENDMENT NAME HERE

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE 802.3an-2006). A historical listing of all projects that have added to or modified IEEE Std 802.3 follows as a part of this introductory material. The listing is in chronological order of project initiation and for each project describes: subject, clauses added (if any), approval dates, and committee officers.

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in, and are superceded by, IEEE Std 802.3-200X and are not maintained as separate documents.

At the date of IEEE Std 802.3xx-200X publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-200X

Section One -- Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two -- Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s physical layer specifications..

Section Three -- Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s physical layer specifications.

.Section Four -- Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s physical layer specifications.

Section Five -- Includes Clause 56 through Clause 74 and Annex 57A through Annex 74A. Clause 56 through Clause 67 and associated annexes specify subscriber access physical layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s physical layer specification. Clause 69 through 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

IEEE Std 802.3at™–200X

> This amendment includes changes to IEEE Std 802.3–200X to augment the capabilities of the IEEE Std 802.3 standard with higher power levels and improved power management information.

IEEE Std 802.3av™–200X

> This amendment includes changes to IEEE Std 802.3–200X and adds Clauses 91 through 93 and Annex 91A. This amendment adds new Physical Layers for 10 Gb/s operation point-to-multipoint passive optical networks.

IEEE 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Participants

The following individuals were members of the IEEE 802.3 working group at the beginning of the P802.3xx working group ballot. Individuals may have not voted, voted for approval, disapproval, or abstained on this amendment.

David J. Law, *Working Group Chair*
Wael William Diab, *Working Group Vice Chair*

Adam Healey, *Working Group Secretary*
Steven B. Carlson, *Working Group Executive Secretary*
Bradley Booth, *Working Group Treasurer*

Glen Kramer, *Chair, 802.3av 10G-EPON PHY Task Force*
Duane Remein, *Chief Editor, 802.3av 10G-EPON PHY Task Force*
Marek Hajduczenia, *Assistant Editor, 802.3av 10G-EPON PHY Task Force*

xxx

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

xxx

xxx

When the IEEE–SA Standards Board approved this standard on 15 September 200X, it had the following membership:

xxx, *Chair*
xxx, *Vice Chair*
xxx, *Past Chair*
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xxx

*Member Emeritus

Also included are the following nonvoting IEEE–SA Standards Board liaisons:

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Michelle Turner
IEEE Standards Program Manager, Document Development

Michael D. Kipness
IEEE Standards Program Manager, Technical Program Development

List of special symbols

For the benefit of those who have received this document by electronic means, what follows is a list of special symbols and operators. If any of these symbols or operators fail to print out correctly on your machine, the editors apologize, and hope that this table will at least help you to sort out the meaning of the resulting funny-shaped blobs and strokes.

Special symbols and operators

Printed character	Meaning	Keystrokes	Character code	Font
∗	Boolean AND	*	ALT-042	Symbol
+	Boolean OR, arithmetic addition	+	ALT-043	Symbol
^	Boolean XOR	^	ALT-094	Times New Roman
!	Boolean NOT	!	ALT-033	Symbol
×	Multiplication	Ctrl-q 4	ALT-0180	Symbol
<	Less than	<	ALT-060	Symbol
≤	Less than or equal to	Ctrl-q #	ALT-0163	Symbol
>	Greater than	>	ALT-062	Symbol
≥	Greater than or equal to	Ctrl-q 3	ALT-0179	Symbol
=	Equal to	=	ALT-061	Symbol
≠	Not equal to	Ctrl-q 9	ALT-0185	Symbol
⇐	Assignment operator	Ctrl-q \	ALT-0220	Symbol
∈	Indicates membership	Ctrl-q Shift-n	ALT-0206	Symbol
∉	Indicates nonmembership	Ctrl-q Shift-o	ALT-0207	Symbol
±	Plus or minus (a tolerance)	Ctrl-q 1	ALT-0177	Symbol
°	Degrees	Ctrl-q 0	ALT-0176	Symbol
∑	Summation	Esc ^ Shift-a	ALT-0229	Symbol
√	Square root	Ctrl-q Shift-v	ALT-0214	Symbol
—	Big dash (em dash)	Ctrl-q Shift-q	ALT-0151	Times New Roman
–	Little dash (en dash), subtraction	Ctrl-q Shift-p	ALT-0150	Times New Roman
|	Vertical bar	|	ALT-0124	Times New Roman
†	Dagger	Ctrl-q Space	ALT-0134	Times New Roman
‡	Double dagger	Ctrl-q ‘	ALT-0135	Times New Roman
α	Lower case alpha	a	ALT-097	Symbol
β	Lower case beta	b	ALT-098	Symbol
γ	Lower case gamma	g	ALT-103	Symbol
δ	Lower case delta	d	ALT-100	Symbol
ε	Lower case epsilon	e	ALT-101	Symbol
λ	Lambda	l	ALT-0108	Symbol
μ	Micro	Ctrl-q 5	ALT-0181	Times New Roman
Ω	Omega	W	ALT-087	Symbol

Changes to ANSI/IEEE Std. IEEE 802.3ay, Clause 1

Editors' Note 1-1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

Editing instructions are shown in 8 point arial Bold red italic font. Four editing instructions are used: ***change***, ***delete***, ***insert***, *and* ***replace***.
Change *is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using strikethrough (to remove old material) or underscore (to add new material).*
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To simplify the addition of new tables, tables in this amendment clause are numbered based on their relationship to tables in the base document (IEEE P802.3ay D2.2). For example, Table 45-BB in this amendment would be renumbered Table-CC when the amendment is merged with IEEE P802.3ay D2.2. Continuing the example, a Table-AAb would then be renumbered Table-DD. All original table numbers in the base document can then be incremented after the merge.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

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Editors' Note 1-2 (to be removed prior to release): Draft revision history for Clause 1

Version	*Date*	*Comments*
D1.1	*Mar 2008*	*Draft for IEEE P802.3av Task Force review.*
D1.2	*Apr 2008*	*Draft for Task Force review with comment resolution from March 2008 meeting.*
D1.3	*May 2008*	*Draft for Task Force review with comment resolution from April 2008 meeting.*
D1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting.*

1. Introduction

1.1 Overview

1.2 Notation

1.3 Normative references

1.4 Definitions

Insert after 1.4.35 10GBASE-LX4, renumber as appropriate

10GBASE-PR:10GBASE-PR: IEEE 802.3 Physical Layer specification for a 10 Gb/s symmetric point-to-multipoint link over one single-mode optical fiber (See IEEE 802.3 Clause 91, Clause 92 and Clause 93).

Insert after 1.4.41 10GBASE-X, renumber as appropriate

10/1GBASE-PRX:10/1GBASE-PRX:IEEE 802.3 Physical Layer specification for a 10 Gb/s downstream, 1 Gb/s upstream asymmetric point-to-multipoint link over one single-mode optical fiber (see IEEE 802.3 Clause 91, Clause 92, Clause 93).

Change subclause 1.4.95 as follows:

1.4.95 channel insertion loss: As used in IEEE 802.3 Clause 38, Clause 52, Clause 53, Clause 58, Clause 59, Clause 60, Clause 68 and Clause 91 for fiber optic links, the static loss of light through a link between a transmitter and receiver. It includes the loss of the fiber, connectors, ~~and~~ splices and optional power splitter/combiner (for details, see subclause @@91.8.1@@)

1.5 Abbreviations

Insert a new abbrevation to the list, sort the list alphabetically:

SCB Single Copy Broadcast

Changes to ANSI/IEEE Std. IEEE 802.3ay, Clause 30

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

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External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 30

Version	Date	Comments
D1.1	Jan 2008	Draft for IEEE P802.3av Task Force review.
D1.2	Apr 2008	Draft for Task Force review with comment resolution from March 2008 meeting.
D1.3	May 2008	Draft for Task Force review with comment resolution from April 2008 meeting.
D1.8023	Jun 2008	Draft for Task Force review with comment resolution from May 2008 meeting.

30. Management

30.1 Overview

30.2 Managed objects

30.3 Layer management for DTEs

30.3.2.1.2 aPhyType

Add:
10/1GBASE-PR Clause 92 symmetric 10 Gb/s 64B/66B
10/1GBASE-PRX Subclause 92.2.1.1 asymmetric 10 Gb/s 64B/66B with 1 Gb/s 8B/10B

30.3.2.1.3 aPhyTypeList

Add:
10/1GBASE-PR Clause 92 symmetric 10 Gb/s 64B/66B
10/1GBASE-PRX Subclause 92.2.1.1 asymmetric 10 Gb/s 64B/66B with 1 Gb/s 8B/10B

30.4 Layer management for 10, 100, and 1000 Mb/s baseband repeaters

30.5 Layer management for 10 Mb/s, 100 Mb/s, 1000 Mb/s and 10 Gb/s medium attachment units (MAUs)

30.5.1.1.2 aMAUType

Change below:

10GBASE-SW	W fiber over 850nm optics as specified in Clause 52
802.9a	Integrated services MAU as specified in IEEE Std 802.9™ ISLAN-16T
10/1GBASE–PRX–D1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 91
10/1GBASE–PRX–D2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 91
10/1GBASE–PRX–D3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 91
10/1GBASE–PRX–U1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 91
10/1GBASE–PRX–U2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 91
10/1GBASE–PRX–U3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 91
10GBASE–PR–D1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 91
10GBASE–PR–D2	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 91
10GBASE–PR–D3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 91
10GBASE–PR–U1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 91

10GBASE–PR–U3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 91

30.5.1.1.15 aFECCorrectedBlocks

Change:

For 1000BASE-PX, ~~or~~ 10GBASE-R, 10GBASE–PR, or 10GBASE–PRX-U PHYs, a count of corrected FEC blocks. This counter will not increment for other PHY types.

30.5.1.1.16 aFECUncorrectableBlocks

Change:

For 1000BASE-PX, ~~or~~ 10GBASE-R PHYs, 10GBASE–PR, or 10GBASE–PRX-U PHYs, a count of uncorrectable FEC blocks. This counter will not increment for other PHY types.

30.6 Management for Link Auto-Negotiation

30.7 Management for Link Aggregation

30.8 Management for WAN Interface Sublayer (WIS)

30.9 Management for Power Sourcing Equipment (PSE)

30.10 Layer management for Midspan

30.11 Layer Management for Physical Medium Entity (PME)

Changes to ANSI/IEEE Std. IEEE 802.3ay, Clause 45

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

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Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 45

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D1.1	*Jan 2008*	*Draft for IEEE P802.3av Task Force review.*
D1.2	*Apr 2008*	*Draft for Task Force review with comment resolution from March 2008 meeting.*
D1.3	*May 2008*	*Draft for Task Force review with comment resolution from April 2008 meeting.*
D1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting.*

45. Management Data Input/Output (MDIO) Interface

45.1 Overview

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Modify row in Table 45-3 for register addresses 1.12 and 1.13 as presented below:

Table 45–3—PMA/PMD speed ability register bit definitions

Register address	Register name
1.12	P2MP ability register
1.13	Reserved

45.2.1.1.4 PMA loopback (1.0.0)

Change first sentence in second paragraph

The loopback function is mandatory for the 1000BASE-KX, 10GBASE-KR, and 10GBASE-X port type and optional for all other port types, except 2BASE-TL, 10PASS-TS, and 10/1GBASE-PRX, which do not support loopback.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change Table 45-6 as shown below

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15:~~7~~8	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.7	10/1G capable	1 = PMA/PMD is capable of operating at 10 Gb/s downstream and 1Gb/s upstream 0 = PMA/PMD is not capable of operating at 10 Gb/s downstream and 1Gb/s upstream.	RO
1.4.6	10M capable	1 = PMA/PMD is capable of operating at 10 Mb/s 0 = PMA/PMD is not capable of operating as 10 Mb/s	RO

[a]RO = Read only

Insert new subclause 45.2.1.4.1 as below renumbering remaining subclauses:

45.2.1.4.1 10/1G capable (1.4.7)

When read as a one, bit 1.4.7 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s in the downstream direction and 1Gb/s in the upstream direction. When read as a zero, bit 1.4.7 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s in the downstream direction and 1Gb/s in the upstream direction.

Change Table 45-7 as shown below

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Insert prior to 45.2.1.10.1, renumber remaining subclauses in 45.2.1.10 as appropriate:

45.2.1.10.1 P2MP ability (1.11.9)

When read as a one, bit 1.1.9 indicates that the PMA/PMD has P2MP abilities listed in register 1.12. When read as a zero, bit 1.11.9 indicates that the PMA/PMD does not have P2MP abilities.

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:~~4~~3	Reserved	Value always 0, writes ignored	R/W
1.7.~~3~~4:0	PMA/PMD type selection	4 3 2 1 0 1 1 0 1 0 = 10GBASE-PR-U3 1 1 0 0 1 = 10GBASE-PR-U1 1 1 0 0 0 = 10/1GBASE-PRX-U3 1 0 1 1 1 = 10/1GBASE-PRX-U2 1 0 1 1 0 = 10/1GBASE-PRX-U1 1 0 1 0 1 = 10GBASE-PR-D3 1 0 1 0 0 = 10GBASE-PR-D2 1 0 0 1 1 = 10GBASE-PR-D1 1 0 0 1 0 = 10/1GBASE-PRX-D3 1 0 0 0 1 = 10/1GBASE-PRX-D2 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 1 1 1 1 = 10BASE-T PMA/PMD type 0 1 1 1 0 = 100BASE-TX PMA/PMD type 0 1 1 0 1 = 1000BASE-KX PMA/PMD type 0 1 1 0 0 = 1000BASE-T PMA/PMD type 0 1 0 1 1 = 10GBASE-KR PMA/PMD type 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD type 0 1 0 0 1 = 10GBASE-T PMA type 0 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

[a]R/W = Read/Write

Change first three rows of Table 45-11 as follows.

Table 45–11—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15:10 ~~9~~	Reserved	Ignore on read	RO
1.11.9	P2MP ability	1 = PMA/PMD has P2MP abilities listed in register 1.12 0 = PMA/PMD does not have P2MP abilities	RO
1.11.8	10BASE-T ability	1 = PMA/PMD is able to perform 10BASE-T 0 = PMA/PMD is not able to perform 10BASE-T	RO

[a]RO = Read only

Insert Subclause 45.2.1.11 and Table 45-12 as shown below, renumber succeding paragraphs and tables.

45.2.1.11 P2MP PMA/PMD ability register (Register 1.12)

The assignment of bits in the P2MP PMA/PMD ability register is shown in Table 45-12. All of the bits in the P2MP PMA/PMD ability register are read only; a write to the P2MP PMA/PMD ability register shall have no effect..

Table 45–12—P2MP PMA/PMD Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.12.15:11	Reserved	Ignore on read	RO
1.12.10	10/1GBASE-PRX-D1 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D1 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D1	RO

Table 45–12—P2MP PMA/PMD Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.12.9	10/1GBASE-PRX-D2 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D2 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D2	RO
1.12.8	10/1GBASE-PRX-D3 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D3 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D3	RO
1.12.7	10GBASE-PR-D1 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D1 0 = PMA/PMD is not able to perform 10GBASE-PR-D1	RO
1.12.6	10GBASE-PR-D2 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D2 0 = PMA/PMD is not able to perform 10GBASE-PR-D2	RO
1.12.5	10GBASE-PR-D3 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D3 0 = PMA/PMD is not able to perform 10GBASE-PR-D3	RO
1.12.4	10/1GBASE-PRX-U1 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U1 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U1	RO
1.12.3	10/1GBASE-PRX-U2 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U2 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U2	RO
1.12.2	10/1GBASE-PRX-U3 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U3 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U3	RO
1.12.1	10GBASE-PR-U1 ability	1 = PMA/PMD is able to perform 10GBASE-PR-U1 0 = PMA/PMD is not able to perform 10GBASE-PR-U1	RO
1.12.0	10GBASE-PR-U3 ability	1 = PMA/PMD is able to perform 10GBASE-PR-U3 0 = PMA/PMD is not able to perform 10GBASE-PR-U3	RO

[a]RO = Read only

45.2.1.11.1 10/1GBASE-PRX-D1 ability (1.12.10)

When read as a one, bit 1.12.10 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D1 PMA/PMD type. When read as a one, bit 1.12.10 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D1 PMA/PMD type.

45.2.1.11.2 10/1GBASE-PRX-D2 ability (1.12.9)

When read as a one, bit 1.12.9 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D2 PMA/PMD type. When read as a one, bit 1.12.9 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D2 PMA/PMD type.

45.2.1.11.3 10/1GBASE-PRX-D3 ability (1.12.8)

When read as a one, bit 1.12.8 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D3 PMA/PMD type. When read as a one, bit 1.12.8 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D3 PMA/PMD type.

45.2.1.11.4 10GBASE-PR-D1 ability (1.12.7)

When read as a one, bit 1.12.7 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D1 PMA/PMD type. When read as a one, bit 1.12.7 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D1 PMA/PMD type.

45.2.1.11.5 10GBASE-PR-D2 ability (1.12.6)

When read as a one, bit 1.12.6 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D2 PMA/PMD type. When read as a one, bit 1.12.6 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D2 PMA/PMD type.

45.2.1.11.6 10GBASE-PR-D3 ability (1.12.5)

When read as a one, bit 1.12.5 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D3 PMA/PMD type. When read as a one, bit 1.12.5 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D PMA/PMD type.

45.2.1.11.7 10/1GBASE-PRX-U1 ability (1.12.4)

When read as a one, bit 1.12.4 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U1 PMA/PMD type. When read as a one, bit 1.12.4 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U1 PMA/PMD type.

45.2.1.11.8 10/1GBASE-PRX-U2 ability (1.12.3)

When read as a one, bit 1.12.3 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U2 PMA/PMD type. When read as a one, bit 1.12.3 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U2 PMA/PMD type.

45.2.1.11.9 10/1GBASE-PRX-U3 ability (1.12.2)

When read as a one, bit 1.12.2 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U3 PMA/PMD type. When read as a one, bit 1.12.2 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U3 PMA/PMD type.

45.2.1.11.10 10GBASE-PR-U1 ability (1.12.1)

When read as a one, bit 1.12.1 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-U1 PMA/PMD type. When read as a one, bit 1.12.1 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-U1 PMA/PMD type.

45.2.1.11.11 10GBASE-PR-U3 ability (1.12.0)

When read as a one, bit 1.12.0 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-U3 PMA/PMD type. When read as a one, bit 1.12.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-U3 PMA/PMD type.

Insert Subclauses 45.2.1.88 through 45.2.1.91 with respective tables, as presented below. Renumber succeeding tables as appropriate.

45.2.1.88 10GBASE-PR FEC ability register (Register 1.176)

The assignment of bits in the 10GBASE-PR FEC ability register is shown in Table 45–65.

Table 45–65—10GBASE-PR FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.176.15:2	Reserved	Value always zero, writes ignored	RO
1.176.1	10GBASE-PR FEC error indication ability	A read of 1 in this bit indicates that the 10GBASE-PR PHY is able to report FEC decoding errors to the PCS layer	RO
1.176.0	10GBASE-PR FEC ability	A read of 1 in this bit indicates that the 10GBASE-PR PHY supports FEC	RO

[a]RO Read only

45.2.1.88.1 10GBASE-PR FEC ability (1.176.0)

When read as a one, this bit indicates that the 10GBASE-PR PHY supports forward error correction (FEC). When read as a zero, the 10GBASE-PR PHY does not support forward error correction.

45.2.1.88.2 10GBASE-PR FEC error indication ability (1.176.1)

When read as a one, this bit indicates that the 10GBASE-PR FEC is able to indicate decoding errors to the PCS layer (see @@Subclause 92.??.??@@). When read as a zero, the 10GBASE-PR FEC is not able to indicate decoding errors to the PCS layer. 10GBASE-PR FEC error indication is controlled by the FEC enable error indication bit in the FEC control register (see @@Subclause 45.2.1.85.2@@).

45.2.1.89 10GBASE-PR FEC control register (Register 1.177)

The assignment of bits in the 10GBASE-PR FEC control register is shown in Table 45–66.

Table 45–66—10GBASE-PR FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.177.15:2	Reserved	Value always zero, writes ignored	RO
1.177.1	FEC enable error indication	A write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer	R/W
1.177.0	FEC enable	A write of 1 to this bit enables 10GBASE-PR FEC A write of 0 to this bit disables 10GBASE-PR FEC	R/W

[a]R/W = Read/Write, RO Read only

45.2.1.89.1 FEC enable (1.177.0)

When written as a one, this bit enables FEC for the 10GBASE-R PHY. When written as a zero, FEC is disabled in the 10GBASE-R PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.89.2 FEC enable error indication (1.177.1)

This bit enables the 10GBASE-PR FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-PR PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero the error indication function is disabled. Writes to this bit are ignored and reads return a zero if the 10GBASE-PR FEC does not have the ability to indicate decoding errors to the PCS layer (see @@Subclause 45.2.1.84.2@@ and @@Subclause 74.8.3@@).

45.2.1.90 10GBASE-PR FEC corrected blocks counter (Register 1.178, 1.179)

The assignment of bits in the 10GBASE-PR FEC corrected blocks counter register is shown in Table 45–67. See @@Subclause 74.8.4.1@@ for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.178, 1.179 are used to read the value of a 32-bit counter. When registers 1.178 and 1.179 are used to read the 32-bit counter value, the register 1.178 is read first, the value of the register 1.179 is latched when (and only when) register 1.178 is read and reads of register 1.179 returns the latched value rather than the current value of the counter.

Table 45–67—10GBASE-PR FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.178.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.179.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.91 10GBASE-PR FEC uncorrected blocks counter (Register 1.180, 1.181)

The assignment of bits in the 10GBASE-R FEC uncorrected blocks counter register is shown in Table 45–68. See @@Subclause 74.8.4.2@@ for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.180, 1.181 are used to read the value of a 32-bit counter. When registers 1.180 and 1.181 are used to read the 32-bit counter value, the register 1.180 is read first, the value of the register 1.181 is latched when (and only when) register 1.180 is read and reads of register 1.181 returns the latched value rather than the current value of the counter.

Table 45–68—10GBASE-PR FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.180.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.181.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3 PCS registers

Change last rows of Table 45-82:

Register address	Register name
3.74	10GBASE-PR and 10/1GBASE-PRX clause 92 BER Monitor Control
~~3.74~~ 3.75 thgough 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

Change row 8 (not including header) of Table 45-83 as follows:

3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 ~~x~~1 = Reserved 0 0 1 0 = 10/1Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

Insert after subclause 45.2.3.28 10P/2B PAF lost ends of fragments register (Register 3.73):

45.2.3.29 10GBASE-PR and 10/1GBASE-PRX Clause 92 BER Monitor Control register (Register 3.74)

The assignment of bits in the 10GBASE-R and 10/1GBASE-PRX BER Monitor Control Register is shown in Table 45–77. This register is only required when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported. The 10G-EPON BER Monitor is described in @@Subclause 92.2.4.1.1.1@@.

Table 45–77—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.74.0:7	10G-EPON BER Monitor Timer	Duration (in units of 5 microseconds) of the timer used by the 10G-EPON BER Monitor function Default value is 25 (ie. 125 microseconds). A value of 0 indicates that the BER monitor function is disabled	R/W
3.74.8:15	10G-EPON BER Monitor Threshold	Number of Sync Header errors within a timer interval that triggers a high BER condition for the 10G-EPON BER Monitor function. Default value is 16. A value of 0 indicates that the BER monitor function is disabled.	R/W

[a]R/W = Read/Write

45.3 Management frame structure

45.4 Electrical interface

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface

Changes to ANSI/IEEE Std. IEEE 802.3ay, Clause 56

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

Editing instructions are shown in 8 point arial Bold red italic font. Four editing instructions are used: ***change***, ***delete***, ***insert***, *and* ***replace***.
Change *is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using strikethrough (to remove old material) or underscore (to add new material).*
Delete *removes existing material.*
Insert *adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction.*
Replace *is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions*
To simplify the addition of new tables, tables in this amendment clause are numbered based on their relationship to tables in the base document (IEEE P802.3ay D2.2). For example, Table 45-BB in this amendment would be renumbered Table-CC when the amendment is merged with IEEE P802.3ay D2.2. Continuing the example, a Table-AAb would then be renumbered Table-DD. All original table numbers in the base document can then be incremented after the merge.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

:

Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 56

Version	Date	Comments
D1.2	Apr 2008	Draft for IEEE P802.3av Task Force review.
D1.3	May 2008	Draft for Task Force review with comment resolution from April 2008 meeting.
D1.8023	Jun 2008	Draft for Task Force review with comment resolution from May 2008 meeting.

56. Introduction to Ethernet for subscriber access networks

56.1 Overview

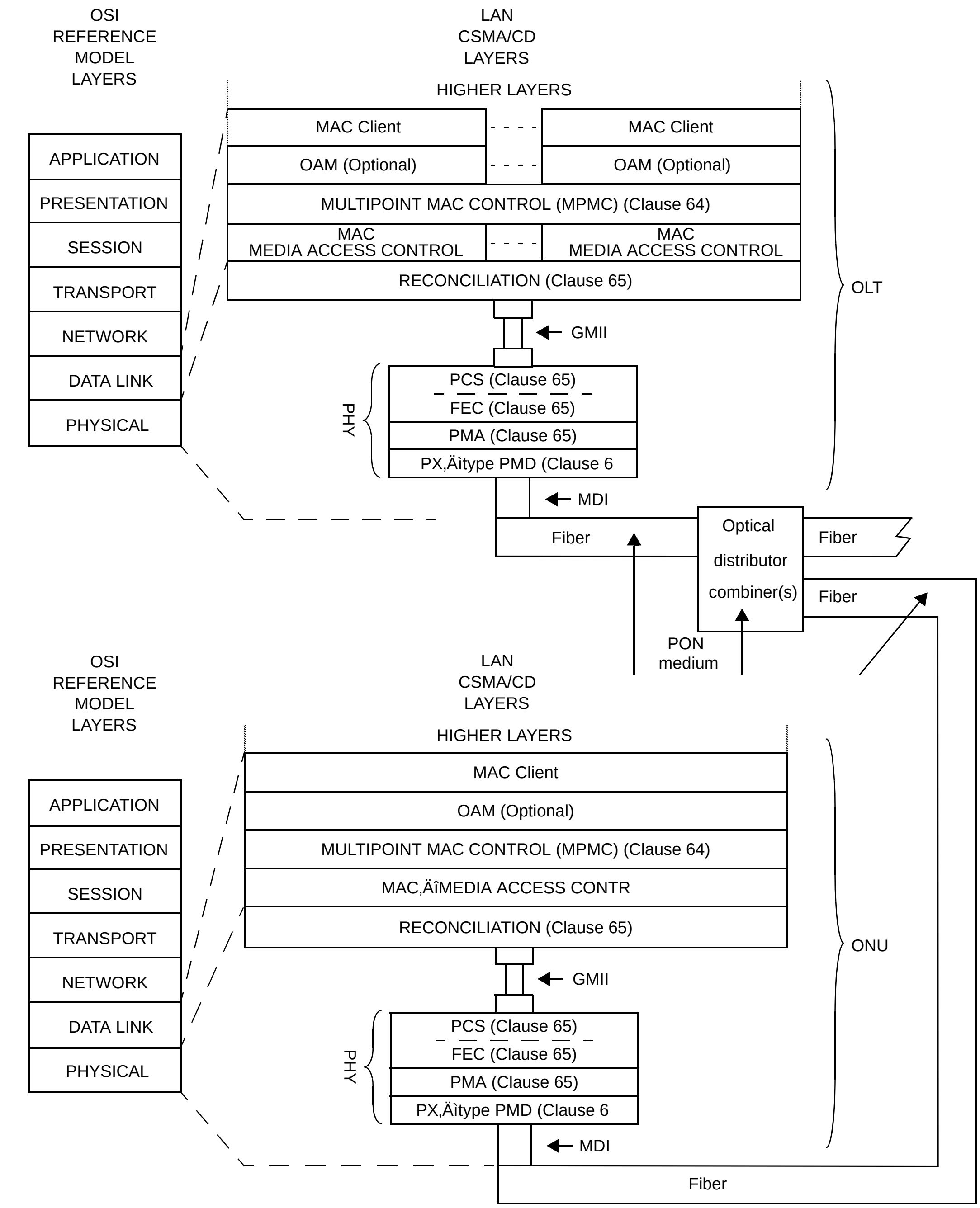
Change first paragraphs shown below:

Ethernet for subscriber access networks, also referred to as “Ethernet in the First Mile”, or EFM, combines a minimal set of extensions to the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers. These Physical Layers include optical fiber and voice grade copper cable Physical Medium Dependent sublayers (PMDs) for point-to-point (P2P) connections in subscriber access networks. EFM also introduces the concept of Ethernet Passive Optical Networks (EPONs), in which a point-to-multipoint (P2MP) network topology is implemented with passive optical splitters, along with extensions to the MAC Control sublayer and Reconciliation sublayer as well as optical fiber PMDs to support this topology. In addition, a mechanism for network Operations, Administration, and Maintenance (OAM) is included to facilitate network operation and troubleshooting. 100BASE-LX10 extends the reach of 100BASE-X to achieve 10 km over conventional single-mode two-fiber cabling. The relationships between these EFM elements and the ISO/IEC Open System Interconnection (OSI) reference model are shown in Figure 56–1 for point-to-point topologies, ~~and~~ Figure 56–2 for symmetric 1Gb/s EPON ~~point-to-multipoint~~ topologies, Figure 56-3 for symmetric 10G-EPON topologies and Figiure 56-4 for asymmetric 10G-EPON topologies.

An important characteristic of EFM is that only full duplex links are supported. A simplified full duplex MAC is defined in Annex 4A for use in EFM networks. P2MP applications must use this simplified full duplex MAC. EFM Copper applications may use either this simplified full duplex MAC or the Clause 4 MAC operating in half duplex mode as described in 61.1.4.1.2. All other EFM P2P applications may use either this simplified full duplex MAC or the Clause 4 MAC operating in full duplex mode.

EFM architecture is extended in Clause 91 and Clause 92 by the addition of 10G–EPON. 10G–EPON includes the symmetric (10 Gb/s downstream and 10 Gb/s upstream) as well as asymmetric (10 Gb/s downstream and 1 Gb/s upstream) PONs. In the following clauses, the symmetric 1 Gb/s EPON is referred to as EPON, while symmetric 10 Gb/s and asymmetric EPONs are referred to as 10G–EPON.

Replace Figure 56-2 with that shown below:

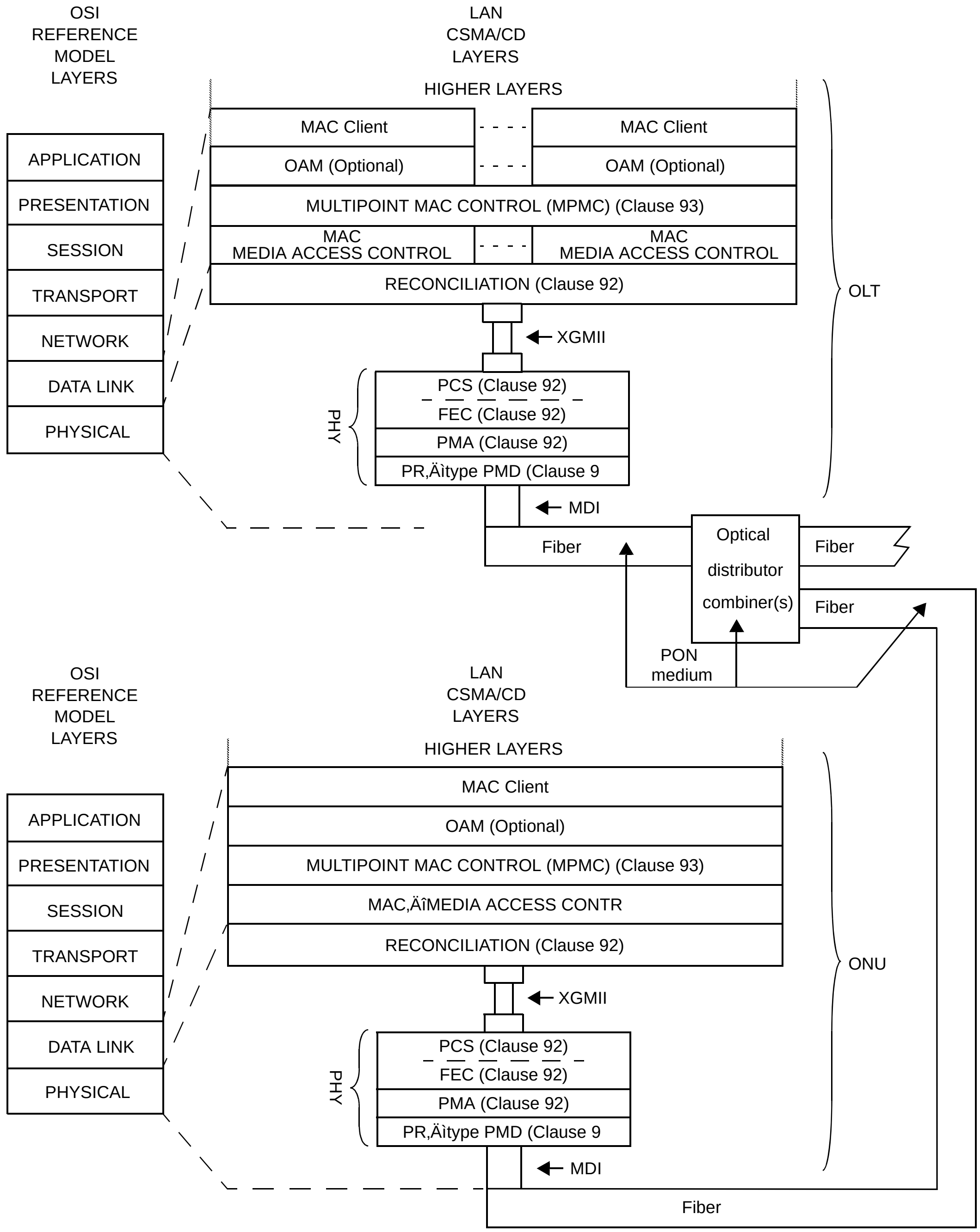


GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 56–2—Architectural positioning of EFM:
P2MP symmetric 1 Gb/s EPON architecture (1 Gb/s downstream, 1 Gb/s upstream)**

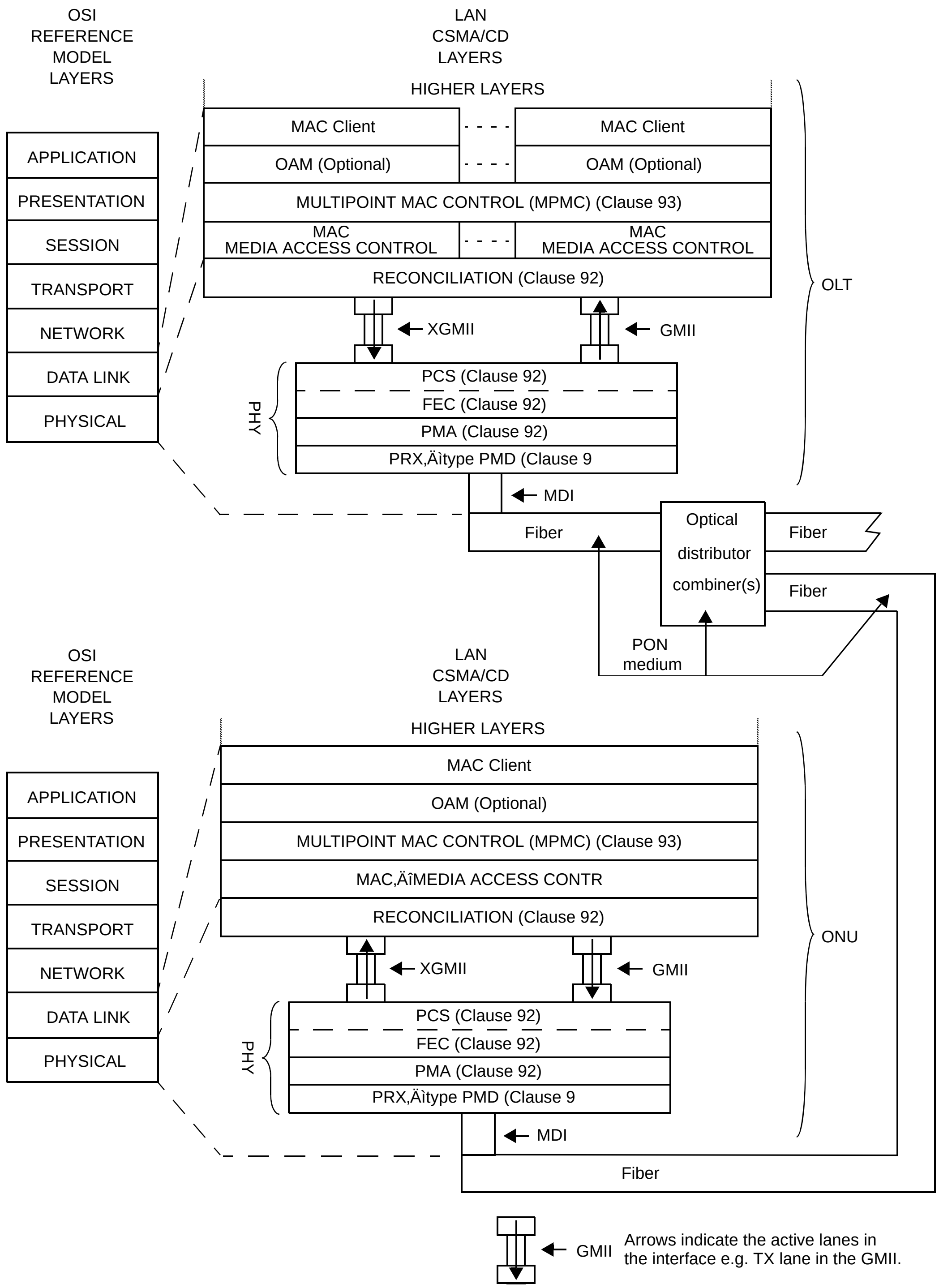
Insert Figure 56-3 and 56-4, renumbering subsequent figures as appropriate.



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–3—Architectural positioning of EFM:
P2MP symmetric 10G–EPON architecture (10 Gb/s downstream, 10 Gb/s upstream)



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–4—Architectural positioning of EFM:
P2MP asymmetric 10G–EPON architecture (10 Gb/s downstream, 1 Gb/s upstream)

Change Subclause 56.1.2 as shown below:

56.1.2 Summary of P2MP sublayers

~~For P2MP optical fiber topologies, EFM supports a nominal bit rate of 1000 Mb/s, shared amongst the population of Optical Network Units (ONUs) attached to the P2MP topology. The P2MP PHYs use the 1000BASE-X Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA) sublayer defined in Clause 65, and an optional FEC function defined in Clause 65.~~

For P2MP optical fiber topologies, EFM supports two systems:

a) PON with a symmetric, EFM supports a nominal bit rate of 1000 Mb1 Gb/s, shared amongst the population of Optical Network Units (ONUs) attached to the P2MP topology. The P2MP PHYs use the 1000BASE-–X Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA) sublayer defined in Clause 65@@Clause 60@@, and an optional FEC Forward Error Correction (FEC) function defined in Clause 65.Clause 65;

b) PON with a nominal bit rate of 10 Gb/s in downstream and 10 Gb/s upstream (symmetric, 10G–EPON) as well as PON with a nominal bit rate of 10 Gb/s in downstream and 1 Gb/s upstream (asymmetric, 10G–EPON), shared amongst the population of ONUs attached to the P2MP topology. The P2MP PHYs use the 10GBASE–R PCS, the PMA sublayer defined in @@Clause 91@@, and an mandatory FEC function defined in @@Clause 92@@.

56.1.2.1 Multipoint MAC Control Protocol (MPCP)

The Multipoint MAC Control Protocol (MPCP) for 1 Gb/s EPON uses messages, state diagrams ~~machines~~, and timers, as defined in Clause 64, to control access to a P2MP topology, while Clause 93 defines the messages, state diagrams, and timers required to control access to a P2MP topology in 10G-EPON (10 Gb/s EPON). The issues related with coexistence of EPON and 10G-EPON on the same fiber plant are described in @@Subclause 93.4@@.

Every P2MP topology consists of one Optical Line Terminal (OLT) plus one or more ONUs, as shown in Figure 56–2. One of several instances of the MPCP in the OLT communicates with the instance of the MPCP in the ONU. A pair of MPCPs that communicate between the OLT and ONU are a distinct and associated pair.

56.1.2.2 Reconciliation Sublayer (RS) and media independent interfaces

The Clause 22 RS and MII, ~~and~~ Clause 35 RS and GMII, and Clause 46 RS and XGMII, are ~~both~~ all employed for the same purpose in EFM, that being the interconnection between the MAC sublayer and the PHY sublayers. Extensions to the Clause 35 RS for P2MP topologies are described in Clause 65, while extensions to the Clause 46 RS for P2MP topologies are described in Clause 92.

The combination of MPCP and the extension of the Reconciliation Sublayer (RS) RS for P2P Emulation allows an underlying P2MP network to appear as a collection of point-to-point links to the higher protocol layers (at and above the MAC Client). It achieves this by prepending a Logical Link Identification (LLID) to the beginning of each ~~packet~~ data frame, replacing two octets of the preamble. This is described in Clause 65 for EPON and in Clause 92 for 10G–EPON. EFM Copper links use the MII of Clause 22 operating at 100 Mb/s. This is described in @Subclause 61.1.4.1.2@@.

56.1.3 Physical Layer signaling systems

Insert below third paragraph in subclause:

Additionally, EFM introduces a family of Physical Layer signaling systems which are derived from 10GBASE–R, but which include extensions to the RS, PCS and PMA, along with a mandatory FEC capability, as defined in @@Clause 92@@. The family of P2MP Physical Layer signaling systems includes the following series of PMD combinations:

c) 10GBASE–PR–D1 and 10GBASE–PR–U1, creating a PR10 power budget, with symmetric 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting the reach of at least 10 km and the split ratio of at least 1:16;
d) 10GBASE–PR–D2 and 10GBASE–PR–U1, creating a PR20 power budget, with symmetric 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting the reach of at least 20 km and the split ratio of at least 1:16 or the reach of at least 10 km and the split ratio of at least 1:32;
e) 10GBASE–PR–D3 and 10GBASE–PR–U3, creating a PR10 power budget, with symmetric 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting the reach of at least 20 km and the split ratio of at least 1:32;
f) 10/1GBASE–PRX–D1 and 10/1GBASE–PR–U1, creating a PRX10 power budget, with asymmetric 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting the reach of at least 10 km and the split ratio of at least 1:16;
g) 10/1GBASE–PRX–D2 and 10/1GBASE–PRX–U1, creating a PRX20 power budget, with asymmetric 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting the reach of at least 20 km and the split ratio of at least 1:16;
h) 10/1GBASE–PRX–D3 and 10/1GBASE–PRX–U3, creating a PRX10 power budget, with asymmetric 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting the reach of at least 20 km and the split ratio of at least 1:32;

All 10G–EPON PMDs are defined in @@Clause 91@@.

Change Table 56-1 as below

Name	Location	Rate ~~(Mb/s)~~	Nominal reach (km)	Medium	Clause
100BASE-LX10	ONU/ OLT[a]	100 Mb/s	10	Two single-mode fibers	@@58 @@
100BASE-BX10-D	OLT	100 Mb/s	10	One single-mode fiber	@@58 @@
100BASE-BX10-U	ONU				
1000BASE-LX10	ONU/ OLT[a]	1000 Mb/s	10 0.55	Two single-mode fibers Two multimode fibers	@@59 @@
1000BASE-BX10-D	OLT	1000 Mb/s	10	One single-mode fiber	@@59 @@
1000BASE-BX10-U	ONU				
1000BASE-PX10-D	OLT	1000 Mb/s	10	One single-mode fiber PON	@@60 @@
1000BASE-PX10-U	ONU				
1000BASE-PX20-D	OLT	1000 Mb/s	20	One single-mode fiber PON	@@60 @@
1000BASE-PX20-U	ONU				
10/1GBASE-PRX-D1	OLT	1000 Mb/s	10	One single-mode fiber PON	91
10/1GBASE-PRX-U1	ONU	10 Gb/s			
10/1GBASE-PRX-D2	OLT	1000 Mb/s	20	One single-mode fiber PON	91
10/1GBASE-PRX-U2	ONU	10 Gb/s			
10/1GBASE-PRX-D3	OLT	1000 Mb/s	20	One single-mode fiber PON	91
10/1GBASE-PRX-U4	ONU	10 Gb/s			
10GBASE-PR-D1	OLT	10 Gb/s	10	One single-mode fiber PON	91
10GBASE-PR-U1	ONU				
10GBASE-PR-D2	OLT	10 Gb/s	20	One single-mode fiber PON	91
10GBASE-PR-U2	ONU				
10GBASE-PR-D3	OLT	10 Gb/s	20	One single-mode fiber PON	91
10GBASE-PR-U3	ONU				

[a]Symmetric

Change paragraph below Table 56-1

Table 56 specifies the correlation between nomenclature and clauses for P2P systems, while Table 56–3specifies the correlation between nomenclature and clauses for P2MP systems. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Replace Table 56-2 with the following table.

Table 56–2—Nomenclature and clause correlation for P2P systems[a]

Nomenclature	**Clause**									
	@@57@@	**@@58@@**		**@@59@@**		**@@61@@**	**@@62@@**	**@@63@@**	**@@66@@**	
	OAM	**100BASE-LX10 PMD**	**100BASE-BX10 PMD**	**1000BASE-LX10 PMD**	**1000BASE-BX10 PMD**	**Cu PCS**	**10PASS-TS PMA & PMD**	**2BASE-TL PMA & PMD**	**100BASE-X PCS, PMA**	**1000BASE-X PCS, PMA**
2BASE-TL	O					M		M		
10PASS-TS	O					M	M			
100BASE-LX10	O	M							M	
100BASE-BX10	O		M						M	
1000BASE-LX10	O			M						M
1000BASE-BX10	O				M					M

[a]O = Optional, M = Mandatory

.Insert Table 56-3 below, renumber remaining tables

Table 56–3—Nomenclature and clause correlation for P2MP systems[a]

Nomenclature	Clause																			
	@@57@@	@@60@@		@@64@@	@@65@@		@@66@@	91											92	93
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX–D1	10/1GBASE–PRX–U1	10/1GBASE–PRX–D2	10/1GBASE–PRX–U2	10/1GBASE–PRX–D3	10/1GBASE–PRX–U3	10GBASE–PR–D1	10GBASE–PR–U1	10GBASE–PR–D2	10GBASE–PR–D3	10GBASE–PR–U3	P2MP RS, PCS, PMA FEC	10G-EPN P2MP MPMCS
1000BASE-PX10-D	O	M		M	M	O	M													
1000BASE-PX10-U	O	M		M	M	O														
1000BASE-PX20-D	O		M	M	M	O	M													
1000BASE-PX20-U	O		M	M	M	O														
10/1GBASE-PRX-D1	O			M				M											M	M
10/1GBASE-PRX-U1	O			M					M										M	M
10/1GBASE-PRX-D2	O			M						M									M	M
10/1GBASE-PRX-U2	O			M							M								M	M
10/1GBASE-PRX-D3	O			M								M							M	M
10/1GBASE-PRX-U3	O			M									M						M	M
10GBASE-PX-D1	O			M										M					M	M
10GBASE-PR-U1	O			M											M				M	M
10GBASE-PX-D2	O			M												M			M	M
10GBASE-PR-U2	O			M													M		M	M
10GBASE-PX-D3	O			M														M	M	M
10GBASE-PR-U3	O			M															M	M

[a]O = Optional, M = Mandatory

56.2 State diagrams

56.3 Protocol implementation conformance statement (PICS) proforma

Changes to ANSI/IEEE Std. IEEE 802.3ay, Clause 66

Editors' Note 66-1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

*Editing instructions are shown in 8 point arial Bold red italic font. Four editing instructions are used: **change**, **delete**, **insert**, and **replace**.*
Change *is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using strikethrough (to remove old material) or underscore (to add new material).*
Delete *removes existing material.*
Insert *adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction.*
Replace *is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions*
To simplify the addition of new tables, tables in this amendment clause are numbered based on their relationship to tables in the base document (IEEE P802.3ay D2.2). For example, Table 45-BB in this amendment would be renumbered Table-CC when the amendment is merged with IEEE P802.3ay D2.2. Continuing the example, a Table-AAb would then be renumbered Table-DD. All original table numbers in the base document can then be incremented after the merge.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

Editors' Note 66-2 (to be removed prior to release): Draft revision history for Clause 66

Version	***Date***	***Comments***
D1.3	*May 2008*	*Draft for Task Force review with comment resolution from April 2008 meeting.*
D1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting.*

66. Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport

66.1 Modifications to the physical coding sublayer (PCS) and physical medium attachment (PMA) sublayer, type 100BASE-X

66.2 Modifications to the physical coding sublayer (PCS) and physical medium attachment (PMA) sublayer, type 1000BASE-X

Change*: modify title of Subclause 66.3 by inserting “P2P” as shown below.*

66.3 Modifications to the reconciliation sublayer (RS) for P2P 10 Gb/s operation

66.3.1 Overview

Change*: modify paragraph by insertign “P2P” as shown below.*

This subclause specifies the 10 Gb/s RS for support of P2P subscriber access networks.

Insert *new section 66.4 as shown below. Renumber subsequent paragraphs as required.*

66.4 Modifications to the RS for P2MP 10 Gb/s operation

66.4.1 Overview

This subclause specifies the 10 Gb/s RS for support of P2MP subscriber access networks.

66.4.2 Functional specifications

The 10 Gb/s RS for P2MP subscriber access networks shall conform to the requirements of the 10 Gb/s RS specified in Clause 46 with the following exception: The 10 Gb/s RS for P2MP subscriber access networks may have the ability to transmit data regardless of whether the PHY has determined that a valid link has been established. The following are the detailed changes to Clause 46 in order to support this additional ability.

66.4.2.1 Link fault signaling

The description of the link fault signaling functional specification is changed to include the contribution of the new unidirectional_enable variable. The second paragraph of @@46.3.4@@ is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. The nature of the P2MP allows for some of these fault conditions to be ignored. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates ~~a Remote Fault status~~ Idle control characters on the transmit data path (possibly truncating a MAC frame being transmitted). If this variable is TRUE, the RS continues to allow the transmissions of MAC data. When Remote Fault status is received by an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates Idle control characters. If this variable is TRUE, the RS continues to allow the transmission of MAC data. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data.

66.4.2.2 Variables

Insert a new variable among those already described in @@46.3.4.2:@@

unidirectional_enable
A control variable that enables the unidirectional mode of operation.
Values: FALSE; Unidirectional capability is not enabled
TRUE; Unidirectional capability is enabled

66.4.2.3 State Diagram

The description of what the RS outputs onto TXC<3:0> and TXD<31:0> is changed to include the contribution of the new unidirectional_enable variable. The lettered list of @@46.3.4.3@@ is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

b) link_fault = Local Fault
If unidirectional_enable = FALSE, t~~T~~he RS shall continuously generate Idle control characters Remote Fault Sequence ordered_sets.
If unidirectional_enable = TRUE, the RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

c) link_fault = Remote Fault
If unidirectional_enable = FALSE, t~~T~~he RS shall continuously generate Idle control characters.
If unidirectional_enable = TRUE, the RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

***Change**: PICS Subclause becomes 66.5*

66.5 Protocol implementation conformance statement (PICS) proforma for Clause 66, Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport

***Insert**: in Subclause 66.5.3 "Major capabilities/options" add item to end of PICS (table heading shown for clarity):*

Item	Feature	Subclause	Value/Comment	Status	Support
*XP2MP	10 Gp/s P2MP operaiont	66	Device supports 10 Gb/s P2MP operation	O	Yes[] No[]

Change: add "P2P" to Subclause 66.5.4.4 title as follows:

66.5.4.4 Extensions of the 10 Gb/s ***P2P*** RS

***Insert**: Subclause 66.5.4.5 and table as follows:*

66.5.4.5 Extensions of the 10 Gb/s P2MP RS

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Integrates 10 Gb/s P2MP RS	@@66.4.2@@	See Clause 46	PUNI * XP2MP:M	Yes[]
PF2	link_fault = OK and MAC frames	@@66.4.2.3@@	RS services MAC frame transmission requests	PUNI * XP2MP:M	Yes[] No[]
PF3	link_fault = OK and no MAC frames	@@66.4.2.3@@	In absence of MAC frames, RS transmits Idle control characters.	PUNI * XP2MP:M	Yes[] No[]
PF4	link_fault = Local Fault and unidirectional_enable = FALSE	@@66.4.2.3@@	RS transmits continuous Idle control characters.	PUNI * XP2MP:M	Yes[] No[]
PF5	link_fault = Local Fault and unidirectional_enable = TRUE and MAC frames	@@66.4.2.3@@	RS services MAC frame transmission requests.	PUNI * XP2MP:M	Yes[] No[]
PF6	link_fault = Local Fault and unidirectional_enable = TRUE and no MAC frames	@@66.4.2.3@@	In absence of MAC frames, RS transmits Idle control characters.	PUNI * XP2MP:M	Yes[] No[]
PF7	link_fault = Remote Fault and unidirectional_enable = FALSE	@@66.4.2.3@@	RS transmits continuous Idle control characters.	PUNI * XP2MP:M	Yes[] No[]
PF8	link_fault = Remote Fault and unidirectional_enable = TRUE and no MAC frames	@@66.4.2.3@@	RS services MAC frame transmission requests.	PUNI * XP2MP:M	Yes[] No[]
PF9	link_fault = Remote Fault and unidirectional_enable = TRUE and no MAC frames	@@66.4.2.3@@	In absence of MAC frames, RS transmits Idle control characters.	PUNI * XP2MP:M	Yes[] No[]

67. System considerations for Ethernet subscriber access networks

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

This amendment is new material to be added to IEEE P802.3ay (D2.2). The material contained in this amendment forms the new comprehensive standard as created by the addition of IEEE P802.3av.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 67

Draft	***Date***	***Comment***
Draft 1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting*

Replace second sentence in 67.6.3 with the following statement:

This is achieved by mapping the local_link_status parameter to variable 'registered' defined in @@Subclause 64.3.3.2@@ for 1 Gb/s P2MP links and @@Subclause 93.3.3.2@@ for 10 Gb/s links as follows:

91. Physical Medium Dependent (PMD) sublayer and medium, type 10GBASE–PR (symmetric 10 Gb/s long wavelength passive optical networks) and 10/1GBASE–PRX (asymmetric 10 Gb/s downstream, 1 Gb/s upstream long wavelength passive optical networks)

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

This amendment is new material to be added to IEEE P802.3ay (D2.2). The material contained in this amendment forms the new comprehensive standard as created by the addition of IEEE P802.3av.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 91

Draft	**Date**	**Comment**
Draft 0.8	Jul 2007	Preliminary draft outline for IEEE P802.3av Task Force
Draft 0.9	Sep 2007	Preliminary draft for IEEE P802.3av Task Force
Draft 0.91	Oct 2007	Initial draft for IEEE P802.3av Task Force (pre–release)
Draft 1.0	Nov 2007	Initial draft for IEEE P802.3av Task Force
Draft 1.1	Feb 2008	Draft for Task Force review with comment resolution from January 2008 meeting
Draft 1.2	Apr 2008	Draft for Task Force review with comment resolution from March 2008 meeting
Draft 1.3	Apr 2008	Draft for Task Force review with comment resolution from April 2008 meeting
Draft 1.8023	Jun 2008	Draft for Task Force review with comment resolution from May 2008 meeting

91.1 Overview

Clause 91 describes Physical Medium dependent (PMD) sublayer for Ethernet Passive Optical Networks operating at the line rate of 10.3125 GBd in either downstream or in both downstream and upstream directions.

91.1.1 Terminology and conventions

The following list contains references to terminology and conventions used in Clause 91:

Basic terminology and conventions, see @@Subclause 1.1@@ and @@Subclause 1.2@@.

Normative references, see @@Subclause 1.3@@.

Definitions, see @@Subclause 1.4@@.

Abbreviations, see @@Subclause 1.5@@.

Informative references, see @@Annex A@@.

Introduction to 1000 Mb/s baseband networks, see @@Clause 34@@.

Introduction to 10 Gb/s baseband network, see @@Clause 44@@.

Introduction to Ethernet for subscriber access networks, see @@Clause 56@@.

EPONs operate over point–to–multipoint (P2MP) topology, also called a tree topology or trunk–and–branch. The device connected at the root of the tree is called Optical Line Terminal (OLT) and devices connected as the leaves are referred to as Optical network Units (ONUs). The direction of the transmission from the OLT to ONUs is referred to as *downstream* direction, while the direction from ONUs to the OLT is referred to as *upstream* direction.

91.1.2 Goals and objectives

The following are the PMD objectives fulfilled by Clause 91:

a) Support subscriber access networks using point–to–multipoint topologies on optical fiber.
b) Provide physical layer specifications:
   1) PHY for PON, 10 Gb/s downstream / 1 Gb/s upstream, a single SMF
   2) PHY for PON, 10 Gb/s downstream / 10 Gb/s upstream, a single SMF
c) PHY(s) to have a BER better than or equal to 10^{-12} at the PHY service interface.
d) Define up to 3 optical power budgets that support split ratios of at least 1:16 and at least 1:32, and distances of at least 10 and at least 20 km.

91.1.3 Power Budget Classes

To support the above–stated objectives, Clause 91 defines three power budget classes:

- *Low power budget class* supports P2MP media channel insertion loss of ≤ 20 dB e.g. a PON with the split ratio of at least 1:16 and the distance of at least 10 km;
- *Medium power budget class* supports P2MP media channel insertion loss of ≤ 24 dB e.g. a PON with the split ratio of at least 1:16 and the distance of at least 20 km or a PON with the split ratio of at least 1:32 and the distance of at least 10 km;
- *High power budget class* supports P2MP media channel insertion loss of ≤ 29 dB e.g. a PON with the split ratio of at least 1:32 and the distance of at least 20 km.

91.1.4 Power Budgets

Each power budget class is represented by PRX–type power budget and PR–type power budget.

- PRX–type power budget describes PHY for PON operating at 10 Gb/s downstream and 1 Gb/s upstream over a single SMF (see objective b.1 above). PRX–type power budgets are also called *asymmetric*.
- PR–type power budget describes PHY for PON operating at 10 Gb/s downstream and 10 Gb/s upstream over a single SMF (see objective b.2 above). PR–type power budgets are also called *symmetric*.

Each power budget is further identified with a numeric representation of its class, where value of 10 represents low power budget, value of 20 represents medium power budget, and value of 30 represents high power budget. Thus, the following power budgets are defined in Clause 91:

- PRX10 – asymmetric, low power budget, compatible with PX10 power budget defined in @@Clause 60@@;
- PRX20 – asymmetric, medium power budget, compatible with PX20 power budget defined in @@Clause 60@@;
- PRX30 – asymmetric, high power budget;
- PR10 – symmetric, low power budget, compatible with PX10 power budget defined in @@Clause 60@@;
- PR20 – symmetric, medium power budget, compatible with PX10 power budget defined in @@Clause 60@@;
- PR30 – symmetric, high power budget;

Table 91–1 shows the primary attributes of all power budget types defined in Clause 91.

Table 91–1—Power budgets defined in Clause 91

Description	Low Power Budget		Medium Power Budget		High Power Budget		Units
	PRX10	PR10	PRX20	PR20	PRX30	PR30	
Fiber type	B1.1, B1.3 SMF						–
Number of fibers	1						–
Nominal downstream line rate	10.3125						GBd
Nominal upstream line rate	1.25	10.3125	1.25	10.3125	1.25	10.3125	GBd
Nominal downstream wavelength	1590				1577		nm
Downstream wave-length band width	20				6		nm
Nominal upstream wavelength	1310	1270	1310	1270	1310	1270	nm
Upstream wavelength band width	100	20	100	20	100	20	nm
Maximum reach	≥10		≥20		≥20		km
Minimum reach	≤0.5						m
Maximum channel insertion loss	20		24		29		dB
Minimum channel insertion loss	5		10		15		dB

91.1.5 Positioning of PMD sublayer within the IEEE 802.3 architecture

Figure 91–1 and Figure 91–2 depict the relationships of the 10 Gb/s symmetric and 10/1 Gb/s asymmetric PMD sublayer (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

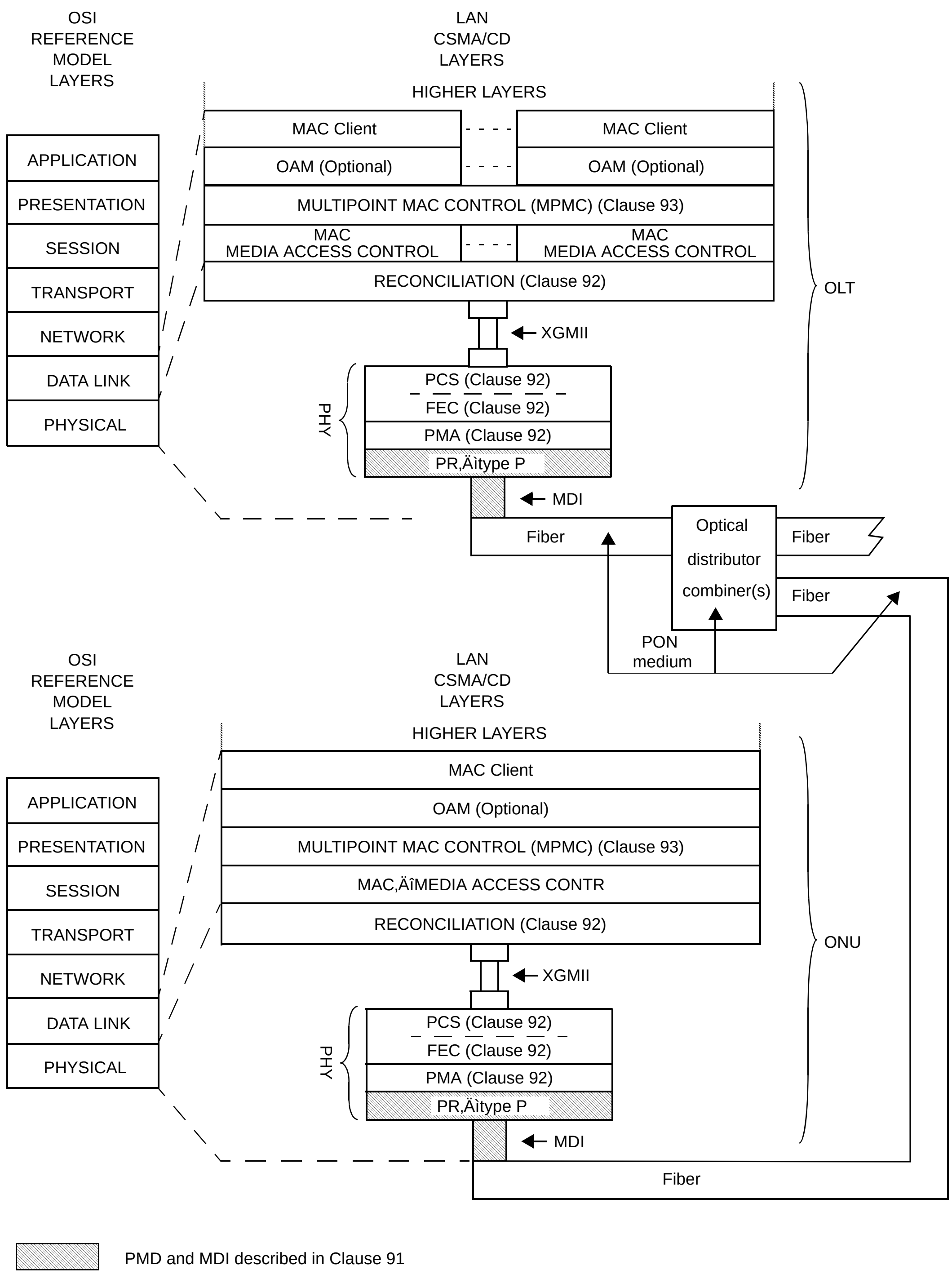
91.2 PMD Types

Similarly to power budget classes, asymmetric and symmetric PMDs are identified by PRX and PR designa-tions, respectively.

The characteristics of the P2MP topology result in significantly different ONU and OLT PMDs. For exam-ple, the OLT PMD operates in a continuous mode in the transmit direction (downstream), but uses a burst mode in the receive direction (upstream). On the other hand, the ONU PMD receives data in a continuous mode, but transmits in a burst mode. To differentiate OLT PMDs from ONU PMDs, the OLT PMD name has a suffix “D” appended to it, where D stands for downstream–facing PMD, e.g., 10GBASE–PR–D1. ONU PMDs have suffix “U” for upstream–facing PMD, e.g., 10GBASE–PR–U1.

In the downstream direction, the signal transmitted by the D–type PMD is received by all U–type PMDs. In the upstream direction, the D–type PMD receives data bursts from each of U–type PMDs.

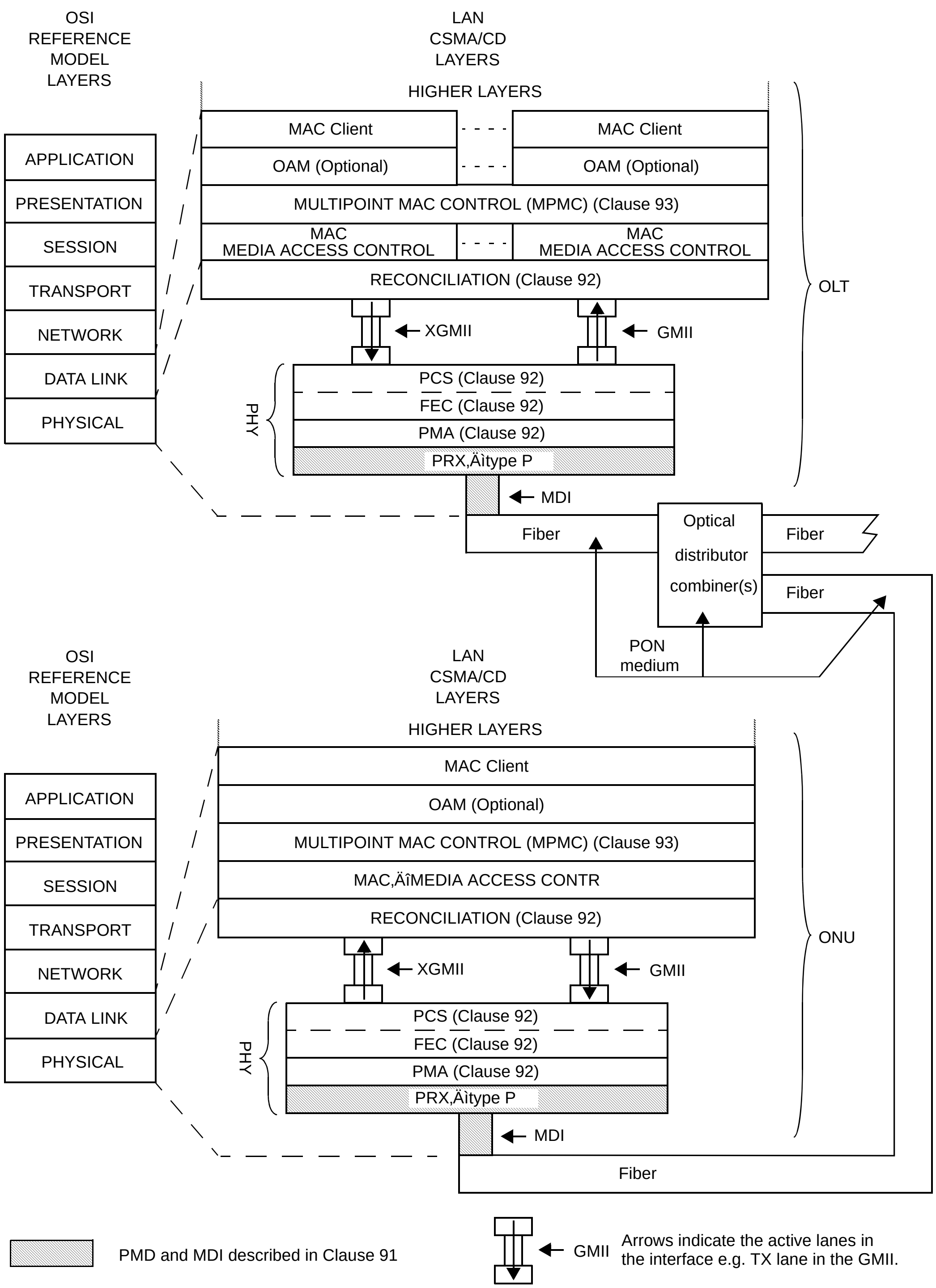
Clause 91 defines several D–type and several U–type PMDs, that differ in their receive and/or transmit char-acteristics. Such PMDs are further distinguished by appending a digit after the suffix D or U, e.g., 10GBASE–PR–D1 or 10GBASE–PR–D2.



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 91–1—Relationship of 10 Gb/s symmetric P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN model



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
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PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 91–2—Relationship of 10/1 Gb/s asymmetric P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN model.

The following OLT PMDs (D–type) are defined in this section:

1) asymmetric D–type PMDs (collectively referred to as 10/1GBASE–PRX–D), transmitting at 10.3125 GBd continuous mode and receiving at 1.25 GBd burst mode:
   i) 10/1GBASE–PRX–D1
   ii) 10/1GBASE–PRX–D2
   iii) 10/1GBASE–PRX–D3
2) symmetric D–type PMDs (collectively referred to as 10GBASE–PR–D), transmitting at 10.3125 GBd continuous mode and receiving at 10.3125 GBd burst mode:
   i) 10GBASE–PR–D1
   ii) 10GBASE–PR–D2
   iii) 10GBASE–PR–D3

The following ONU PMDs (U–type) are defined in this section:

1) asymmetric U–type PMDs (collectively referred to as 10/1GBASE–PRX–U), transmitting at 1.25 GBd burst mode and receiving at 10.3125 GBd continuous mode:
   i) 10/1GBASE–PRX–U1
   ii) 10/1GBASE–PRX–U2
   iii) 10/1GBASE–PRX–U3
2) symmetric U–type PMDs (collectively referred to as 10GBASE–PR–U), transmitting at 10.3125 GBd burst mode and receiving at 10.3125 GBd continuous mode:
   i) 10GBASE–PR–U1
   ii) 10GBASE–PR–U3

A specific power budget is achieved by combining an OLT PMD (D–type) with an ONU PMD (U–type) as shown in Clause 91.2.1 below. Detailed PMD receive and transmit characteristics for D–type PMDs are given in Clause 91.4 and characteristics for U–type PMDs are presented in Clause 91.5. Every PMD has non–overlapping transmit and receive wavelength bands and operates over a single SMF (see Subclause 91.6.1).

91.2.1 Mapping of PMDs to Power Budgets

The end–to–end power budget is determined by the PMDs located at the ends of the physical media. This section describes how PMDs may be combined to achieve the power budgets listed in Table 91–1.

91.2.1.1 Asymmetric, 10 Gb/s downstream and 1 Gb/s upstream power budgets (PRX type)

Table 91–2 illustrates recommended parings of asymmetric ONU PMDs with asymmetric OLT PMDs to achieve the power budgets as shown in Table 91–1.

Table 91–2—PMD – power budget mapping for asymmetric PRX–type power budgets

		OLT PMDs		
		10/1GBASE–PRX–D1	**10/1GBASE–PRX–D2**	**10/1GBASE–PRX–D3**
ONU PMDs	**10/1GBASE–PRX–U1**	PRX10	N/A	N/A
	10/1GBASE–PRX–U2	N/A	PRX20	N/A
	10/1GBASE–PRX–U3	N/A	N/A	PRX30

91.2.1.2 Symmetric, 10 Gb/s power budgets (PR type)

Table 91–3 illustrates recommended parings of symmetric ONU PMDs with symmetric OLT PMDs to achieve the power budgets as shown in Table 91–1

Table 91–3—PMD – power budget mapping for symmetric PR–type power budgets

		OLT PMDs		
		10GBASE–PR–D1	**10GBASE–PR–D2**	**10GBASE–PR–D3**
ONU PMDs	**10GBASE–PR–U1**	PR10	PR20	N/A
	10GBASE–PR–U3	N/A	N/A	PR30

91.3 PMD functional specifications

The 10GBASE–PR and 10/1GBASE–PRX type PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

91.3.1 PMD service interface

The following specifies the services provided by Clause 91 PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of a continuous stream of bits, representing either 64B/66B blocks (the transmit and receive paths in 10GBASE–PR PMDs, transmit path in 10/1GBASE–PRX–D PMDs) or 8B/10B blocks (transmit path in 10/1GBASE–PRX–U PMDs, receive path in 10/1GBASE–PRX–D PMDs), between the PMA and PMD entities. The PMD translates the serialized data received from the compatible PMA to and from signals suitable for the specified medium. The following primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indication

PMD_SIGNAL.request

PMD_SIGNAL.indication

91.3.1.1 Delay constraints

An upper bound to the delay through the PMD is required for predictable operation of the MAC Control MPCP operation. The PMD shall introduce a constant transmit delay of not more than 4 time–quanta and constant receive delay of not more than 4 time–quanta. A description of the overall system delay constraints can be found in @@Subclause 93.3.2.4@@, and the definition for the time_quantum can be found in @@Subclause 93.2.2.1@@.

91.3.1.2 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the @@Clause 65@@ or @@Clause 92@@ PMA to the PMD.

The semantics of the service primitive are PMD_UNITDATA.request(tx_bit). The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO. The @@Clause 92@@ PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling speed of 10.3125 GBd in the case of symmetric OLT, symmetric ONU and asymmetric OLT PMDs. The @@Clause 65@@ PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling speed of 1.25 GBd in the case of asymmetric ONU PMDs. Upon the receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

91.3.1.3 PMD_UNITDATA.indication

This primitive defines the transfer of data from the PMD to the @@Clause 65@@ or @@Clause 92@@ PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(rx_bit). The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the @@Clause 92@@ PMA corresponding to the signals received from the MDI, at the nominal signaling speed of 10.3125 GBd in the case of symmetric OLT, symmetric ONU and asymmetric ONU PMDs or to the @@Clause 65@@ PMA at the nominal signaling speed of 1.25 GBd in the case of asymmetric OLT PMDs.

91.3.1.4 PMD_SIGNAL.request

In the upstream direction, this primitive is generated by the @@Clause 92@@ PCS to turn on and off the transmitter according to the granted time. A signal for laser control is generated as described in @@Subclause 92.3.1.1@@ for @@Clause 92@@ PCS.

The semantics of the service primitive are PMD_SIGNAL.request(tx_enable). The tx_enable parameter can take on one of two values: ENABLE or DISABLE, determining whether the PMD transmitter is on (enabled) or off (disabled). The @@Clause 92@@ PCS generates this primitive to indicate a change in the value of tx_enable. Upon the receipt of this primitive, the PMD turns the transmitter on or off as appropriate.

91.3.1.5 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

The semantics of the service primitive are PMD_SIGNAL.indication(SIGNAL_DETECT). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio. PMD_SIGNAL.indication(SIGNAL_DETECT) has different characteristics for upstream and downstream links, Subclause 91.3.5.

91.3.2 PMD block diagram

The PMD sublayer is defined at the eight reference points shown in Figure 91–3 for 10GBASE–PR PMDs and in Figure 91–4 for 10/1GBASE–PRX PMDs. In Figure 91–3 and Figure 91–4, test points in ovals represent the downstream channel, while the test points in rectangles represent the upstream channel.

For 10GBASE–PR PMDs, test points TP1 – TP4 refer to the downstream channel, while test points TP5 – TP8 refer to the upstream channel. In the downstream channel, TP2 and TP3 are compliance points, while in the upstream channel TP6 and TP7 are compliance points. TP1 and TP4 and TP5 and TP8 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2 for the downstream channel and TP6 in the upstream channel), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in Subclause 91.9 are made at TP2 and TP6. The optical receive signal is defined at the output of the fiber optic cabling (TP3 for the downstream channel and TP7 for the upstream channel) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in Subclause 91.9 are made at TP3 and TP7.

The electrical specifications of the PMD service interface (TP1 and TP4 for the downstream channel and TP5 and TP8 for the upstream channel) are not system compliance points (these are not readily testable in a system implementation).

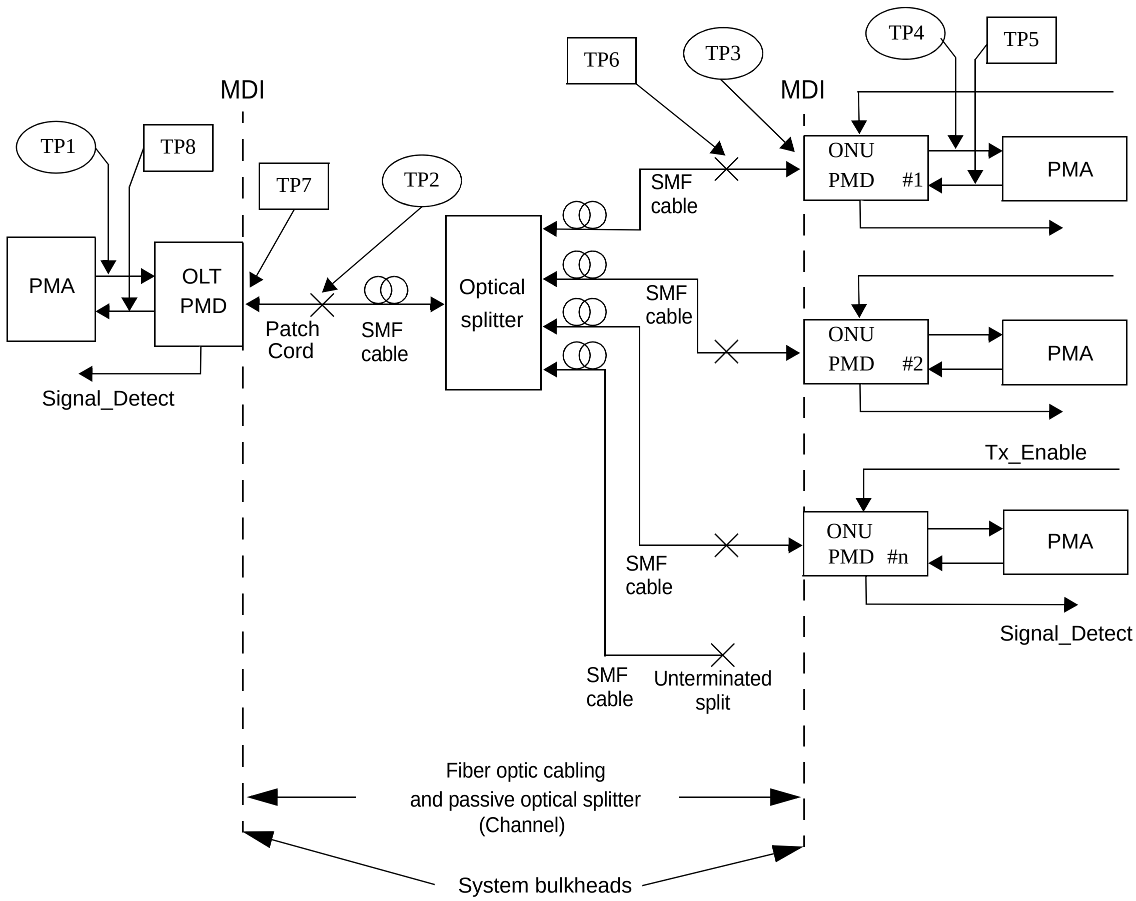


Figure 91–3—10GBASE–PR block diagram

For 10/1GBASE–PRX PMDs, test points TP1 – TP4 refer to the downstream channel (ovals), while test points TP1 – TP4 (rectangles) refer to the upstream channel. Two points, TP2 and TP3, are compliance points. TP1 and TP4 are reference points for use by Implementers. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in @@Subclause 60.7@@ are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in Subclause 91.9 are made at TP3.

The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation).

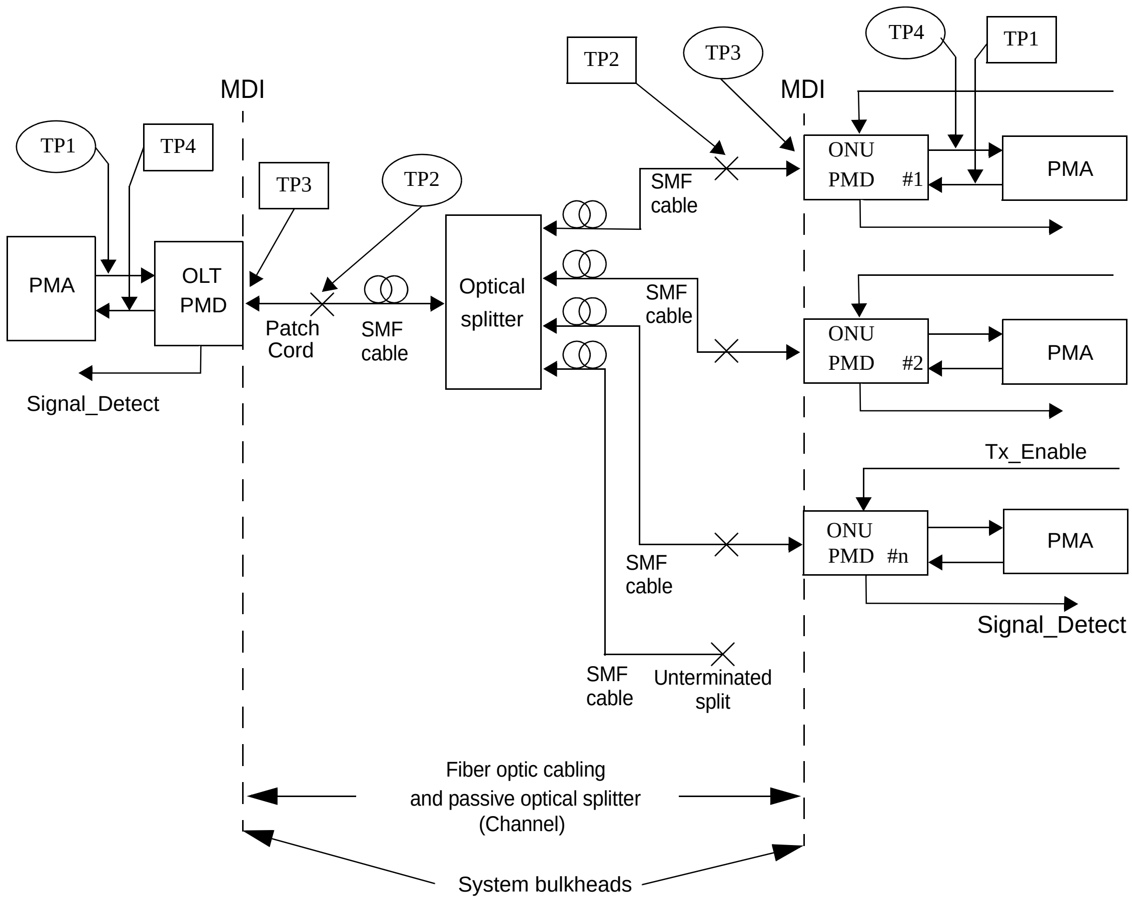


Figure 91–4—10/1GBASE–PRX block diagram

91.3.3 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in Clause 91.

In the upstream direction, the flow of bits is interrupted according to PMD_SIGNAL.request(tx_enable). This implies three optical levels, 1, 0, and dark, the latter corresponding to the transmitter being in the OFF state. The higher optical power level shall correspond to tx_bit = ONE.

91.3.4 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in Clause 91 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

91.3.5 PMD signal detect function

91.3.5.1 ONU PMD signal detect

The PMD Signal Detect function for the continuous mode downstream signal shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT) which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of the presence of the optical signal.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 91–4 for 10GBASE–PR and 10/1GBASE–PRX type PMDs. The ONU PMD receiver is not required to verify whether a compliant 10GBASE–PR signal is being received.

91.3.5.2 OLT PMD signal detect

The response time for the PMD Signal Detect function for the burst mode upstream signal may be longer or shorter than a burst length, thus, it may not fulfill the traditional requirements placed on Signal Detect. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. The signal detect function in the OLT may be realized in the PMD or the @@Clause 92@@ PMA sub–layer.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 91–4 for Clause 91 type PMDs. The 10GBASE–PR–D PMD receiver is not required to verify whether a compliant 10GBASE–PR signal is being received. Similarly, the 10/1GBASE–PRX–D PMD receiver is not required to verify whether a compliant 1000BASE–PX signal is being received.

91.3.5.3 10GBASE–PR and 1000BASE–PX Signal detect functions

The Signal Detect value definitions for Clause 91 PMDs are shown in Table 91–4.

Table 91–4—SIGNAL_DETECT value definitions for Clause 91 PMDs

Receive conditions			**Signal_detect value**
10GBASE–PR–D1, 10GBASE–PR–D2, 10GBASE–PR–D3	**10GBASE–PR–U1, 10GBASE–PR–U3, 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2, 10/1GBASE–PRX–U3**	**10/1GBASE–PRX–D1, 10/1GBASE–PRX–D2, 10/1GBASE–PRX–D3**	
Average input optical power ≤ Signal Detect Threshold (min) in Table 91–6 at the specified receiver wavelength	Average input optical power ≤ Signal Detect Threshold (min) in Table 91–11 at the specified receiver wavelength	Average input optical power ≤ Signal Detect Threshold (min) in Table 91–7 at the specified receiver wavelength	FAIL
Average input optical power ≥ Receive sensitivity (max) in Table 91–6 with a compliant 10GBASE–PR signal input at the specified receiver wavelength	Average input optical power ≥ Receive sensitivity (max) in Table 91–11 with a compliant 10GBASE–PR signal input at the specified receiver wavelength	Average input optical power ≥ Receive sensitivity (max) in Table 91–7 with a compliant 1000BASE–PX signal input at the specified receiver wavelength	OK
All other conditions	All other conditions	All other conditions	Unspecified

91.3.6 PMD transmit enable function for ONU

PMD_SIGNAL.request(tx_enable) is defined for all ONU PMDs specified in Clause 91. PMD_SIGNAL.request(tx_enable) is asserted prior to data transmission by the ONU PMDs.

91.4 PMD to MDI optical specifications for symmetric and asymmetric OLT PMDs.

This section details the PMD to MDI optical specifications for symmetric and asymmetric OLT PMDs, as specified in Subclause 91.2. Specifically, Subclause 91.4.1 defines the OLT transmit parameters, while Subclause 91.4.2 defines the OLT receive parameters.

The operating ranges for PR and PRX power budget classes are defined in Table 91–1. A PR and PRX compliant transceiver operates over the media types listed in Table 91–20 according to the specifications described in Subclause 91.11. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single–mode solution operating at 10.5 km meets the minimum range requirement of 0.5 m to 10 km for PR10).

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in @@Subclause 58.7.6@@.

91.4.1 Transmitter optical specifications

The signaling speed, operating wavelength, side mode suppression ratio, average launch power, extinction ratio, return loss tolerance, OMA, eye and Transmitter and Dispersion Penalty (TDP) for transmitters making part of the symmetric and asymmetric OLT PMDs (as specified in Subclause 91.2) shall meet the specifications defined in Table 91–5 per measurement techniques described in Subclause 91.9. Its $RIN_{15}OMA$ should meet the value listed in Table 91–5 per measurement techniques described in Subclause 91.9.8. Note that 10GBASE–PR–D1 and 10/1GBASE–PRX–D1, 10GBASE–PR–D2 and 10/1GBASE–PRX–D2 and finally 10GBASE–PR–D3 and 10/1GBASE–PRX–D3 share the same transmit parameters.

Table 91–5—PR and PRX type OLT PMD transmit characteristics

Description	10GBASE–PR–D1 and 10/1GBASE–PRX–D1	10GBASE–PR–D2 and 10/1GBASE–PRX–D2	10GBASE–PR–D3 and 10/1GBASE–PRX–D3	Unit
Signaling speed (range)	10.3125 ± 100 ppm	10.3125 ± 100 ppm	10.3125 ± 100 ppm	GBd
Wavelength (range)	1580 to 1600	1580 to 1600	1574 to 1580	nm
Side Mode Suppression Ratio (min)[a]	30	30	30	dB
Average launch power (max)	4	9	5	dBm
Average launch power (min)[b]	1	5	2	dBm
Average launch power of OFF transmitter (max)	–39	–39	–39	dBm
Extinction ratio (min)	6	6	6	dB
$RIN_{15}OMA$ (max)	–128	–128	–128	dB/Hz
Launch OMA (min)[b]	2.91 (1.95)	6.91 (4.91)	3.91 (2.46)	dBm (mW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}	UI
Optical return loss tolerance (max)	15	15	15	dB
Transmitter reflectance (max)	–10	–10	–10	dB
Transmitter and dispersion penalty (max)	1.5	1.5	1.5	dB
Decision timing offset for transmitter and dispersion penalty	±0.05	±0.05	±0.05	UI

[a]Transmitter is a single longitudinal mode device. Chirp is allowed such that the total optical path penalty does not exceed that found in Table 91–13.
[b]Minimum average launch power and minimum launch OMA are valid for ER = 9 dB (see Figure 91–5 for details)

The relationship between OMA, extinction ratio and average power is described in @@Subclause 58.7.6@@ and illustrated in Figure 91–5 for a compliant transmitter. Note that the OMA_{min} and AVP_{min} are calculated for the ER = 9 dB, where AVP_{min} represents the Average launch power (min) as presented in Table 91–5. The transmitter specifications are further relaxed by allowing lower ER = 6 dB while maintaining the OMA_{min} and AVP_{min} constant. Shaded area indicates compliant part.

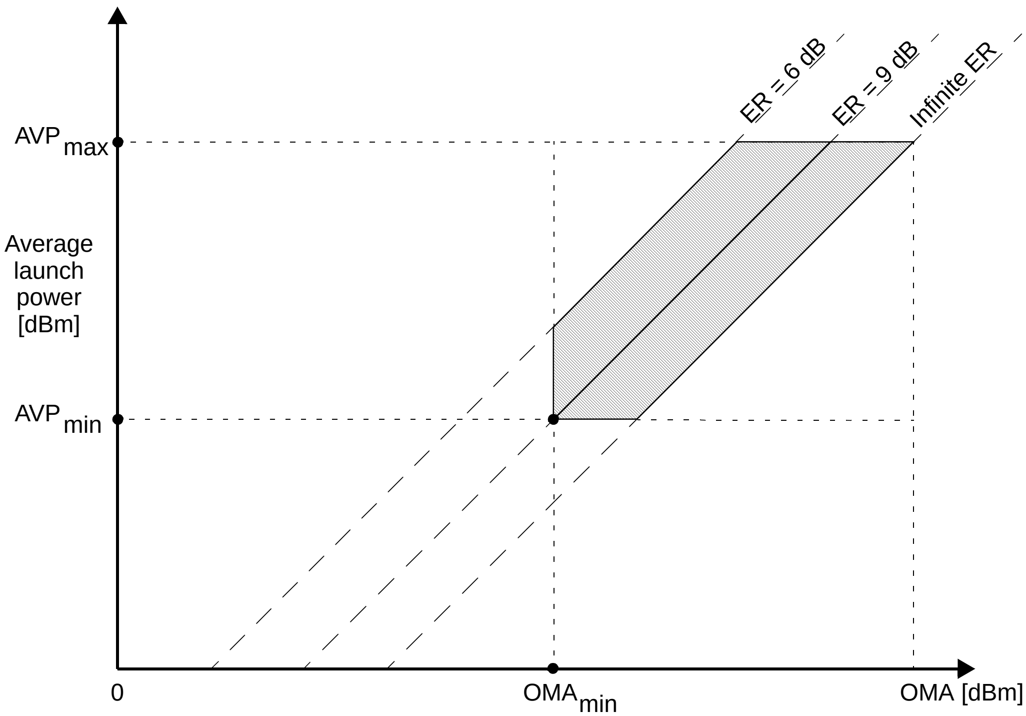


Figure 91–5—Relaxed PR–D type PMD specifications.

91.4.2 Receiver optical specifications

The signaling speed, operating wavelength, overload, stressed sensitivity, reflectivity and signal detect for receivers making part of the symmetric and asymmetric OLT PMDs (as specified in Clause 91.2) shall meet the specifications defined in Table 91–6 for symmetric OLT PMDs and in Table 91–7 for asymmetric OLT PMDs, per measurement techniques defined in Subclause 91.9. Its (unstressed) receive characteristics should meet the values listed in Table 91–6 and Table 91–7 per measurement techniques described in Subclause 91.9.11. Either the damage threshold included in Table 91–6 and Table 91–7 shall be met, or, the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage.

Damage threshold included in Table 91–6 and Table 91–7 does not guarantee direct ONU–OLT connection, which may result in damage of the receiver. If direct ONU–OLT connection is necessary, optical attenuators and/or equivalent loss components should be inserted to decrease receive power below damage threshold.

Table 91–6—PR type OLT PMD receive characteristics

Description	10GBASE –PR–D1	10GBASE –PR–D2	10GBASE –PR–D3	Unit
Signaling speed (range)	10.3125 ± 100 ppm	10.3125 ± 100 ppm	10.3125 ± 100 ppm	GBd
Wavelength (range)	1260 to 1280	1260 to 1280	1260 to 1280	nm
Bit error ratio (max)[a]	10^{-3}	10^{-3}	10^{-3}	–
Average receive power (max)	–1	–6	–6	dBm
Damage threshold (max)[b]	0	–5	–5	dBm
Receiver sensitivity (max)	–24	–28	–28	dBm
Receiver sensitivity OMA (max)	–23.22 (4.77)	–27.22 (1.90)	–27.22 (1.90)	dBm (μW)
Signal detect threshold (min)	–45	–45	–45	dBm
Receiver reflectance (max)	–12	–12	–12	dB
Stressed receive sensitivity (max)[c]	–21	–25	–25	dBm
Stressed receive sensitivity OMA (max)	–20.22 (9.51)	–24.22 (3.79)	–24.22 (3.79)	dBm (μW)
Vertical eye–closure penalty[d]	2.99	2.99	2.99	dB
$T_{receiver\_settling}$ (max)[e]	800	800	800	ns
Stressed eye jitter	0.3	0.3	0.3	UI pk to pk
Jitter corner frequency for a sinusoidal jitter	4	4	4	MHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	(0.05, 0.15)	UI

[a]The BER of 10^{-12} is achieved by the utilization of FEC as described in @@Subclause 92.2@@.
[b]Direct ONU–OLT connection may result in damage of the receiver.
[c]The stressed receiver sensitivity is mandatory.
[d]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.
[e]$T_{receiver\_settling}$ represents an upper bound. Optics with better performance may be used in compliant implementations, since the OLT notifies the ONUs on its requirements in terms of the $T_{receiver\_settling}$ time via the SYNCTIME parameter (see @@Subclause 93.3.3.2@@).

Table 91–7—PRX type OLT PMD receive characteristics

Description	10/1GBASE –PRX–D1	10/1GBASE –PRX–D2	10/1GBASE –PRX–D3	Unit
Signaling speed (range)	same as 1000BASE–PX10–D receive parameters (see Table 60–5)	same as 1000BASE–PX20–D receive parameters (see Table 60–8)	1.25 ± 100 ppm	GBd
Wavelength (range)			1260 to 1360	nm
Bit error ratio (max)			10^{-12}	
Average receive power (max)			–9.38	dBm
Damage threshold (max)			–8.38	dBm
Receiver sensitivity (max)			–29.78	dBm
Receiver sensitivity OMA (max)			–29.00 (1.26)	dBm (μW)
Signal detect threshold (min)			–45	dBm
Receiver reflectance (max)			–12	dB
Stressed receive sensitivity (max)[a]			–28.38	dBm
Stressed receive sensitivity OMA (max)			–27.60 (1.74)	dBm (μW)
Vertical eye–closure penalty[b]			1.4	dB
$T_{receiver\_settling}$ (max)[c]			400	ns
Stressed eye jitter			0.28	UI pk to pk
Jitter corner frequency for a sinusoidal jitter			637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)			(0.05, 0.15)	UI

[a]The stressed receiver sensitivity is mandatory.
[b]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.
[c]$T_{receiver\_settling}$ represents an upper bound. Optics with better performance may be used in compliant implementations, since the OLT notifies the ONUs on its requirements in terms of the $T_{receiver\_settling}$ time via the SYNCTIME parameter (see @@Subclause 93.3.3.2@@).

91.5 PMD to MDI optical specifications for symmetric and asymmetric ONU PMDs.

This section details the PMD to MDI optical specifications for symmetric and asymmetric ONU PMDs, as specified in Subclause 91.2. Specifically, Subclause 91.5.1 defines the ONU transmit parameters, while Subclause 91.5.2 defines the ONU receive parameters.

The operating ranges for PR10, PR20, PR30 power budget classes are defined in Table 91–1. The operating ranges for PRX10, PRX20, PRX30 power budget classes are defined in Table 91–1. A PR10, PR20, PR30, PRX10, PRX20 or PRX30 compliant transceiver operates over the media types listed in Table 91–20 according to the specifications described in Subclause 91.11. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single–mode solution operating at 10.5 km meets the minimum range requirement of 0.5 m to 10 km for PR10).

NOTE—The specifications for OMA have been derived from extinction ratio of 9 dB and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in @@Subclause 58.7.6@@.

91.5.1 Transmitter optical specifications

The signaling speed, operating wavelength, spectral width (for asymmetric ONU PMDs) or side mode suppression ratio (for symmetric ONU PMDs), average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP for transmitters making part of the symmetric and asymmetric ONU PMDs (as specified in Subclause 91.2) shall meet the specifications defined in Table 91–8 for symmetric ONU PMDs and in Table 91–9 for asymmetric ONU PMDs, per measurement techniques described in Subclause 91.9. Its $RIN_{15}OMA$ should meet the value listed in Table 91–8 and Table 91–9 per measurement techniques described in Subclause 91.9.8.

Table 91–8—PR type ONU PMD transmit characteristics

Description	10GBASE –PR–U1	10GBASE –PR–U3	Unit
Signaling speed (range)	10.3125 ± 100 ppm	10.3125 ± 100 ppm	GBd
Wavelength (range)	1260 to 1280	1260 to 1280	nm
Side Mode Suppression Ratio (min)[a]	30	30	dB
Average launch power (max)	4	9	dBm
Average launch power (min)[b]	–1	4	dBm
Average launch power of OFF transmitter (max)	–45	–45	dBm
Extinction ratio (min)	6	6	dB
$RIN_{15}OMA$ (max)	–128	–128	dB/Hz
Launch OMA (min)[c]	–0.22 (0.95)	4.78 (3.01)	dBm (mW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}	UI
Ton (max)	512	512	ns
Toff (max)	512	512	ns
Optical return loss tolerance (max)	15	15	dB
Transmitter reflectance (max)	–10	–10	dB
Transmitter and dispersion penalty (max)[c]	3.0	3.0	dB
Decision timing offset for transmitter and dispersion penalty	±0.0625	±0.0625	UI

[a]Transmitter is a single longitudinal mode device. Chirp is allowed such that the total optical path penalty does not exceed that found in Table 91–13.
[b]Minimum average launch power and minimum launch OMA are valid for ER = 6 dB (see Figure 91–6 for details).
[c]If a laser source has a lower TDP, the minimum transmitter launch OMA (OMA_{min}) and average minimum launch power (AVP_{min}) may be relaxed by the same amount as the TDP.

The relationship between OMA, extinction ratio and average power is described in @@Subclause 58.7.6@@ and illustrated in Figure 91–6 for a compliant transmitter. Note that the OMA_{min} and AVP_{min} are calculated for the ER = 6 dB. The transmitter average launch power specifications are further relaxed by allowing ER higher than 6 dB while maintaining the OMA_{min} constant. Shaded area indicates compliant part.

Table 91–9—PRX type ONU PMD transmit characteristics

Description	10/1GBASE –PRX–U1	10/1GBASE –PRX–U2	10/1GBASE –PRX–U3	Unit
Signaling speed (range)	same as 1000BASE–PX10–U transmit parameters (see Table 60–3)	same as 1000BASE–PX20–U transmit parameters (see Table 60–6)	1.25 ± 100 ppm	GBd
Wavelength[a] (range)			1260 to 1360	nm
RMS spectral width (max)			see [b]	nm
Average launch power (max)			5.62	dBm
Average launch power (min)[c]			0.62	dBm
Average launch power of OFF transmitter (max)			–45	dBm
Extinction ratio (min)			6	dB
$RIN_{15}OMA$ (max)			–115	dB/Hz
Launch OMA (min)[c]			1.40 (1.38)	dBm (mW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}			{0.22, 0.375, 0.20, 0.20, 0.30}	UI
Ton (max)			512	ns
Toff (max)			512	ns
Optical return loss tolerance (max)			15	dB
Transmitter reflectance (max)			–10	dB
Transmitter and dispersion penalty (max)			1.4	dB
Decision timing offset for transmitter and dispersion penalty			±0.125	UI

[a]This represents the range of center wavelength ±1σ of the rms spectral width.
[b]In case FP–LD is used, RMS spectral width shall comply with Table 91–10. In case DFB laser is used, transmitter's side mode suppression ratio (min) shall be 30 dB.
[c]Minimum average launch power and minimum launch OMA are valid for ER = 6 dB.

The maximum RMS spectral width vs. wavelength for 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2 and 10/1GBASE–PRX–U3 PMDs are shown, respectively, in @@Table 60–4@@, @@Table 60–7@@ and Table 91–10. The equation used to generate these values is included in @@Subclause 60.7.2@@. The central column values are normative, the right hand column is informative.

91.5.2 Receiver optical specifications

The signaling speed, operating wavelength, overload, stressed sensitivity, reflectivity and signal detect for receivers making part of the symmetric ONU and asymmetric ONU PMDs (as specified in Subclause 91.2) shall meet the specifications defined in Table 91–11 for Clause 91 ONU PMDs, per measurement techniques defined in Subclause 91.9. The (unstressed) receive characteristics should meet the values listed in Table 91–11 per measurement techniques described in Subclause 91.9.11. Either the damage threshold included in Table 91–11 shall be met, or the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage.

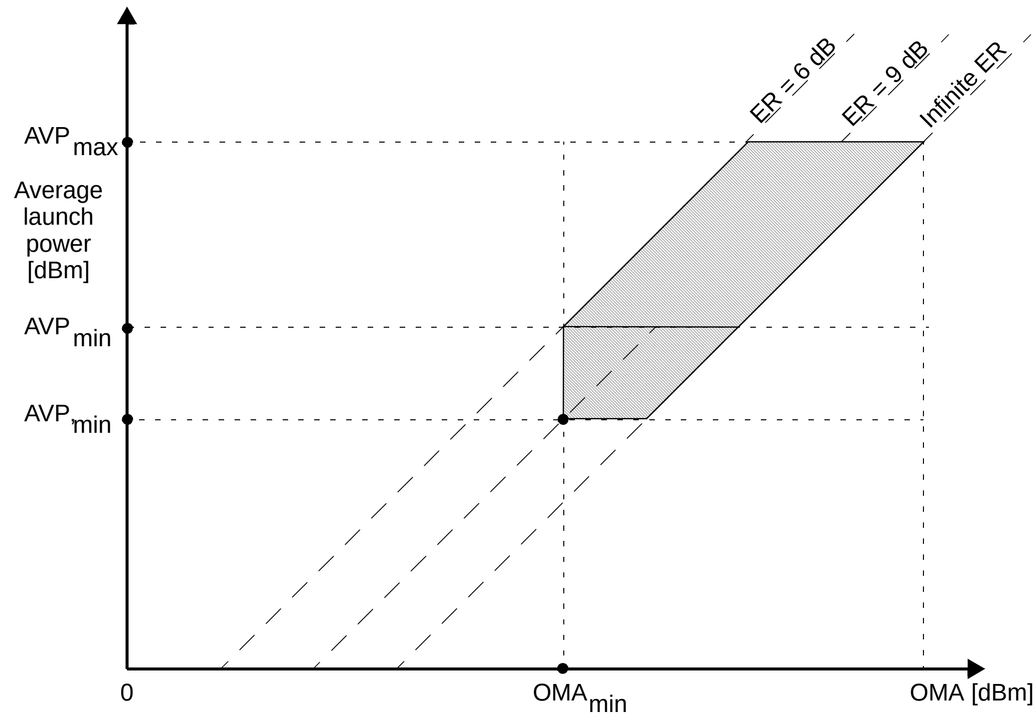


Figure 91–6—Relaxed PR–U type PMD specifications.

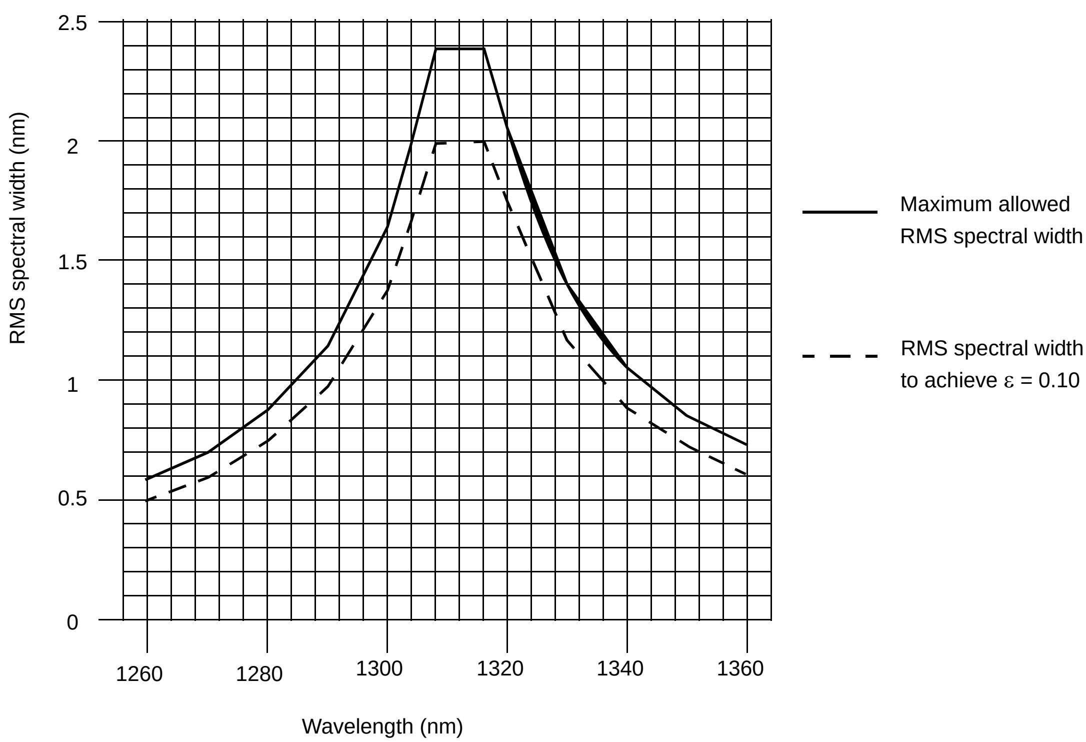


Figure 91–7—10/1GBASE–PRX–U3 transmitter spectral limits

Damage threshold included in Table 91–11 does not guarantee direct ONU–OLT connection, which may result in damage of the receiver. If direct ONU–OLT connection is necessary, optical attenuators and/or equivalent loss components should be inserted to decrease receive power below damage threshold.

Table 91–10—10/1GBASE–PRX–U3 transmitter spectral limits

Center Wavelength	RMS spectral width (max)[a]	RMS spectral width to achieve epsilon ε <=0.08 (informative)
nm	**nm**	**nm**
1260	**0.59**	0.5
1270	**0.7**	0.59
1280	**0.87**	0.74
1290	**1.14**	0.97
1300	**1.64**	1.39
1304	**1.98**	1.67
1305	**2.09**	1.77
1308	**2.4**	2
1317	**2.4**	2
1320	**2.07**	1.75
1321	**1.98**	1.67
1330	**1.4**	1.18
1340	**1.06**	0.89
1350	**0.86**	0.72
1360	**0.72**	0.61

[a]These limits for the 10/1GBASE–PRX–U3 transmitter are illustrated in Figure 91–7. The equation used to calculate these values is detailed in Subclause 60.7.2. Limits at intermediate wavelengths may be found by interpolation.

Table 91–11—PR and PRX type ONU PMD receive characteristics

Description	10GBASE–PR–U1 10/1GBASE–PRX–U1 10/1GBASE–PRX–U2	10GBASE–PR–U3 10/1GBASE–PRX–U3	Unit
Signaling speed (range)	10.3125 ± 100 ppm	10.3125 ± 100 ppm	GBd
Wavelength (range)	1580 to 1600	1574 to 1580	nm
Bit error ratio (max)[a]	10^{-3}	10^{-3}	–
Average receive power (max)	–1	–10	dBm
Damage threshold (max)[b]	0	–9	dBm
Receiver sensitivity (max)	–20.50	–28.50	dBm
Receiver sensitivity OMA (max)	–18.59 (13.84)	–26.59 (2.19)	dBm (μW)
Signal detect threshold (min)	–44	–44	dBm
Receiver reflectance (max)	–12	–12	dB
Stressed receive sensitivity (max)[c]	–19	–27	dBm

Table 91–11—PR and PRX type ONU PMD receive characteristics

Description	10GBASE–PR–U1 10/1GBASE–PRX–U1 10/1GBASE–PRX–U2	10GBASE–PR–U3 10/1GBASE–PRX–U3	Unit
Stressed receive sensitivity OMA (max)	–17.09 (19.55)	–25.09 (3.10)	dBm (μW)
Vertical eye–closure penalty[d]	1.5	1.5	dB
Stressed eye jitter (min)	0.3	0.3	UI pk to pk
Jitter corner frequency for a sinusoidal jitter	4	4	MHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	UI

[a]The BER of 10^{-12} is achieved by the utilization of FEC as described in @@Subclause 92.2@@.
[b]Direct ONU–OLT connection may result in damage of the receiver.
[c]The stressed receiver sensitivity is mandatory
[d]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

91.6 Illustrative channels and penalties (informative) for PR10, PR20, PR30, PRX10, PRX20 and PRX30 power budget classes.

Illustrative power budget for PR10, PR20 and PR30 power budget classes are shown in Table 91–12. Illustrative power budget for PRX10, PRX20 and PRX30 power budget classes are shown in Table 91–13.

Table 91–12—Illustrative PR10, PR20 and PR30 channel insertion loss and penalties (symmetric, 10 Gb/s power budget classes)

Description	PR10		PR20		PR30		Unit
	US[a]	DS[a]	US[a]	DS[a]	US[a]	DS[a]	
Fiber Type	B1.1, B1.3 SMF						
Measurement wavelength for fiber	1270	1590[b]	1270	1590[b]	1270	1577[c]	nm
Nominal distance[d]	10		20		20		km
Available power budget[e]	23	21.5	27	25.5	32	30.5	dB
Channel insertion loss (max)[f]	20		24		29		dB
Channel insertion loss (min)[g]	5		10		15		dB
Allocation for penalties[h]	3	1.5	3	1.5	3	1.5	dB
Optical return loss of ODN (min)	20						dB

[a]US stands for Upstream, DS stands for Downstream
[b]The nominal transmit wavelength is 1590 nm.
[c]The nominal transmit wavelength is 1577 nm.
[d]Nominal distance refers to the expected maximum distance a PMD will be capable of achieving in a typical ODN, numerous ODN implementation practices may result is longer or shorter distances being actually achievable in a users' network.
[e]The available power budget assumes input BER from the PMD service interface of 10^{-3}. The required BER of 10^{-12} at the PCS service interface is achieved by the FEC function of the PCS.
[f]The channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components such as splitters.
[g]The power budgets for PR10, PR20 and PR30 power budget classes are such that a minimum insertion loss is assumed between transmitter and receiver. This minimum attenuation is required for PMD testing.
[h]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst case operating wavelength is considered a penalty. This allocation may be used to compensate for transmission related penalties. Further details are given in Subclause 91.9.2.

Table 91–13—Illustrative PRX10, PRX20 and PRX30 channel insertion loss and penalties (asymmetric, 10 Gb/s downstream, 1 Gb/s upstream power budget classes)

Description	PRX10		PRX20		PRX30		Unit
	US[a]	DS[a]	US[a]	DS[a]	US[a]	DS[a]	
Fiber Type	B1.1, B1.3 SMF						
Measurement wavelength for fiber	1310	1590[b]	1310	1590[b]	1310	1577[c]	nm
Nominal distance[d]	10		20		20		km
Available power budget	23.0	21.5[e]	26.0	25.5[e]	30.4	30.5[e]	dB
Channel insertion loss (max)[f]	20		24		29		dB
Channel insertion loss (min)[g]	8	5	8	10	15	15	dB
Allocation for penalties[h]	3	1.5	3	1.5	1.4	1.5	dB
Optical return loss of ODN (min)	20						dB

[a]US stands for Upstream, DS stands for Downstream
[b]The nominal transmit wavelength is 1590 nm.
[c]The nominal transmit wavelength is 1577 nm.
[d]Nominal distance refers to the expected maximum distance a PMD will be capable of achieving in a typical ODN, numerous ODN implementation practices may result is longer or shorter distances being actually achievable in a users' network.
[e]The available power budget assumes input BER from the PMD service interface of 10^{-3}. The required BER of 10^{-12} at the PCS service interface is achieved by the FEC function of the PCS.
[f]The channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components such as splitters.
[g]The power budgets for PRX10, PRX20 and PRX30 power budget classes are such that a minimum insertion loss is assumed between transmitter and receiver. This minimum attenuation is required for PMD testing.
[h]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst case operating wavelength is considered a penalty. This allocation may be used to compensate for transmission related penalties. Further details are given in Subclause 91.9.2.

NOTE—The budgets include an allowance for –12 dB reflection at the receiver.

91.6.1 Wavelength allocation

Figure 91–7 depicts the wavelength allocation plan for EPON and 10G–EPON systems, as discussed below.

91.6.1.1 Downstream wavelength allocation

The 1 Gb/s downstream transmission uses the 1480 – 1500 nm wavelength band, as specified in @@Clause 60@@. The 10 Gb/s downstream transmission uses the 1574 – 1600 nm wavelength band, as specified in Clause 91. Therefore, there are two distinct downstream channel ranges, as depicted in Figure 91–7.

NOTE—different power budget classes use different sub–sets of the 1574 – 1600 nm band, i.e. PR10, PR20, PRX10 and PRX20 power budgets use 1580 – 1600 nm range while PR30 and PRX30 power budgets use 1574 – 1580 nm range.

An OLT supporting both downstream channels may multiplex the output of the two transmitters using a WDM coupler, while an ONU selects the relevant downstream channel using an optical filter.

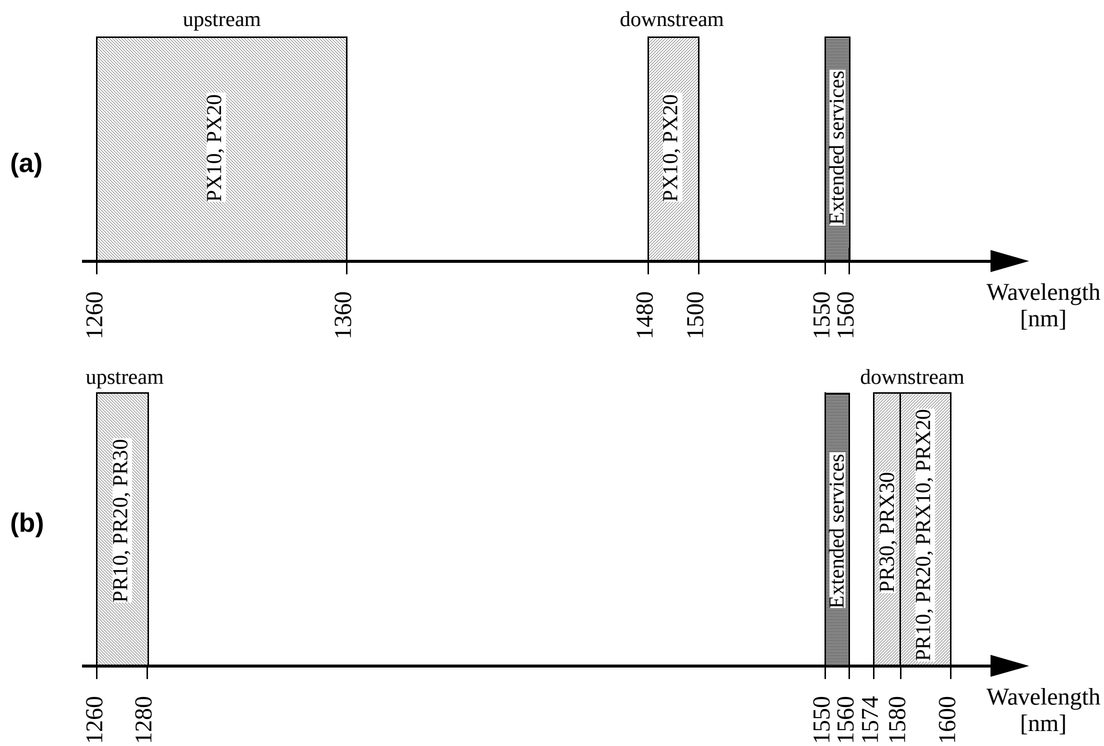


Figure 91–8—Wavelength allocation plan for (a) EPON and (b) 10G–EPON.

91.6.1.2 Upstream wavelength allocation

The 1 Gb/s upstream transmission uses the 1260 – 1360 nm wavelength band, as specified in @@Clause 60@@. The 10 Gb/s upstream transmission uses the 1260 – 1280 nm wavelength band, as specified in @@Clause 92@@. The two wavelength bands overlap, thus WDM channel multiplexing cannot be used to separate the two data channels.

An OLT supporting both upstream channels must use TDMA techniques to avoid collisions between transmissions originating from different ONUs, resulting in a dual–rate, burst mode transmission as discussed in Subclause 91.7.

91.7 Dual–rate operation (informative)

The OLT receiver must support burst mode operation. If the OLT supports a single upstream channel e.g. only 1 Gb/s or 10 Gb/s data rate, the receiver can be designed to handle the designated upstream data rate and line code. However, if the OLT supports both 1 Gb/s and 10 Gb/s upstream channels, the OLT receiver must support both data rates via TDMA.

From a topological point of view, the PMD has a single optical input, sensitive to 1260 – 1360 nm signal, and two corresponding derived electrical outputs: 1.25 GBd and 10.3125 GBd. Thus, at a certain point in the stack it is necessary to introduce a signal split, where the location of such a signal split is an implementation choice. The incoming signal can be split in the optical domain and fed into two, independent photodetectors as shown in Figure 91–9(a). Alternatively, the signal can be detected using a single photodetector as shown in Figure 91–9(b) and then split in the electrical domain after the TIA block.

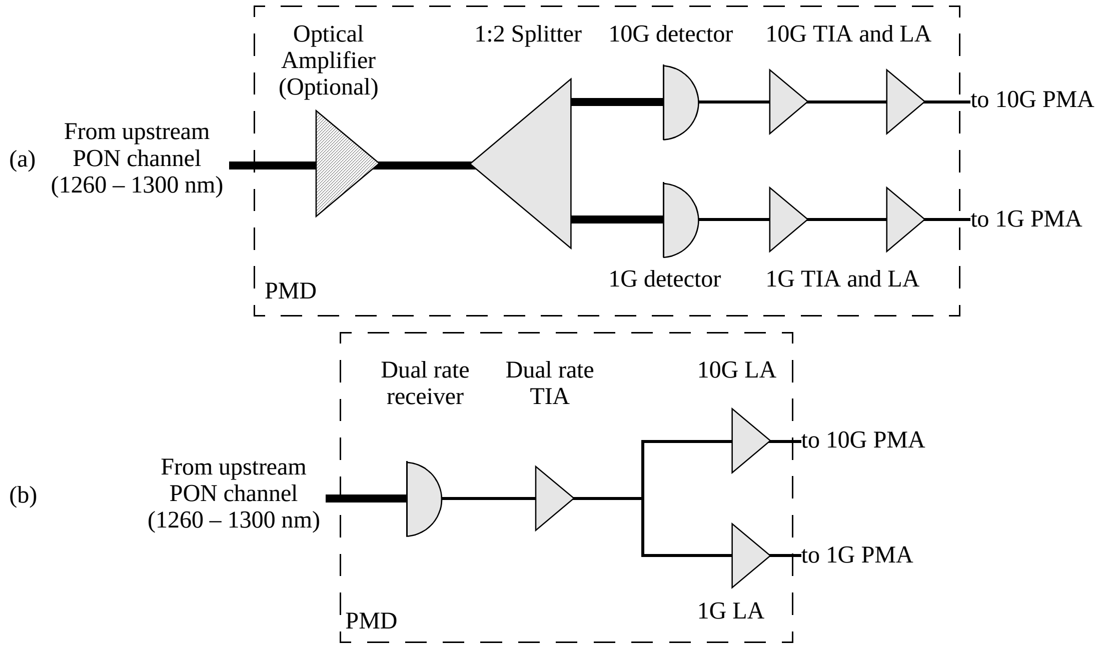


Figure 91–9—Dual–rate PMD topologies with the split in the (a) optical domain, (b) electrical domain.

When the incoming signal is split in the optical domain, it is possible to design each PMD channel specifically to match the signaling speed, offering optimum sensitivity for both 1 Gb/s and 10 Gb/s signals. However, the additional 1:2 optical splitter presented in Figure 91–9(a) will degrade the sensitivity of the PMD by introducing additional loss and lowering the power of the optical signal. Such a sensitivity reduction may be tolerable in the PX10/PR10/PRX10 type PMDs, but the more stringent power budgets including PX20, PR20, PRX20, PR30 and PRX30 may be very challenging or even impossible to implement with such an additional loss on the OLT receiver side. This particular problem may be resolved via an additional, low–gain optical amplifier introduced in–line with the 1:2 optical splitter, as presented in Figure 91–9(a), used to boost the power level of the incoming signal sufficiently to overcome the loss introduced by the 1:2 optical splitter.

When the incoming signal is split in the electrical domain, only one photodetector and one TIA units are used. The resulting optical sensitivity theoretically can be maintained without the need for optical amplification, reducing the complexity of the OLT receiver. However, the photodetector and TIA must cope with both data rates in quick succession, switching between 1 Gb/s and 10 Gb/s bursts during the guardband. The key aspect here is that the detector–TIA bandwidth directly affects the sensitivity. If the circuit parameters of the detector–TIA can be rapidly adapted to the correct value, optimum sensitivity can be maintained. There are three implementation choices in this regard, as shown in Figure 91–10(a)–(c):

a) This design fixes the detector parameters at some predefined value, resulting in the reduction of the OLT receiver sensitivity by approximately 2 dB. However, it should be noted that this penalty can be divided in such a way that both 1 Gb/s and 10 Gb/s sensitivities are 1 dB lower than their ideal values.
b) This design fixes the APD bias, but switches the TIA transimpedance depending on the target signaling speed for the given incoming burst, resulting in the reduction of the receiver sensitivity by approximately 1 dB. The said sensitivity penalty could be subdivided to both data rate channels by setting the APD bias to a compromise value.

c) This design switches both the APD bias and the TIA transimpedance depending on the signaling speed of the incoming burst. This results in ideal performance at both 1 Gb/s and 10 Gb/s data rates. However, it is the most complex design in terms of the number of elements and the control complexity, and it is unclear if the benefits outweigh the costs.

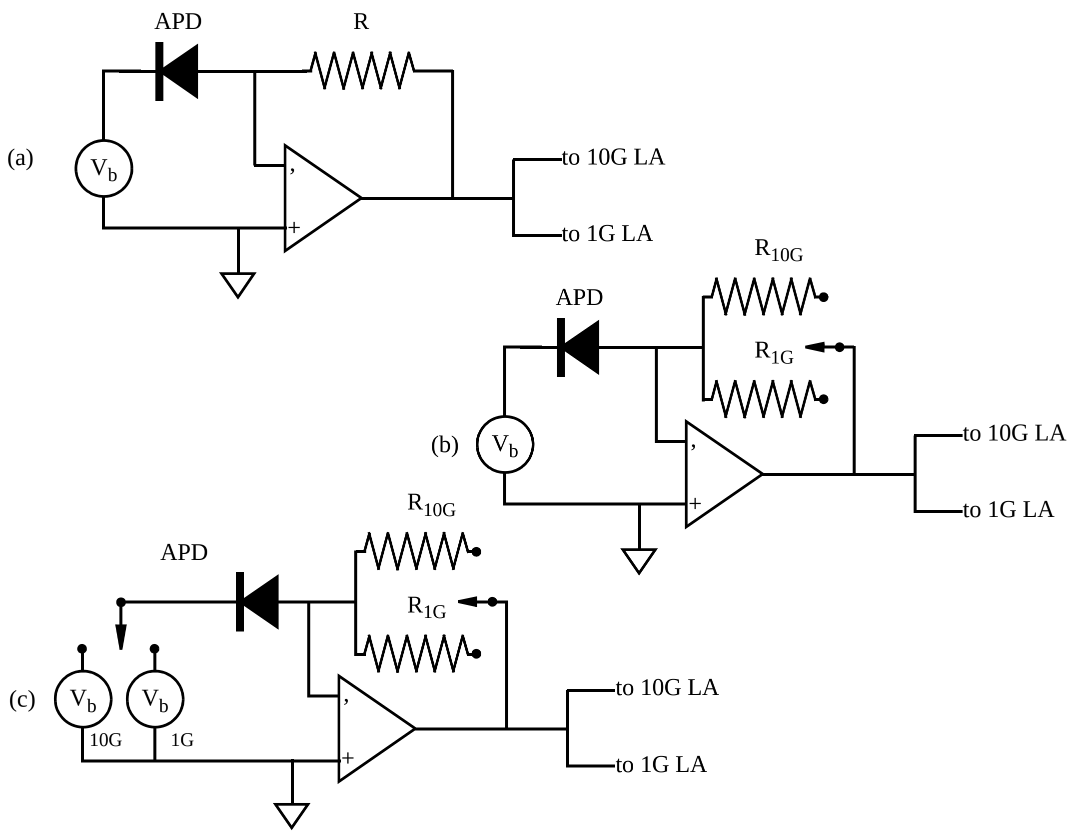


Figure 91–10—Dual rate APD–TIA architectures: (a) static, (b) half–dynamic, (c) fully–dynamic

In the case of dynamic detector designs, it is necessary to determine the data rate of the incoming burst before adjusting the dynamic detector to match the target data rate.

In general, the PMD layer does not have the a–priori knowledge of which data rate will be used in the given burst – such information is available only at the MAC Client level and its delivery to the PMD layer would violate the stack layering restrictions. Therefore, some sort of data rate detector circuit must be utilized. One of the simple methods is based on measuring the spectral energy content of the received signal at frequencies well above 1.25 GHz (e.g., in the range of 2 – 10 GHz). The 1 Gb/s signal has very little energy at said frequency range, while the 10 Gb/s signal has ample energy there. Thus, the presence of 5 GHz energy indicates that a 10 Gb/s signal is incident. Other implementation specific methods to control the APD–TIA speed are also possible, though are not discussed in this document.

In the dual–rate PMD topologies with the split in the electrical domain, 10 Gb/s detector and TIA are being implemented for receiving both 1 Gb/s and 10 Gb/s signals. Therefore, damage threshold (max) of the 1/10 Gb/s dual–rate receiver shall comply with the 10 Gb/s receiver specification in Table 91–6, even when receiving 1 Gb/s signal. Those values for 1000BASE–PX10–D and 1000BASE–PX20–D in @@Table 60–5@@ and @@Table 60–8@@, and also those of 10/1GBASE–PRX–D1 and 10/1GBASE–PRX–D2 in Table 91–7 cannot be applied for dual–rate OLT receiver.

91.8 Jitter at TP1–TP8 for PR10, PR20, PR30, PRX10, PRX20, PRX30 (informative)

The entries in Table 91–14 and Table 91–15 represent high frequency jitter above 4 MHz and those in Table 91–16 relate to jitter frequencies above 637 kHz. For PR10, PR20, PR30 upstream jitter transfer function is defined by Equation 91–1. The gain curve and corresponding gain values are shown in Figure 91–11 and Table 91–17. For PRX10, PRX20, PRX30 jitter transfer function, gain curve and gain values are shown in Equation 91–1, Figure 91–12, and Table 91–18 respectively.

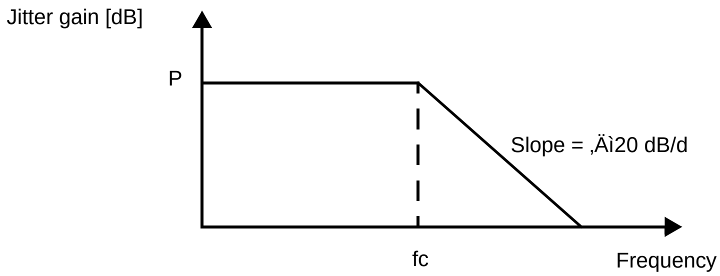


Figure 91–11—Jitter gain curve values for PR10, PR20 and PR30

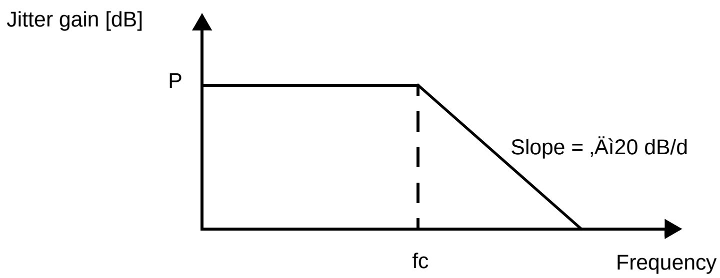


Figure 91–12—Jitter gain curve values for PRX10, PRX20 and PRX30

Table 91–14—PR10, PR20, PR30, PRX10, PRX20, PRX30 downstream jitter budgets (informative)[a]

Reference point	Total jitter	
	UI	ps
TP1	0.25	24
TP2	0.35	34
TP3	0.55	53
TP4	0.70	68

[a]NOTES:
These are preliminary jitter values based on simulations @ BER = 10^{-12} and need to be finalized.
All jitter values relate to high frequency (>4 MHz) jitter.
0.1 UI of sinusoidal jitter stress is assumed at the receiver.
The Gaussian jitter is assumed to be weak function of BER.
In downstream external modulator is assumed.

Table 91–15—PR10, PR20, PR30 upstream jitter budgets (informative)[a]

Reference point	Total jitter	
	UI	ps
TP5	0.25	24
TP6	0.40	39
TP7	0.50	48
TP8	0.70	68

[a]NOTES:
These are preliminary jitter values based on simulations @ BER = 10^{-12} and need to be finalized.
All jitter values relate to high frequency (>4 MHz) jitter.
0.1 UI of sinusoidal jitter stress is assumed at the receiver.
The Gaussian jitter is assumed to be weak function of BER.
In downstream external modulator is assumed.

Table 91–16—PRX10, PRX20, PRX30 upstream jitter budgets (informative)[a]

Reference point	Total jitter	
	UI	ps
TP1	0.24	192
TP2	0.40	320
TP3	0.49	392
TP4	0.67	536

[a]NOTES:
These numbers are reproduced from IEEE 802.3ah specifications @@Table 60–11@@ and may be revised if supported by new data.

Table 91–17—Jitter gain curve values for PR10, PR20 and PR30

	Value	Unit
P	0.3	dB
fc	8	MHz

$$\text{Jitter Transfer} = 20\log_{10}\left[\frac{\text{Jitter on upstream signal (UI)}}{\text{Jitter on downstream signal (UI)}} \times \frac{\text{downstream\_baudrate}}{\text{upstream\_baudrate}}\right] \quad (91\text{-}1)$$

91.9 Definitions of optical parameters and measurement methods

Table 91–18—Jitter gain curve values for PRX10, PRX20 and PRX30

	Value	Unit
P	0.3	dB
fc	1274	kHz

In measuring TP1 and TP5 it is recommended that jitter contributions at frequencies below receiver corner frequencies viz. 4 MHz for 10.3125 GBd receiver and 637 kHz for 1.25 GBd receiver are filtered at the measurement unit. The following sections describe definitive patterns and test procedures for certain PMDs of this standard. Implementers using alternative verification methods must ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods. All optical measurements, except TDP and $RIN_{15}OMA$ shall be made through a short patch cable between 2 and 5 m in length.

91.9.1 Insertion loss

Insertion loss for SMF fiber optic cabling (channel) is defined at 1270, 1310, 1577 or 1590 nm, depending on the particular PMD. A suitable test method is described in ITU–T G.650.1.

91.9.2 Allocation for penalties in 10G EPON PMDs

The Clause 91 receivers are required to tolerate a path penalty not exceeding 1 dB to account for total degradations due to reflections, intersymbol interference, mode partition noise, laser chirp and detuning of the central wavelength, including chromatic dispersion penalty. All the transmitter types specified in Clause 91 introduce less than 1 dB of optical path penalty over the PON plant. An increase in the optical path penalty is acceptable, provided that any increase in optical path penalty over 1 dB is compensated by an increase of the minimum transmitter OMA. The path penalty is a component of transmitter and dispersion penalty (TDP) which is specified in Table 91–5, Table 91–8, Table 91–9 and described in @@Subclause 58.7.9@@.

91.9.3 Test patterns

Compliance is to be achieved in normal operation. Two types of test patterns are used, square wave (@@Subclause 52.9.1.2@@) and other (@@Subclause 52.9.1.1@@) for testing of 10 Gb/s optical PMDs. These 10 Gb/s test patterns for 10GBASE–PR and 10/1GBASE–PRX are in Table 91–19. Two types of test frames are used, random and jitter (@@Subclause 59.7.1@@) for 1 Gb/s tests relevant to the 10/1GBASE–PRX PHY. All test patterns are listed in Table 91–19.

91.9.4 Wavelength and spectral width measurement

The center wavelength and spectral width (RMS) shall meet specifications according to ANSI/TIA/EIA–455–127 under modulated conditions using an appropriate PRBS or a valid 10GBASE–PR signal, 1000BASE–X signal, or another representative test pattern.

NOTE 1—The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

NOTE 2—The 20 dB width for SLM lasers is taken as 6.07 times the RMS width.

91.9.5 Optical power measurements

Optical power shall meet specifications according to the methods specified in ANSI/EIA–455–95. A measurement may be made with the port transmitting any valid encoded 8B/10B or 64B/66B data stream.

Table 91–19—Test patterns

Test	10 Gb/s Pattern[a]	1 Gb/s Pattern	Related Subclause
Average optical power	1 or 3	Valid 8B/10B	91.9.5
OMA (modulated optical power)	Square	Idles	91.9.7
Extinction ratio	1 or 3	Idles	91.9.6
Transmit eye	1 or 3	Valid 8B/10B	91.9.7
Receive upper cutoff frequency	1 or 3	Random frame	91.9.14
$RIN_{15}OMA$	Square	Idles	91.9.8
Wavelength, spectral width	1 or 3	Valid 8B/10B	91.9.4
Side mode suppression ratio	1 or 3	Valid 8B/10B	–
VECP calibration	2 or 3	Jitter frame	91.9.12
Receiver sensitivity	1 or 3	Random frame	91.9.11
Receiver overload	1 or 3	Valid 8B/10B	–
Stressed receive sensitivity	2 or 3	Random frame	91.9.12
Transmitter and dispersion penalty	2 or 3	Random frame	91.9.10
Jitter	2 or 3	Jitter frame	91.9.13
Laser On/Off	1 or 3	Valid 8B/10B	91.9.15
Receiver settling	1 or 3	Valid 8B/10B	91.9.16

[a]Individual 10 Gb/s test pattern are described in @@Subclause 52.9.1.2@@ for a square wave and @@Subclause 52.9.1.1@@ for test patterns, represented by numbers.

91.9.6 Extinction ratio measurements

Extinction ratio shall meet specifications according to IEC 61820–2–2 with the port transmitting a repeating idle pattern /I2/ ordered_set (see @@Subclause 36.2.4.12@@) or valid 10GBASE–PR signal that may be interspersed with OAM packets per @@Subclause 43.B.2@@, and with minimal back reflections into the transmitter, lower than –20dB. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

91.9.7 Optical modulation amplitude (OMA) test procedure

A description of OMA measurements for 1 Gb/s PHYs is found in @@Subclause 58.7.5@@. A description of OMA measurements for 10 Gb/s PHYs shall be compliant with the description found in @@Subclause 52.9.5@@.

91.9.8 Relative intensity noise optical modulation amplitude (RINxOMA) measuring procedure

This procedure describes a component test that may not be appropriate for a system level test depending on the implementation. If used, the procedure shall be performed as described in @@Subclause 52.9.6@@ for 10 Gb/s PHYs and in @@Subclause 58.7.7@@ for 1 Gb/s PHYs.

91.9.9 Transmit optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 91–13 and Figure 91–14.

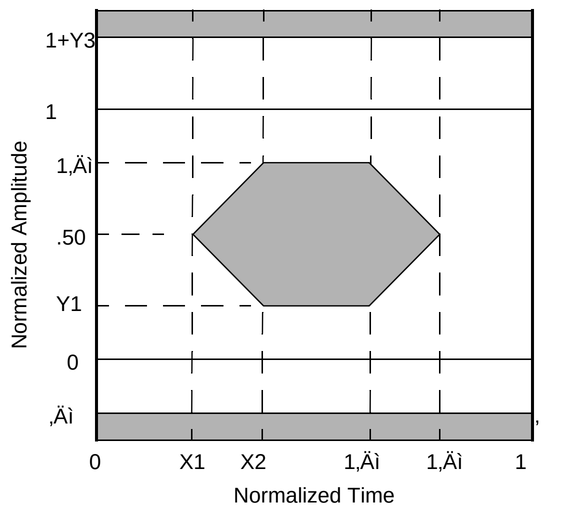


Figure 91–13—Transmitter eye mask definition

The measurement procedure is described in @@Subclause 58.7.8@@ for 1 Gb/s PHYs and @@Subclause 52.9.7@@ for 10 Gb/s PHYs and references therein. The eye shall comply to the mask of the eye using a fourth–order Bessel–Thomson receiver response with f_r = 0.75 * bitRate, and where the relative response vs. relative frequency is defined in ITU–T G.957, Table B.2 (STM–16 values), along with the allowed tolerances for its physical implementation.

NOTE 1—This Bessel–Thomson filter is not intended to represent the noise filter within an optical receiver, but is intended to provide uniform measurement conditions on the transmitter.

NOTE 2—The fourth order Bessel–Thomson filter is reactive. In order to suppress reflections, an attenuator may be required at the filter input and/or output.

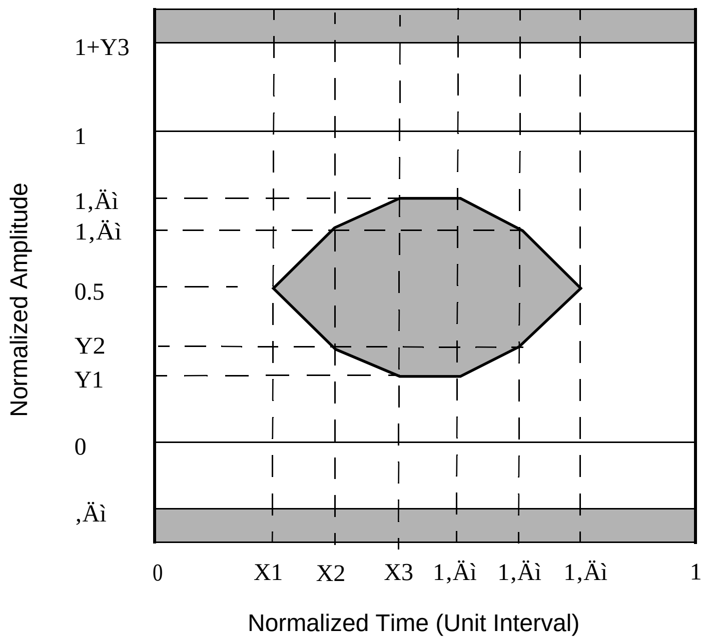


Figure 91–14—Transmitter eye mask definition

91.9.10 Transmitter and dispersion penalty (TDP)

TDP measurement tests for transmitter impairments with chromatic effects for a transmitter to be used with single–mode fiber. Possible causes of impairment include intersymbol interference, jitter, and RIN. Meeting the separate requirements (e.g. eye mask, spectral characteristics) does not in itself guarantee the transmitter and dispersion penalty (TDP). The TDP limit shall be met. See @@Subclause 58.7.9@@ for details of the measurement for 1 Gb/s PHYs and @@Subclause 52.9.10@@ for 10 Gb/s PHYs.

91.9.11 Receive sensitivity

Receiver sensitivity is defined for the random pattern test frame, or test pattern 1, or test pattern 3, and an ideal input signal quality with the specified extinction ratio. The measurement procedure is described in @@Subclause 58.7.10@@ for 1 Gb/s PHYs and @@Subclause 52.9.8@@ for 10 Gb/s PHYs. The sensitivity shall be met for the bit error ratio defined in Table 91–6, Table 91–7, and Table 91–11 as appropriate.

91.9.12 Stressed receiver conformance test

The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics which could cause errors when combined with a distorted but compliant signal. If stressed receiver compliance is necessary, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 91–6, Table 91–7, and Table 91–11 as appropriate, according to the measurement procedures of @@Subclause 58.7.11@@ for 1 Gb/s PHYs and @@Subclause 52.9.9@@ for 10 Gb/s PHYs.

91.9.13 Jitter measurements

Jitter measurements for 1 Gb/s are described in @@Subclause 58.7.12@@. Jitter measurements for 10 Gb/s are described in @@Subclause 52.8.1@@.

91.9.14 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency may be measured as described in @@Subclause 52.9.11@@.

91.9.15 Laser On/Off timing measurement

Laser On/Off timing measurement procedure is described in @@Subclause 60.7.13.1@@ with the following changes:

a) T_{on} is defined in @@Subclause 60.7.13.1.1@@, value is less than 512 ns (defined in Table 91–8 and Table 91–9).
b) $T_{receiver\_settling}$ is defined in @@Subclause 60.8.13.2.1@@ (informative) value is defined in Table 91–6 and Table 91–7.
c) T_{cdr} is defined in @@Subclause 92.3.2.1@@, value less than 400 ns.
d) $T_{code\_group\_align}$ is defined in @@Subclause 36.6.2.4@@ value is less than 4 ten–bit code–groups for 1 Gb/s PHYs, and is defined as 0 for 10 Gb/s PHYs.
e) T_{off} is defined in @@Subclause 60.7.13.11.1@@, value is less than 512 ns (defined in Table 91–8 and Table 91–9).

91.9.16 Receiver settling timing measurement (informative)

The receiver settling time measurement is described in @@Subclause 60.7.13.2@@.

91.10 Environmental, safety, and labeling

91.10.1 Safety

The 10GBASE–PR and 10/1GBASE–PRX environmental specifications are as defined in @@Subclause 52.10.1@@ for general safety, and as defined in @@Subclause 52.10.2@@ for laser safety.

91.10.2 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

91.10.3 Environment

The 10GBASE–PR and 10/1GBASE–PRX operating environment specifications are as defined in @@Subclause 52.11@@, as defined in @@Subclause 52.11.1@@ for electromagnetic emission, and as defined in @@Subclause 52.11.2@@ for temperature, humidity, and handling.

Reference @@Annex 67A@@ for additional environmental information. Two optional temperature ranges are defined in @@Table 60–13@@. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

91.10.4 PMD labeling

The 10GBASE–PR and 10/1GBASE–PRX labeling recommendations and requirements are as defined in @@Subclause 52.12@@.

Defined PMDs are: 10/1GBASE–PRX–D1, 10/1GBASE–PRX–D2, 10/1GBASE–PRX–D3, 10GBASE–PR–D1, 10GBASE–PR–D2, 10GBASE–PR–D3, 10/1GBASE–PRX–U1, 10/1GBASEPRX–U2, 10/1GBASE–PRX–U3, 10GBASE–PR–U1 and 10GBASE–PR–U3.

91.11 Characteristics of the fiber optic cabling

The 10GBASE–PR and 10/1GBASE–PRX fiber optic cabling shall meet the dispersion specifications defined in IEC 60793–2 and ITU–T G.652, as shown in Table 91–20. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 91–3 and Figure 91–4.

91.11.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 91–3 and Figure 91–4.

NOTE—The optical splitter presented in Figure 91–3 and Figure 91–4 may be replaced by a number of smaller 1:n splitters such that a different topology may be implemented while preserving the link characteristics and power budget as defined in Table 91–12 and Table 91–13.

The maximum channel insertion losses shall meet the requirements specified in Table 91–1. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA–526–7 [B15], method A–1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

91.11.2 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793–2 Type B1.1 (dispersion un–shifted SMF) and Type B1.3 (low water peak SMF) and ITU G.652 as noted in Table 91–20.

91.11.3 Optical fiber connection

Table 91–20—Optical fiber and cable characteristics

Description[a]	Type B1.1, B1.3 SMF					Unit
Nominal wavelength[b]	1270	1310	1550	1577	1590	nm
Cable attenuation (max)[c]	0.44	0.4	0.35	0.35	0.36	dB/km
Zero dispersion wavelength[d]	$1300 \le \lambda_0 \le 1324$					nm
Dispersion slope (max)	0.093					$ps / nm^2 \cdot km$

[a]The fiber dispersion values are normative, all other values in the table are informative.
[b]Wavelength specified is the nominal wavelength and typical measurement wavelength. Power penalties at other wavelengths are accounted for.
[c]Attenuation for single–mode optical fiber cables for 1310 nm and 1550 nm is defined in ITU–T G.652. The attenuation in the 1270 nm, 1577 nm and 1590 nm windows was calculated using spectral attenuation modelling method (5.4.4) included in G.650.1 (06/2004) and the matrix coefficients included in Appendix III herein. 1310 nm (0.4 dB/km), 1380 nm (0.5 dB/km) and 1550 nm (0.35 dB/km) attenuation values were used as the input for the predictor model.
[d]See IEC 60793 or ITU–T G.652.

An optical fiber connection as shown in Figure 91–3 and Figure 91–4 consists of a mated pair of optical connectors. The 10GBASE–PR or 10/1GBASE–PRX PMD is coupled to the fiber optic cabling through an optical connection and any optical splitters into the MDI optical receiver, as shown in Figure 91–3. The channel insertion loss includes the loss for connectors, splices and other passive components such as splitters, see Table 91–12 and Table 91–13.

The channel insertion loss was calculated under the assumption of 14.5 dB loss for a 1:16 splitter / 18.1 dB loss for a 1:32 splitter (G.671 am 1). Unitary fiber attenuation for particular transmission wavelength is provided in Table 91–20. The number of splices / connectors is not predefined – the number of individual fiber sections between the OLT MDI and the ONU MDI is not defined. The only requirement is that the resulting channel insertion loss is within the limits specified in Table 91–1. Other fiber arrangements (i.e. increasing the split ratio while decreasing the fiber length or vice versa) are supported as long as the limits for the channel insertion loss specified in Table 91–1 are observed.

The maximum discrete reflectance for single–mode connections shall be less than –26 dB.

91.11.4 Medium Dependent Interface (MDI)

The 10GBASE–PR or 10/1GBASE–PRX PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” as shown in Figure 91–3 and Figure 91–4. Examples of an MDI include:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a remateable connection, it shall meet the interface performance specifications of IEC 61753–1. The MDI carries the signal in both directions for 10GBASE–PR or 10/1GBASE–PRX PMD and couples to a single fiber.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in Subclause 91.3.2, not at the MDI.

91.12 Protocol implementation conformance statement (PICS) proforma for Clause 91, Physical Medium Dependent (PMD) sublayer and medium, type 10GBASE–PR (symmetric 10 Gb/s long wavelength passive optical networks) and 10/1GBASE–PRX (asymmetric 10 Gb/s downstream, 1 Gb/s upstream long wavelength passive optical networks)[a]

91.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 91, Physical Medium Dependent (PMD) sublayer and medium, type 10GBASE–PR (symmetric 10 Gb/s long wavelength passive optical networks) and 10/1GBASE–PRX (asymmetric 10 Gb/s downstream, 1 Gb/s upstream long wavelength passive optical networks), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in @@Clause 21@@.

91.12.2 Identification

91.12.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

[a]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this Subclause so that it can be used for its intended purpose and may further publish the completed PICS.

91.12.2.2 Protocol Summary

Identification of protocol standard	IEEE Std 802.3–2005, Clause 91, Physical Medium Dependent (PMD) sublayer and medium, type 10GBASE–PR (symmetric 10 Gb/s long wavelength passive optical networks) and 10/1GBASE–PRX (asymmetric 10 Gb/s downstream, 1 Gb/s upstream long wavelength passive optical networks)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?	No [ ] Yes [ ]
(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3–2008.)	

Date of Statement	

91.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DTX	Transmit delay	91.3.1.1	Constant delay of 4 TQ (max)	M	Yes [ ]
DRX	Receive delay	91.3.1.1	Constant delay of 4 TQ (max)	M	Yes [ ]
HT	High temperature operation	91.10.3	–5 to 85 ºC	O	Yes [ ] No [ ]
LT	Low temperature operation	91.10.3	–40 to 60 ºC	O	Yes [ ] No [ ]
*PR10U	10GBASE–PR–D1 or 10GBASE–PR–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PR10D	10GBASE–PR–D1 or 10GBASE–PR–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PR20U	10GBASE–PR–D2 or 10GBASE–PR–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PR20D	10GBASE–PR–D2 or 10GBASE–PR–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PR30U	10GBASE–PR–D3 or 10GBASE–PR–U3 PMD	91.4, 91.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PR30D	10GBASE–PR–D3 or 10GBASE–PR–U3 PMD	91.4, 91.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PRX10U	10/1GBASE–PRX–D1 or 10/1GBASE–PRX–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PRX10D	10/1GBASE–PRX–D1 or 10/1GBASE–PRX–U1 PMD	91.4, 91.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PRX20U	10/1GBASE–PRX–D2 or 10/1GBASE–PRX–U2 PMD	91.4, 91.5	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PRX20D	10/1GBASE–PRX–D2 or 10/1GBASE–PRX–U2 PMD	91.4, 91.5	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PRX30U	10/1GBASE–PRX–D3 or 10/1GBASE–PRX–U3 PMD	91.4, 91.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PRX30D	10/1GBASE–PRX–D3 or 10/1GBASE–PRX–U3 PMD	91.4, 91.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*INS	Installation / Cable	91.4.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufac-turer.	O	Yes [ ] No [ ]

91.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 10GBASE–PR (symmetric 10 Gb/s long wavelength passive optical networks) and 10/1GBASE–PRX (asymmetric 10 Gb/s downstream, 1 Gb/s upstream long wavelength passive optical networks)

91.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	91.3.3	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	91.3.3	Higher optical power transmitted is a logic 1	M	Yes [ ]
FN3	Receive function	91.3.4	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	91.3.4	Higher optical power received is a logic 1	M	Yes [ ]
FN5	Signal detect function	91.3.5.1	Mapping to PMD service interface	M	Yes [ ]
FN6	Signal detect parameter	91.3.5.1	Generated according to Table 91–4	M	Yes [ ]
FN7	Signal detect function	91.3.5.2	Mapping to PMD service interface	O/2	Yes [ ]
FN7	Signal detect function	91.3.5.2	Provided by higher layer	O/2	Yes [ ]
FN8	Signal detect parameter	91.3.5.1	Generated according to Table 91–4	O	Yes [ ]

91.12.4.2 PMD to MDI optical specifications for 10GBASE–PR–D1

Item	Feature	Subclause	Value/Comment	Status	Support
PRD1F1	10GBASE–PR–D1 transmitter	91.4.1	Meets specifications in Table 91–5	PRD1F1:M	Yes [ ] N/A [ ]
PRD1F2	10GBASE–PR–D1 receiver	91.4.2	Meets specifications in Table 91–6	PRD1F2:M	Yes [ ] N/A [ ]
PRD1F3	10GBASE–PR–D1 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–6	PRD1F3:O	Yes [ ] No [ ] N/A[ ]
PRD1F4	10GBASE–PR–D1 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–6 then label accordingly	PRD1F4:M	Yes [ ] N/A [ ]

91.12.4.3 PMD to MDI optical specifications for 10GBASE–PR–D2

Item	Feature	Subclause	Value/Comment	Status	Support
PRD2F1	10GBASE–PR–D2 transmitter	91.4.1	Meets specifications in Table 91–5	PRD2F1:M	Yes [ ] N/A [ ]
PRD2F2	10GBASE–PR–D2 receiver	91.4.2	Meets specifications in Table 91–6	PRD2F2:M	Yes [ ] N/A [ ]
PRD2F3	10GBASE–PR–D2 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–6	PRD2F3:O	Yes [ ] No [ ] N/A[ ]
PRD2F4	10GBASE–PR–D2 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–6 then label accordingly	PRD2F4:M	Yes [ ] N/A [ ]

91.12.4.4 PMD to MDI optical specifications for 10GBASE–PR–D3

Item	Feature	Subclause	Value/Comment	Status	Support
PRD3F1	10GBASE–PR–D3 transmitter	91.4.1	Meets specifications in Table 91–5	PRD3F1:M	Yes [ ] N/A [ ]
PRD3F2	10GBASE–PR–D3 receiver	91.4.2	Meets specifications in Table 91–6	PRD3F2:M	Yes [ ] N/A [ ]
PRD3F3	10GBASE–PR–D3 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–6	PRD3F3:O	Yes [ ] No [ ] N/A[ ]
PRD3F4	10GBASE–PR–D3 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–6 then label accordingly	PRD3F4:M	Yes [ ] N/A [ ]

91.12.4.5 PMD to MDI optical specifications for 10/1GBASE–PRX–D1

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD1F1	10/1GBASE–PXR–D1 transmitter	91.4.1	Meets specifications in Table 91–5	PRXD1F1:M	Yes [ ] N/A [ ]
PRXD1F2	10/1GBASE–PRX–D1 receiver	91.4.2	Meets specifications in Table 91–7	PRXD1F2:M	Yes [ ] N/A [ ]
PRXD1F3	10/1GBASE–PRX–D1 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–7	PRXD1F3:O	Yes [ ] No [ ] N/A[ ]
PRXD1F4	10/1GBASE–PRX–D1 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–7 then label accordingly	PRXD1F4:M	Yes [ ] N/A [ ]

91.12.4.6 PMD to MDI optical specifications for 10/1GBASE–PRX–D2

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD2F1	10/1GBASE–PXR–D2 transmitter	91.4.1	Meets specifications in Table 91–5	PRXD2F1:M	Yes [ ] N/A [ ]
PRXD2F2	10/1GBASE–PRX–D2 receiver	91.4.2	Meets specifications in Table 91–7	PRXD2F2:M	Yes [ ] N/A [ ]
PRXD2F3	10/1GBASE–PRX–D2 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–7	PRXD2F3:O	Yes [ ] No [ ] N/A[ ]
PRXD2F4	10/1GBASE–PRX–D2 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–7 then label accordingly	PRXD2F4:M	Yes [ ] N/A [ ]

91.12.4.7 PMD to MDI optical specifications for 10/1GBASE–PRX–D3

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD3F1	10/1GBASE–PXR–D3 transmitter	91.4.1	Meets specifications in Table 91–5	PRXD3F1:M	Yes [ ] N/A [ ]
PRXD3F2	10/1GBASE–PRX–D3 receiver	91.4.2	Meets specifications in Table 91–7	PRXD3F2:M	Yes [ ] N/A [ ]
PRXD3F3	10/1GBASE–PRX–D3 stressed receiver sensitivity	91.4.2	Meets specifications in Table 91–7	PRXD3F3:O	Yes [ ] No [ ] N/A[ ]
PRXD3F4	10/1GBASE–PRX–D3 receiver damage threshold	91.4.2	If the receiver does not meet the damage requirements in Table 91–7 then label accordingly	PRXD3F4:M	Yes [ ] N/A [ ]

91.12.4.8 PMD to MDI optical specifications for 10GBASE–PR–U1

Item	Feature	Subclause	Value/Comment	Status	Support
PRU1F1	10GBASE–PR–U1 transmitter	91.5.1	Meets specifications in Table 91–8	PRU1F1:M	Yes [ ] N/A [ ]
PRU1F2	10GBASE–PR–U1 receiver	91.5.2	Meets specifications in Table 91–11	PRU1F2:M	Yes [ ] N/A [ ]
PRU1F3	10GBASE–PR–U1 stressed receiver sensitivity	91.5.2	Meets specifications in Table 91–11	PRU1F3:O	Yes [ ] No [ ] N/A[ ]
PRU1F4	10GBASE–PR–U1 receiver damage threshold	91.5.2	If the receiver does not meet the damage requirements in Table 91–11 then label accordingly	PRU1F4:M	Yes [ ] N/A [ ]

91.12.4.9 PMD to MDI optical specifications for 10GBASE–PR–U3

Item	Feature	Subclause	Value/Comment	Status	Support
PRU3F1	10GBASE–PR–U3 transmitter	91.5.1	Meets specifications in Table 91–8	PRU3F1:M	Yes [ ] N/A [ ]
PRU3F2	10GBASE–PR–U3 receiver	91.5.2	Meets specifications in Table 91–11	PRU3F2:M	Yes [ ] N/A [ ]
PRU3F3	10GBASE–PR–U3 stressed receiver sensitivity	91.5.2	Meets specifications in Table 91–11	PRU3F3:O	Yes [ ] No [ ] N/A[ ]
PRU3F4	10GBASE–PR–U3 receiver damage threshold	91.5.2	If the receiver does not meet the damage requirements in Table 91–11 then label accordingly	PRU3F4:M	Yes [ ] N/A [ ]

91.12.4.10 PMD to MDI optical specifications for 10/1GBASE–PRX–U1

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU1F1	10/1GBASE–PRX–U1 transmitter	91.5.1	Meets specifications in Table 91–9	PRXU1F1:M	Yes [ ] N/A [ ]
PRXU1F2	10/1GBASE–PRX–U1 receiver	91.5.2	Meets specifications in Table 91–11	PRXU1F2:M	Yes [ ] N/A [ ]
PRXU1F3	10/1GBASE–PRX–U1 stressed receiver sensitivity	91.5.2	Meets specifications in Table 91–11	PRXU1F3:O	Yes [ ] No [ ] N/A[ ]
PRXU1F4	10/1GBASE–PRX–U1 receiver damage threshold	91.5.2	If the receiver does not meet the damage requirements in Table 91–11 then label accordingly	PRXU1F4:M	Yes [ ] N/A [ ]

91.12.4.11 PMD to MDI optical specifications for 10/1GBASE–PRX–U2

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU2F1	10/1GBASE–PRX–U2 transmitter	91.5.1	Meets specifications in Table 91–9	PRXU2F1:M	Yes [ ] N/A [ ]
PRXU2F2	10/1GBASE–PRX–U2 receiver	91.5.2	Meets specifications in Table 91–11	PRXU2F2:M	Yes [ ] N/A [ ]
PRXU2F3	10/1GBASE–PRX–U2 stressed receiver sensitivity	91.5.2	Meets specifications in Table 91–11	PRXU2F3:O	Yes [ ] No [ ] N/A[ ]
PRXU2F4	10/1GBASE–PRX–U2 receiver damage threshold	91.5.2	If the receiver does not meet the damage requirements in Table 91–11 then label accordingly	PRXU2F4:M	Yes [ ] N/A [ ]

91.12.4.12 PMD to MDI optical specifications for 10/1GBASE–PRX–U3

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU3F1	10/1GBASE–PRX–U3 transmitter	91.5.1	Meets specifications in Table 91–9	PRXU3F1:M	Yes [ ] N/A [ ]
PRXU3F2	10/1GBASE–PRX–U3 receiver	91.5.2	Meets specifications in Table 91–11	PRXU3F2:M	Yes [ ] N/A [ ]
PRXU3F3	10/1GBASE–PRX–U3 stressed receiver sensitivity	91.5.2	Meets specifications in Table 91–11	PRXU3F3:O	Yes [ ] No [ ] N/A[ ]
PRXU3F4	10/1GBASE–PRX–U3 receiver damage threshold	91.5.2	If the receiver does not meet the damage requirements in Table 91–11 then label accordingly	PRXU3F4:M	Yes [ ] N/A [ ]

91.12.4.13 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	91.9.1	2 m to 5 meters in length	M	Yes [ ]
OM2	Wavelength and spectral width measurement	91.9.4	Per TIA/EIA–455–127 under modulated conditions	M	Yes [ ]
OM3	Average optical power	91.9.5	Per TIA/EIA–455–95	M	Yes [ ]
OM4	Extinction ratio	91.9.6	Per ANSI/TIA/EIA–526–4A with minimal back reflections and fourth–order Bessel–Thomson receiver	M	Yes [ ]
OM5	Optical modulation amplitude (OMA) test procedure	91.9.7	As described in @@Subclause 58.7.5@@ for 1 Gb/s PHY and in @@Subclause 52.956@@ for 10 Gb/s PHY.	M	Yes [ ]
OM6	RIN_xOMA	91.9.8	As described in @@Subclause 58.8.7@@	M	Yes [ ]
OM7	Transmit optical waveform (transmit eye)	91.9.9	Per ANSI/TIA/EIA–526–4A with test pattern and fourth–order Bessel–Thomson receiver	M	Yes [ ]
OM8	Transmitter and dispersion penalty measurements	91.9.10	As described in @@Subclause 58.7.7@@ for 1 Gb/s PHY and in @@Subclause 52.9.6@@ for 10 Gb/s PHY.	M	Yes [ ]
OM9	Receive sensitivity	91.9.11	As described in @@Subclause 58.7.10@@ for 1 Gb/s PHY and in @@Subclause 52.9.8@@ for 10 Gb/s PHY. Values defined in Table 91–6, Table 91–7, and Table 91–11 as appropriate.	M	Yes [ ]
*OM10	Stressed receiver conformance test	91.9.12	As described in @@Subclause 58.7.11@@ for 1 Gb/s PHY and in @@Subclause 52.9.9@@ for 10 Gb/s PHY. Values defined in Table 91–6, Table 91–7, and Table 91–11 as appropriate.	O	Yes[ ] N/A[ ]
OM11	Jitter measurements	91.9.13	As described in @@Subclause 58.7.12@@ for 1 Gb/s PHY and in @@Subclause 52.8.1@@ for 10 Gb/s PHY.	M	Yes [ ]
OM12	Measurement of the receiver 3 dB electrical upper cutoff frequency	91.9.14	As described in @@Subclause 52.9.11@@ for 10 Gb/s PHY. Optional for 1 Gb/s PHY.	M	Yes [ ]
OM13	Laser On/Off timing measurement	91.9.15	As described in @@Subclause 60.7.13.1@@ for 1 Gb/s PHY and in @@Subclause 60.7.13.1@@ with modifications defined in Subclause 91.9.15 for 10 Gb/s PHY.	M	Yes [ ]
OM14	Receiver settling timing measurement	91.9.16	As described in @@Subclause 60.7.13.2@@ for 1 Gb/s and 10 Gb/s PHY.	O	Yes [ ] No [ ]

91.12.4.14 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	91.11	Specified in Table 91–20	INS:M	Yes [ ] N/A[ ]
F02	End –to–end channel loss	91.11	Meeting the requirements of Table 91–12 and Table 91–13	INS:M	Yes [ ] N/A[ ]
FO3	Maximum discrete reflectance – single–mode fiber	91.11.3	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO4	MDI requirements	91.11.4	Meet the interface performance specifications of IEC 61753–1, if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

91.12.4.15 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	91.10.1	Conforms to IEC–60950	M	Yes [ ]
ES2	Laser safety —IEC Class 1	91.10.1	Conform to Class 1 laser requirements defined in IEC 60825–1	M	Yes [ ]
ES3	Documentation	91.10.1	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range labeling	91.10.4	If required	M	Yes [ ] N/A[ ]

92. Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point-to-multipoint media, types 10GBASE-PR and 10/1GBASE-PRX

Editors' Note 92-1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

:

Editors' Note 92-2 (to be removed prior to release): Draft revision history for Clause 92

Version	*Date*	*Comments*
D0.8	*Jul 2007*	*Preliminary draft outline for IEEE P802.3av Task Force review.*
D0.9	*Sep 2007*	*Preliminary draft for IEEE P802.3av Task Force review.*
D1.0	*Nov 2007*	*Initial draft for IEEE P802.3av Task Force comments.*
D1.1	*Jan 2008*	*Draft for Task Force review with comment resolution from January 2008 meeting.*
D1.2	*Apr 2008*	*Draft for Task Force review with comment resolution from March 2008 meeting.*
D1.3	*May 2008*	*Draft for Task Force review with comment resolution from April 2008 meeting.*
D1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting.*

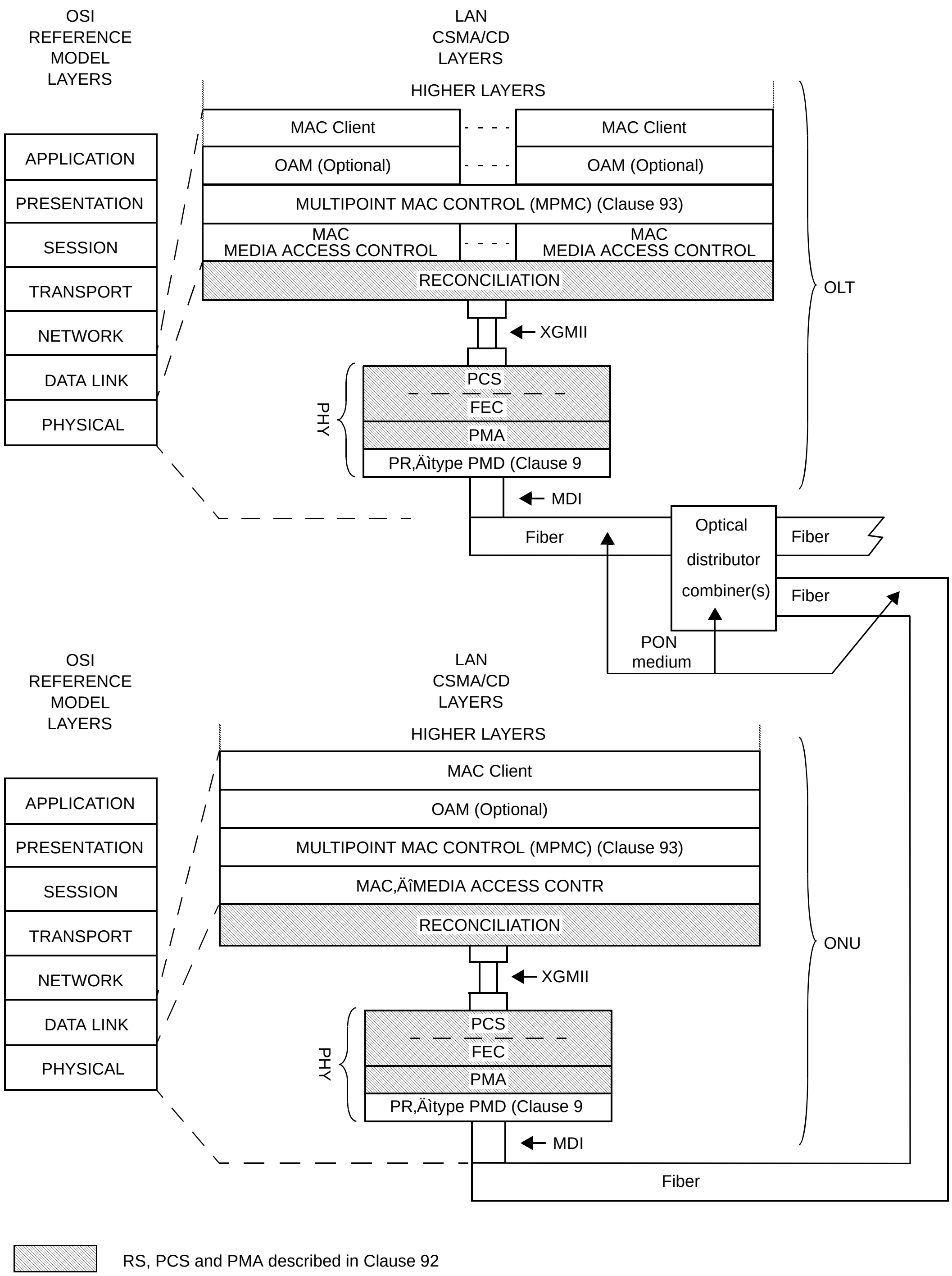
External cross references are marked with double "@" signs (for example @@1.1.1@@). These will be converted to hyper links in a later draft.

This Clause describes the Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS) / Physical Media Attachment (PMA) used with 10GBASE-PR and 10/1GBASE-PRX point-to-multipoint (P2MP) networks. These are passive optical multipoint networks (PONs) that connect multiple DTEs using a single shared fiber. The architecture is asymmetrical, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 93.

92.1 Reconciliation Sublayer (RS)

92.1.1 Overview

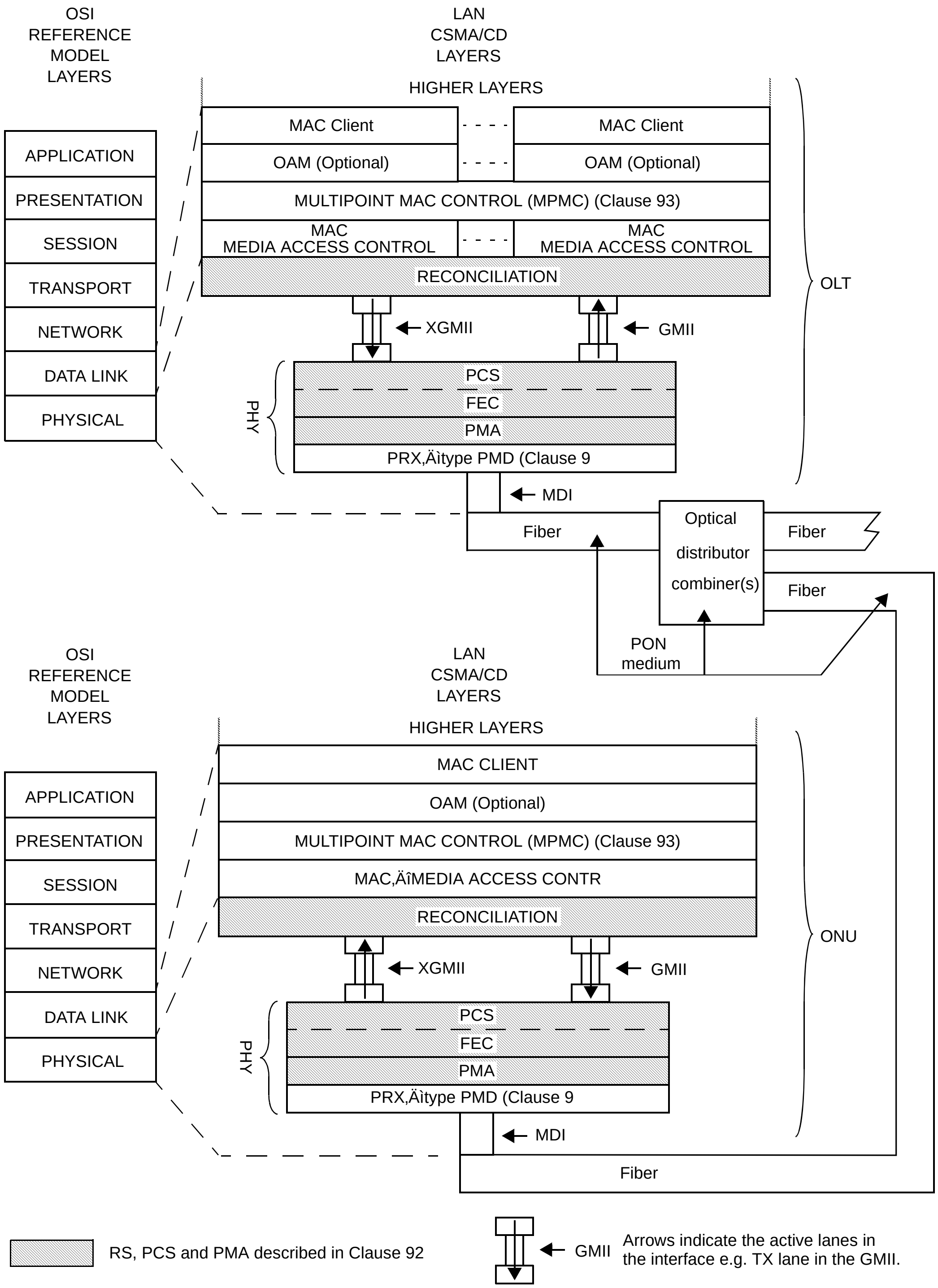
This Subclause extends Clause 46 to enable multiple data link layers to interface with a single physical layer and Clause 65 to enable asymmetrical data links, transmitting at one data rate (e.g. 10 Gb/s) and receive in another data rate (e.g. 1 Gb/s). The number of MACs supported is limited only by the implementation. It is acceptable for only one MAC to be connected to this Reconciliation Sublayer. Figure 92–1 and Figure 92–2 show the relationship between this RS to the ISO/IEC OSI reference model. The mapping of GMII/XGMII signals to PLS service primitives is described in Subclause @@35.2.1@@ for GMII and @@46.1.7@@ for XGMII with exceptions noted herein.



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 92–1—Relationship of 10 Gb/s symmetric P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN model



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 92–2—Relationship of 10/1 Gb/s asymmetric P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN model.

92.1.2 Dual-speed Media Independent Interface

In legacy EPON architectures, the GMII is the interface used to bridge between the MAC and the PHY. For symmetric 10 Gb/s EPON architectures, the XGMII is the interface used to bridge between the MAC and the PHY. When using an asymmetric EPON architecture, a combination of both GMII and XGMII is needed in order to support transmission and reception at different speeds. Through the parallel use of the GMII and XGMII, the following modes are supported:

- symmetric 10 Gb/s operation for transmit and receive data paths, providing all of the functionality of the XGMII defined in Clause 46.
- symmetric 1 Gb/s operation for transmit and receive data paths, providing all of the functionality of the GMII defined in Clause 35.
- asymmetric operation for transmit and receive data paths at the OLT, providing transmit path functionality of the XGMII defined in Clause 46 and receive path functionality of the GMII defined in Clause 35.
- asymmetric operation for transmit and receive data paths at the ONU, providing transmit path functionality of the GMII defined in Clause 35 and receive path functionality of the XGMII defined in Clause 46.
- coexistence of various ONU types by utilizing different data paths within the OLT.

92.1.2.1 Symmetric mode

Symmetric mode supports transmit and receive data paths operating at 10 Gb/s. When operating in symmetric mode, the XGMII transmit and receive data paths are used for both transmission and reception. Figure 92–3(a) depicts the operation of the symmetric mode.

92.1.2.2 Asymmetric mode

Asymmetric mode supports transmit and receive data paths operating at different line rates. When operating in asymmetric mode, a combination of XGMII and GMII data paths is used for transmission and reception.

At the OLT, the transmit path uses XGMII signals TXD<31:0>, TXC<3:0> and TX_CLK, while the receive path uses GMII signals RXD<7:0>, RX_ER, RX_CLK, and RX_DV. At the ONU, the transmit path uses GMII signals TXD<7:0>, TX_EN, TX_ER, and GTX_CLK, while the receive path uses XGMII signals RXD<31:0>, RXC<3:0> and RX_CLK.

Figure 92–3(b) depicts the operation of the asymmetric mode.

92.1.2.3 Dual rate mode

To support coexistence of symmetric 10 Gb/s, asymmetric 10/1 Gb/s, and legacy 1 Gb/s ONUs on the same outside plant, the OLT may be configured to use a dual–rate mode. Dual–rate mode supports transmission and reception at both 10 Gb/s and 1 Gb/s. When operating in a dual–rate mode, a combination of XGMII and GMII data paths are used for transmission and reception. Figure 92–4 depicts the OLT operating in a dual–rate mode.

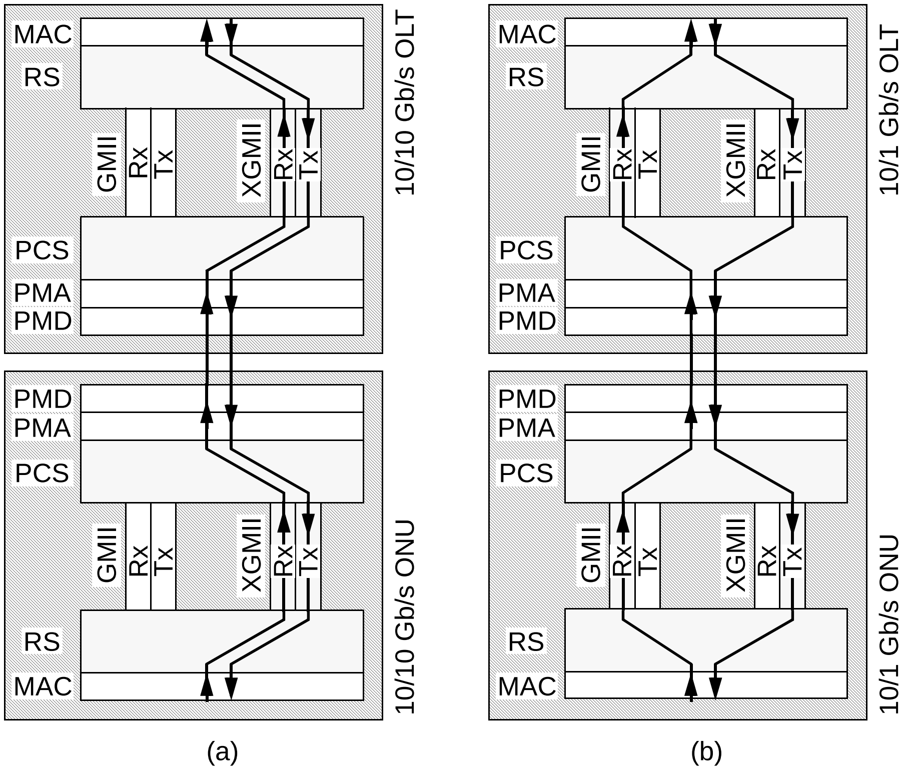


Figure 92–3—Symmetric (a) and asymmetric (b) operation of OLT and ONU.

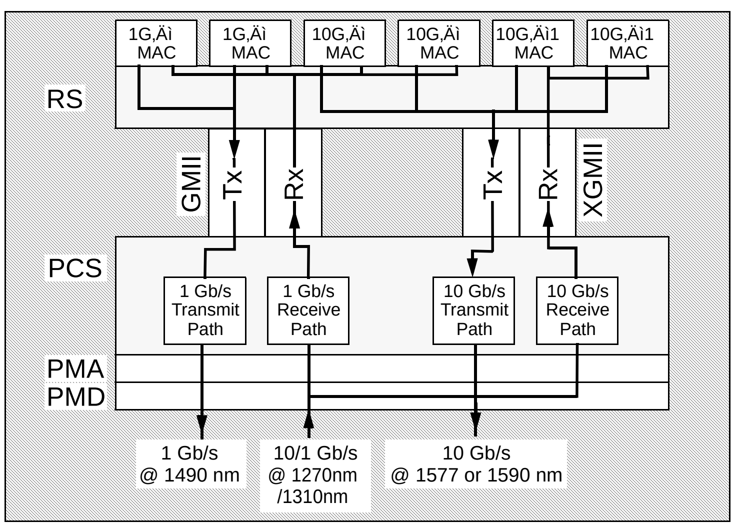


Figure 92–4—PCS and Reconciliation sublayer for dual rate mode at OLT.

92.1.2.4 Binding of XGMII and GMII primitives

Subclause 92.1.6 describes the mapping of XGMII/GMII signals to the PLS.DATA.request and PLS_DATA.indication primitives. Additional details are provided below in Table 92–1 which shows the mapping of PLS_DATA.request primitives to transmit interface signals for different types of OLTs and

ONUs. Table 92–2 shows the mapping of PLS_DATA.indication primitives to receive interface signals for different types of OLTs and ONUs.

92.1.3 Summary of major concepts

A successful registration process, described in Subclause @@93.3.3@@, results in the assignment of values to the MODE and LLID variables associated with a MAC. This may be one of many MACs in an OLT or a single MAC in an ONU. The MODE and LLID variables are used to identify a packet transmitted from that MAC and how received packets are directed to that MAC. The PCS in the OLT shall operate in unidirectional mode as defined in @@Subclause 66.2.2@@.

As described in Subclause @@93.1.2@@, multiple MACs within an OLT are bound to a single XGMII, or to an XGMII transmit path and a GMII receive path. At the ONU the MAC is either bound to an XGMII or to an XGMII receive path and a GMII transmit path. Correspondingly, only one PLS_DATA.request primitive is active at any time.

For 10G links, the mechanism is extended to allow the MAC to be bound to a single XGMII, or to a GMII transmit path and an XGMII receive path (in the case of an asymmetric ONU), or to an XGMII transmit path and a GMII receive path (in the case of an asymmetric OLT).

In the transmit direction, the RS maps the active PLS_DATA.request to either the GMII signals (TXD<7:0>, TX_EN, TX_ER, and GTX_CLK) or the XGMII signals (TXD<31:0>, TXC<3:0>, and TX_CLK) according to the MAC instance generating the request. The RS replaces octets of preamble with the values of the transmitting MAC's MODE and LLID variables.

In the receive direction, the MODE and LLID values embedded within the preamble identify the MAC to which this frame should be directed. The RS establishes a temporal mapping of either the GMII signals (RXD<7:0>, RX_ER, RX_CLK, and RX_DV) or the XGMII signals (RXD<31:0>, RXC<3:0> and RX_CLK) to the correct PLS_DATA.indication and PLS_DATA_VALID.indication primitives.

92.1.3.1 Application

This Subclause applies to the interface between the MAC and PHY in an OLT or an ONU. The physical implementation of the interface is primarily intended to be chip-to-chip but may also be used as a logical interface between ASIC logic modules within an integrated circuit. These interfaces are used to provide media independence so that an identical media access controller may be used with all 10GBASE-PR and 10/1GBASE-PRX PHY types.

92.1.3.2 Delay constraints

The MPCP relies on strict timing based on the distribution of timestamps. The actual delay is implementation dependent but an implementation shall maintain a combined delay variation through RS, PCS, and PMA sublayers of no more than 1 TQ so as to comply with this mechanism.

92.1.4 GMII structure

See Clause 35.

92.1.5 XGMII structure

The XGMII structure is discussed in Clause @@46.1.6@@, and @@Figure 46-2@@ depicts a schematic view of the RS inputs and outputs.

92.1.6 Mapping of XGMII and GMII signals to PLS service primitives

Except as noted below, the mapping of the signals provided at the XGMII to the PLS service primitives is defined in Subclause @@46.1.7@@.

As discussed in Subclause @@46.1.7.3@@, the PLS_CARRIER.indication primitive is not used for 10 Gb/s operation. However, 10G-EPON operation extends the 10 Gb/s RS by using the PLS_CARRIER.indication primitive to defer the MAC between frames in order to allow the PCS to insert FEC parity octets

Table 92–1—Binding of PLS_DATA.request primitive

MAC Location	MAC operating speed	Transmit Interface	Signals
OLT	Legacy (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK
OLT	Symmetric (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
OLT	Asymmetric (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
ONU	Legacy (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK
ONU	Symmetric (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
ONU	Asymmetric (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK

Table 92–2—Binding of PLS_DATA.indication primitive

MAC Location	MAC operating speed	Transmit Interface	Signals
OLT	Legacy (Rx: 1 Gb/s)	GMII	RXD<7:0>, RX_ER, RX_DV, RX_CLK
OLT	Symmetric (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK
OLT	Asymmetric (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK
ONU	Legacy (Rx: 1 Gb/s)	GMII	RXD<7:0>, RX_ER, RX_DV, RX_CLK
ONU	Symmetric (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK
ONU	Asymmetric (Rx: 1 Gb/s)	GMII	RXD<7:0>, RX_ER, RX_DV, RX_CLK

92.1.6.1 Generation of PLS_CARRIER.Indication primitive

92.1.6.1.1 Function

Map the primitive PLS_CARRIER.indication to the CARRIER_STATUS parameter generated by the Reconciliation Sublayer.

92.1.6.1.2 Semantics of the service primitive

PLS_CARRIER.indication(CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. CARRIER_STATUS assumes the value CARRIER_ON at the beginning of every frame and assumes the value of CARRIER_OFF after frame transmission is complete and enough time has elapsed to allow for the insertion of FEC parity. The state diagram depicted in Figure 92–5 controls the updating of the CARRIER_STATUS parameter.

92.1.6.1.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa. To ensure that enough time is inserted between frames transmitted by different MACs, the PLS_CARRIER.Indication primitive is generated simultaneously for all MACs bound the the XGMII transmit channel.

92.1.6.1.4 Conventions

The notation used in the state diagram follows the conventions of Subclause @@21.5@@. The notation ++ after a counter indicates it is to be incremented by 1. The notation -- after a counter indicates it is to be decremented by 1. The notation -= after a counter indicates that the counter value is to be decremented by the following value. The notation += after a counter indicates it is to sum itself with the following value.

92.1.6.1.5 Functions, constants, variables and counters

block_size
This constant represents the size of the FEC codeword, expressed in the units of XGMII transfer columns.
Value: 54

C_TYPE()
A function that determines what type of column is to be transmitted.
Values:
C; The column contains one of the following:
a) four valid control characters other than /Q/, /S/, /T/ and /E/;
b) one valid sequence ordered_set.
S; The column contains an /S/ in lane 0, and all characters following the /S/ are data characters.
T; The column contains a /T/ in one of its lanes, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/, and /T/.
D; The column contains four data characters.
E; The column does not meet the criteria for any other value.

col
This variable contains the contents of the current column.

new_col
TYPE: Boolean
Indicates that new column is available to transmit
Value: set to TRUE if a new column is available for transmission, reset to FALSE otherwise.

parity_cnt
This variable counts the amount of parity data to be inserted by the PCS. This variable is expressed in the units of XGMII transfer columns, where one XGMII transfer column = 4 bytes.

parity_ratio
The number of parity data columns (where 1 column = 4 bytes or one XGMII transfer) to be inserted at the end of the given FEC codeword.
Value: 8

tx_cnt
A count of the number of columns transmitted. This counter increments at TX_CLK rate (on both the rising and falling clock transitions) unless reset.

92.1.6.1.6 State diagram

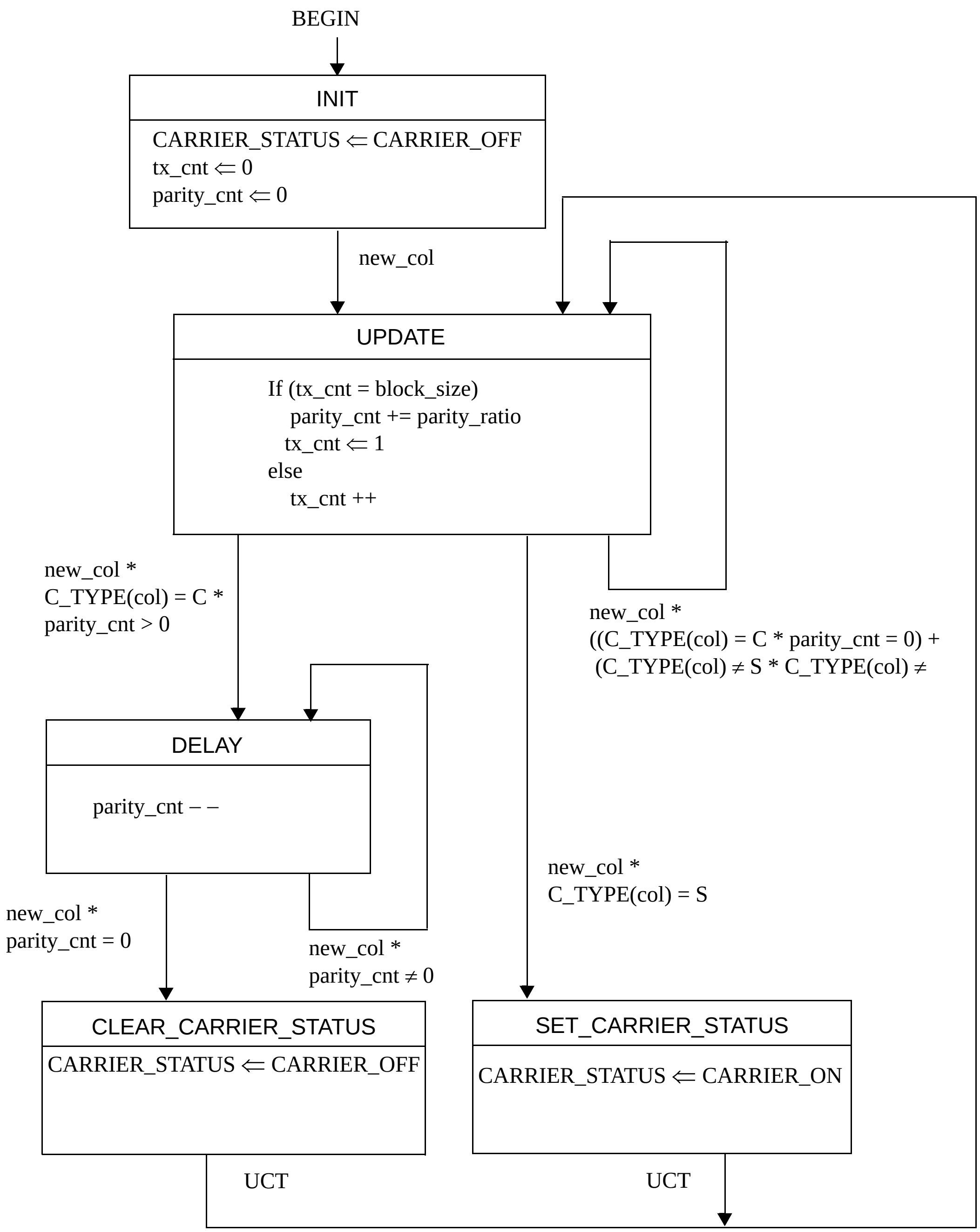


Figure 92–5—Carrier Status Generation state diagram

92.1.6.2 Functional specifications for Multiple MACs

92.1.6.2.1 Variables

The variables of @@65.1.3.1@@ are inherited except as shown below.

logical_link_id
Value: 15 bits
This variable shall be set to the broadcast value of 0x7FFE for the unregistered ONU MAC. Enabled OLT MACs may use any value for this variable. Registered ONU MACs may use any value other than 0x7FFE for this variable.

92.1.6.2.2 RS Transmit function

The transmit function is described in @@65.1.3.2@@ except as noted below in Table 92–3, which shows the replacement mapping for 10G-EPON.

Table 92–3—Preamble/SFD replacement mapping

Column	Lane	Field	Preamble/SFD	Modified preamble/SFD
0	0	-	0x55	same
	1	-	0x55	same
	2	SLD	0x55	0xd5
	3	-	0x55	same
1	0	-	0x55	same
	1	LLID[15:8]	0x55	<mode,locical_link_id[14:8]>[a]
	2	LLID[7:0]	0x55	<logical_link_id[7:0]>[b]
	3	CRC8	0xd5	The 8 bit CRC calculated over column 0 lane 2 through column 1 lane 2

[a]mode maps to TXD[15], logical_link_id[14] maps to TXD[14], logical_link_id[8] maps to TXD[8].
[b]logical_link_id[7] maps to TXD[23], logical_link_id[0] maps to TXD[16].

92.1.6.2.3 RS Receive function

The receive function is described in Subclause @@65.1.3.3@@ except as noted below.

Table @@65-2@@ is not applicable to 10G-EPON.

92.1.6.2.3.1 SLD

The 10 Gb/s RS transmit function must maintain an alignment for its start control character to lane 0. The SLD is transmitted as the third octet and therefore is aligned to lane 2 in the same column containing the start control character. This is the only possibility considered when parsing the incoming octet stream for the SLD. If the SLD field is not found then the packet shall be discarded. If the packet is transferred, the SLD shall be replaced with a normal preamble octet and the two octets preceding the SLD and the one octet following the SLD are passed without modification. See Table 92–3.

92.1.6.2.3.2 LLID

This section supersedes the stipulations of Subclause@@ 65.1.3.3.2@@.

The third and fourth octets following the SLD contain the mode and logical_link_id values. OLTs and ONUs act upon these values in a different manner.

If the device is an OLT, then the following comparison is made:

a) The received mode bit is ignored
b) If the received logical_link_id value matches 0x7FFF or 0x7FFE and an enabled MAC exists with a logical_link_id variable with the same value, then the comparison is considered a match to that MAC.
c) If the received logical_link_id has a value other than 0x7FFF or 0x7FFE and an enabled MAC exists with a mode variable with a value of 0 and a logical_link_id variable matching the received logical_link_id value, then the comparison is considered a match to that MAC.

If the device is an ONU then the following comparison is made:

a) If the received mode bit is equal to 0 and the received logical_link_id value matches the logical_link_id variable, then the comparison is considered a match.
b) If the received mode bit is equal to 1 and the received logical_link_id value does not match the logical_link_id variable, or the received logical_link_id matches 0x7FFE, then the comparison is considered a match.

If no match is found, then the packet shall be discarded within the RS. If a match is found, then the packet is intended to be transferred. If the packet is transferred, then both octets of the LLID field shall be replaced with normal preamble octets.

If the packet is transferred, the one octet preceding the LLID is passed without modification. See Table 92–4 for a list of reserved LLIDs.

Table 92–4—Reserved LLID values

LLID value	Purpose
0x7FFF	unregistered ONU [a b]
0x7FFE	unregistered ONU [b c]
0x7FED - 0x7F00	reserved for future use [b c]

[a]Normative for 1000BASE-X
[b]Normative for 10/1GBASE-PRX and 10GBASE-PR
[c]Informative for 1000BASE-X

92.1.6.2.3.3 CRC-8

The CRC-8 field is as described in Subclause @@65.1.3.3.3@@.

92.2 Physical Coding Sublayer (PCS) for 10G-EPON

92.2.1 Overview

This subclause defines the physical coding sublayers 10GBASE-PR and 10/1GBASE-PRX, supporting burst mode operation of the point-to-multipoint physical medium. The 10GBASE-PR PCS is specified to support 10Gb/s symmetric mode, where both the receive and transmit paths operate at 10 Gb/s rate. The 10/1GBASE-PRX PCS supports 10/1 Gb/s asymmetric mode, in which OLT transmit path and ONU receive path operate at 10 Gb/s, while the ONU transmit path and the OLT receive path operate at 1 Gb/s rate.

This subclause also specifies a forward error correction (FEC) mechanism to increase the optical link budget or the fiber distance. Figure 92–1 and Figure 92–2 show the relationship between the extended PCS sublayer and the ISO/IEC OSI reference model.

92.2.1.1 10/1GBASE-PRX PCS

Conceptually, 10/1GBASE-PRX PCS represents a combination of transmit and receive functions defined in 10GBASE-PR PCS (specified in this clause) and 1000BASE-PX PCS (specified in Clause 65). At the OLT, the 10/1GBASE-PRX consists of 10GBASE-PR transmit function and 1000BASE-PX receive function (see Figure 92–6). Reciprocally, at the ONU, the 10/1GBASE-PRX PCS consists of 10GBASE-PR receive function and 1000BASE-PX transmit function (see Figure 92–7).

In this clause, no explicit specification is provided for 10/1GBASE-PRX PCS. It is expected that deriving such specification from 10GBASE-PR and 1000BASE-PX PCS specifications as described above will be a straightforward process.

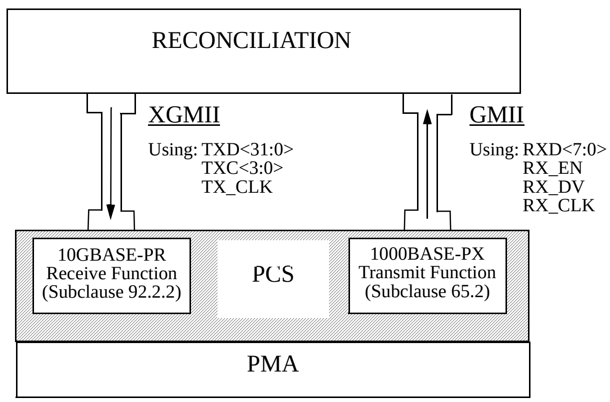


Figure 92–6—Conceptual Diagram of 10/1GBASE-PRX PCS, OLT Side

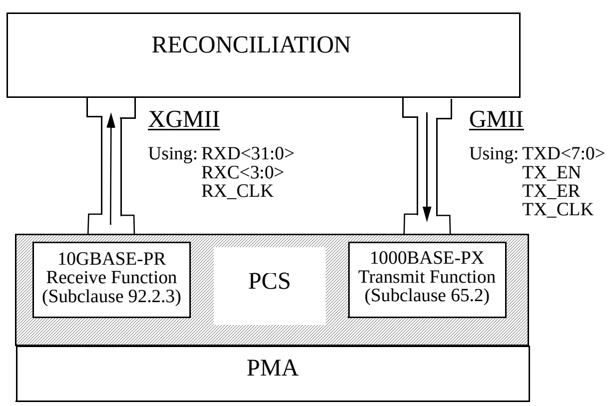


Figure 92–7—Conceptual Diagram of 10/1GBASE-PRX PCS, ONU Side

92.2.1.2 10GBASE-PR PCS

The 10GBASE-PR PCS extends the physical coding sublayer described in Clause 49 to support burst mode operation of the point-to-multipoint physical medium. Figure 92–8 illustrates functional block diagram of the downstream path and Figure 92–9 represents functional block diagram of the upstream path.

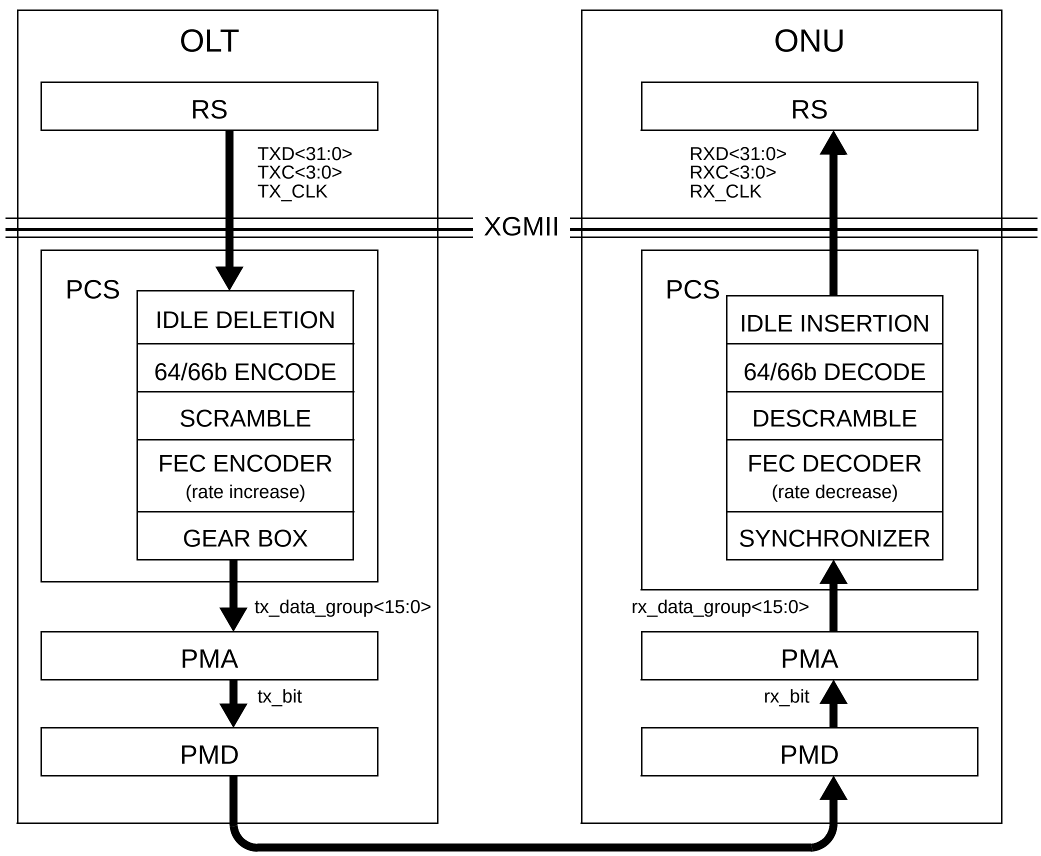


Figure 92–8—PCS Extension functional block diagram, downstream path

92.2.2 PCS Transmit function

This subclause defines the transmit direction of physical coding sublayers for 10GBASE-PR and 10/1GBASE-PRX. In the OLT, the PCS operates at a 10 Gb/s rate in a continuous mode. In the ONU, the PCS may operate at a 10 Gb/s rate, as specified herein (10GBASE-PR), or at a 1 Gb/s rate, compliant with Clause 65 (10/1GBASE-PRX). For both 10GBASE-PR and 10/1GBASE-PRX, the ONU PCS always operates in a burst mode. When operating at the 10 Gb/s rate, the PCS includes a mandatory FEC encoder. The transmit direction of OLT PCS is illustrated in Figure 92–8 and in Figure 92–9 for the transmit direction of the ONU PCS.

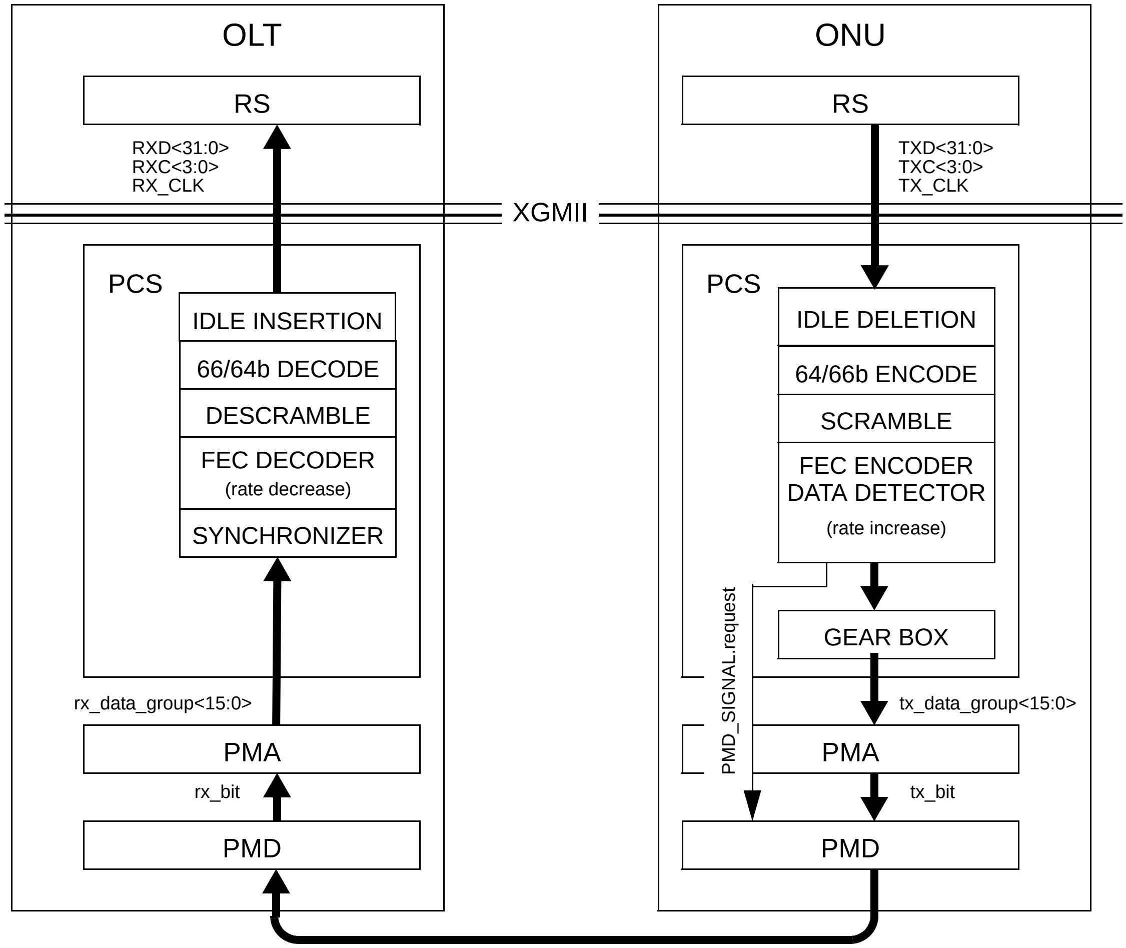


Figure 92–9—PCS Extension functional block diagram, upstream path

92.2.2.1 Alignment and IDLE control character deletion

The IDLE DELETION process is responsible for deleting excess IDLE characters to allow the parity data be inserted without increasing the PMD line rate. This process deletes four 72-bit vectors containing IDLE characters per every thirty-one 72-bit vectors received from the XGMII, always ensuring that the minimum IPG has been preserved between two adjacent frames.

In addition, at the ONU, the IDLE DELETION process aligns the start of the first frame in a burst, such that, if the start control code is in lane 0 of column 1, the burst will be shifted to align the start to lane 0 of column 0. If this alignment is not done, the ONU's transmission period may extend by a full FEC codeword, causing interference with transmissions by other ONUs.

The Alignment and Idle Detection function shall be implemented in the PCS as depicted in Figure 92–11 for ONUs and as in Figure 92–10 for OLTs, including compliance with the associated state variables as specific in Subclause 92.2.2.1.1. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in @@Subclause 21.5@@. State diagram variables follow the conventions of @@Subclause 21.5.2@@

except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

92.2.2.1.1 Constants

FEC_DSize
TYPE: 16-bit unsigned
The number of 72-bit vectors consituting a payload of a FEC codeword. To normalize pre-FEC data rate, the IDLE Deletion function removes FEC_PSize vectors per every FEC_DSize vectors transfered to the 64B/66B encoder.
Value: 27

FEC_PSize
TYPE: 16-bit unsigned
The number of 72-bit vectors consituting parity portion of a FEC codeword. To normalize pre-FEC data rate, the IDLE Deletion function removes FEC_PSize vectors per every FEC_DSize vectors transfered to the 64B/66B encoder.
Value: 4

MinIpg
TYPE: 8-bit unsigned
The number of 72-bit vectors consisting of IDLE control characters that constitute minimum IPG.
Value: 1

92.2.2.1.2 Variables

BEGIN
TYPE: Boolean
This variable is used when initiating operation of the state diagram. It is set to true following initialization and every reset.

DelayBound
TYPE: 16-bit unsigned
This value represents the delay sufficient to initiate the laser and to stabilize the receiver at the OLT (i.e. the maximum FIFO size expressed in 66-bit blocks). The value includes maximum laserOnTime (@@93.3.3.2@@), $T_{receiver\_settling}$, T_{CDR}, Burst Delimiter, and the two 66-bit blocks containing IDLEs, that preceed the first frame in the burst. This variable is used only by the ONU.
Default: 0x010F

HalfShift
TYPE: Boolean
True if data is currently shifted by one XGMII column. False if data is not currently shifted.

tx_next<35:0>
36-bit vector containing one XGMII transfer. This vector is used to shift the data stream by one XGMII clock in order to align burst start to even XGMII transfer. The XGMII transfer is mapped into the tx_next<35:0> as follows:
RXC<3:0> bits are mapped to bits tx_next<3:0>;
RXD<31:0> bits are mapped to bits tx_next<35:4>.

tx_raw<71:0>
72-bit vector containing two XGMII transfers passed to the Idle Deletion function. The XGMII transfers are mapped into the tx_raw<71:0> as follows:

RXC<3:0> of the first transfer are mapped to bits tx_raw<3:0>;
RXD<31:0> of the first transfer are mapped to bits tx_raw<35:4>;
RXC<3:0> of the second transfer are mapped to bits tx_raw<39:36>;
RXD<31:0> of the second transfer are mapped to bits tx_raw<71:40>.

tx_raw_out<71:0>
72-bit vector sent from the output of the Idle Deletion function to the 64B/66B encoder. The vector contains two XGMII transfers mapped as shown for tx_raw<71:0>.

tx_temp<35:0>
36-bit vector used to temporarily hold one XGMII transfer. The XGMII transfer is mapped into the tx_temp<35:0> as shown for tx_next<35:0> above.

92.2.2.1.3 Functions

T_TYPE(rx_raw<71:0>)
This function is defined in @@49.2.13.2.3@@.

92.2.2.1.4 Counters

DelCount
TYPE: 16-bit unsigned
Counts the number of 72-bit vectors than need to be deleted.

IdleCount
TYPE: 16-bit unsigned
Counts the number of 72-bit vectors containing IDLE control characters or other control vectors.

VectorCount
TYPE: 16-bit unsigned
Counts the number of 72-bit vectors transmitted.

92.2.2.1.5 State Diagrams

The OLT PCS Idle deletion function shall implement the state machine as shown in Figure 92–10. The ONU PCS Idle deletion function shall implement the state machine as shown in Figure 92–11. Should there be a discrepancy between a state machines and descriptive text, the state machines prevail..

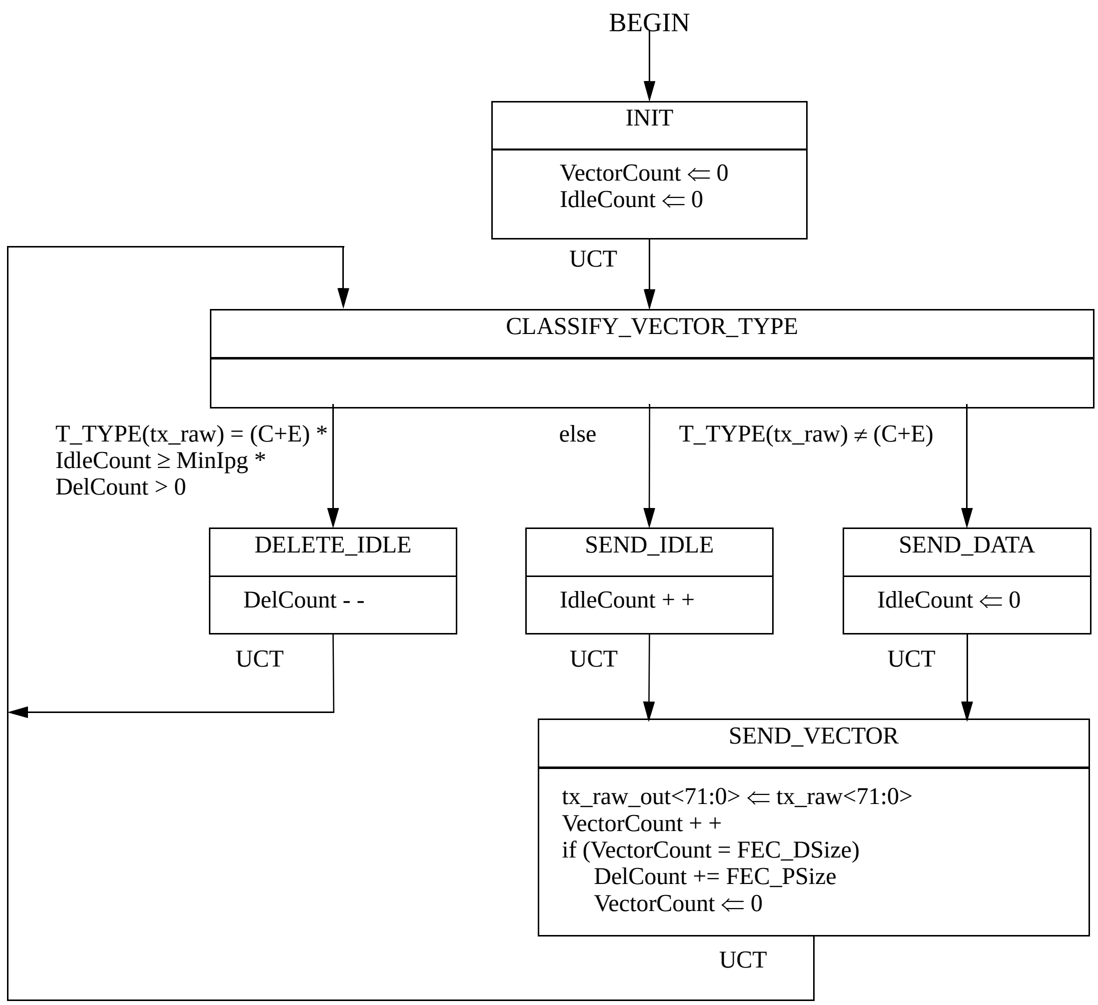


Figure 92–10—OLT Idle Deletion state diagram

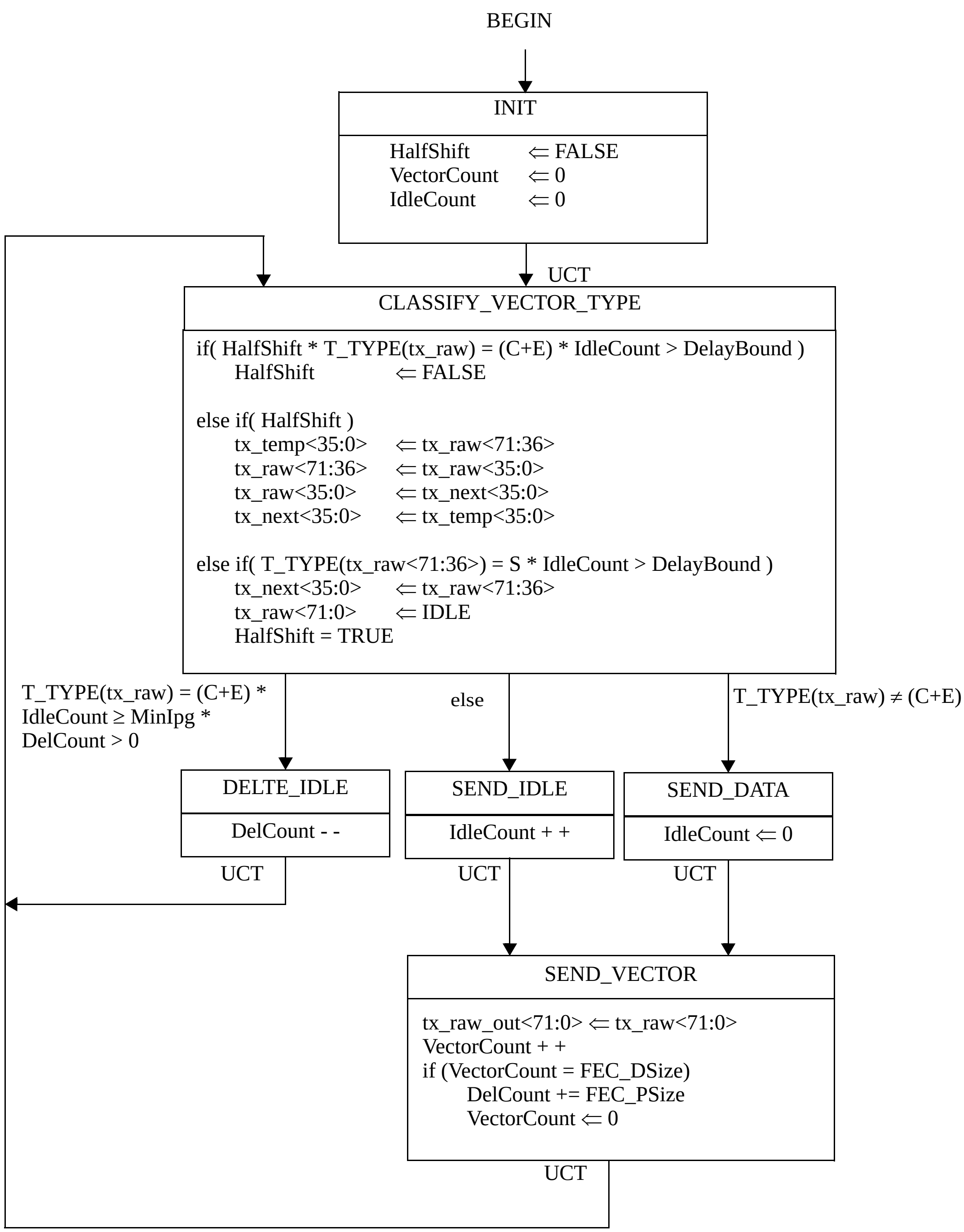


Figure 92–11—ONU Idle Deletion state diagram

92.2.2.2 64B/66B Encode

See Subclause @@49.2.4@@ 64B/66B transmission code.

92.2.2.3 Scrambler

See Subclause @@49.2.6@@ Scrambler.

92.2.2.4 FEC Encoding

The FEC code used for 10G-EPON links is the Reed-Solomon code (255, 223).

92.2.2.4.1 FEC Algorithm (RS(255, 223))

The FEC code used for 10GBASE-PR links is a linear cyclic block code - the Reed-Solomon code (255, 223) over the Galois Field of GF(2^8) - a non-binary code operating on 8-bit symbols. The code encodes 223 information symbols and adds 32 parity symbols. The code is systematic - meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is based on the generating polynomial $G(x) = \prod_{i=0}^{31}(x - \alpha^i)$.

where:

α is equal to 0x02 and is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$

A codeword of the systematic code is presented by $D(x) + P(x) = G(x) \times L(x)$

where:

$D(x)$ is the data vector $D(x) = D_{222}X^{254} + \ldots + D_0X^{32}$. D_{222} is the first data octet and D_0 is the last.

$P(x)$ is the parity vector $P(x) = P_{31}X^{31} + \ldots + P_0$. P_{31} is the first parity octet and P_0 is the last.

A data octet (d_7, d_6, ..., d_1, d_0) is identified with the element: $d_7\alpha^7 + d_6\alpha^6 + \ldots + d_1\alpha^1 + d_0$ in GF(2^8), the finite field with 2^8 elements. The code has a correction capability of up to sixteen symbols.

Note - For the (255,223) Reed-Solomon code, the symbol size equals one octet. The d_0 is identified as the LSB and d_7 is identified as the MSB bit in accordance with the conventions of Subclause @@3.1.1@@. See Figure 92–12.

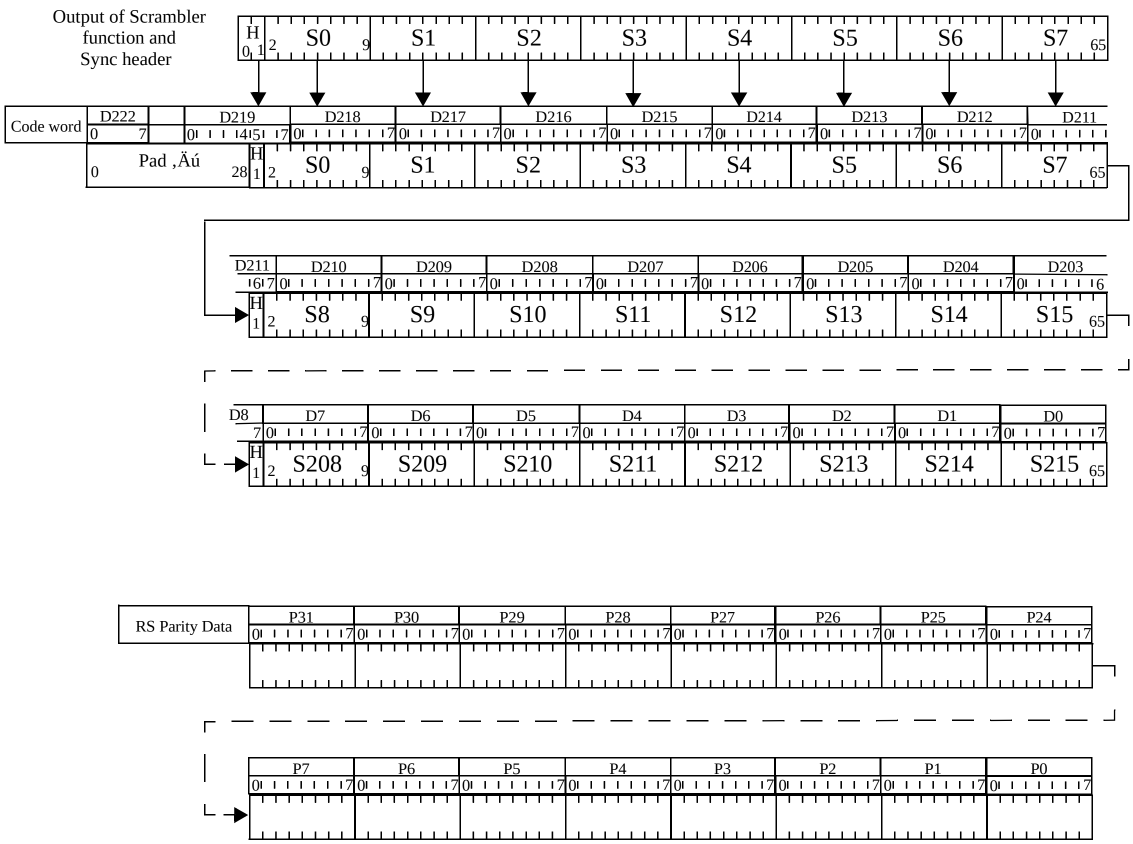


Figure 92–12—Bit ordering in FEC codeword generation

92.2.2.4.2 Parity Calculation

Padding of FEC codewords and appending FEC parity bytes in the 10GBASE-PR PCS transmitter is illustrated in Figure 92–13. The 64B/66B encoder and scrambler produce 66-bit blocks. The FEC encoder accumulates 27 of these 66-bit blocks to form the basis of an FEC codeword, removing the redundant first bit (i.e. sync header bit <0>) of each block (the first bit is guaranteed to be the complement of the second bit).

The FEC encoder then prepends 29 "0" padding bits to the 27 65-bit blocks to form the 223-byte payload portion of an FEC codeword. This data is then FEC-encoded, resulting in the 32-byte parity portion of the FEC codeword. The 223-byte payload portion and 32-byte parity portion combine to form the 255-byte Reed-Solomon codeword. The padding is used to generate the FEC codeword but is not transmitted.

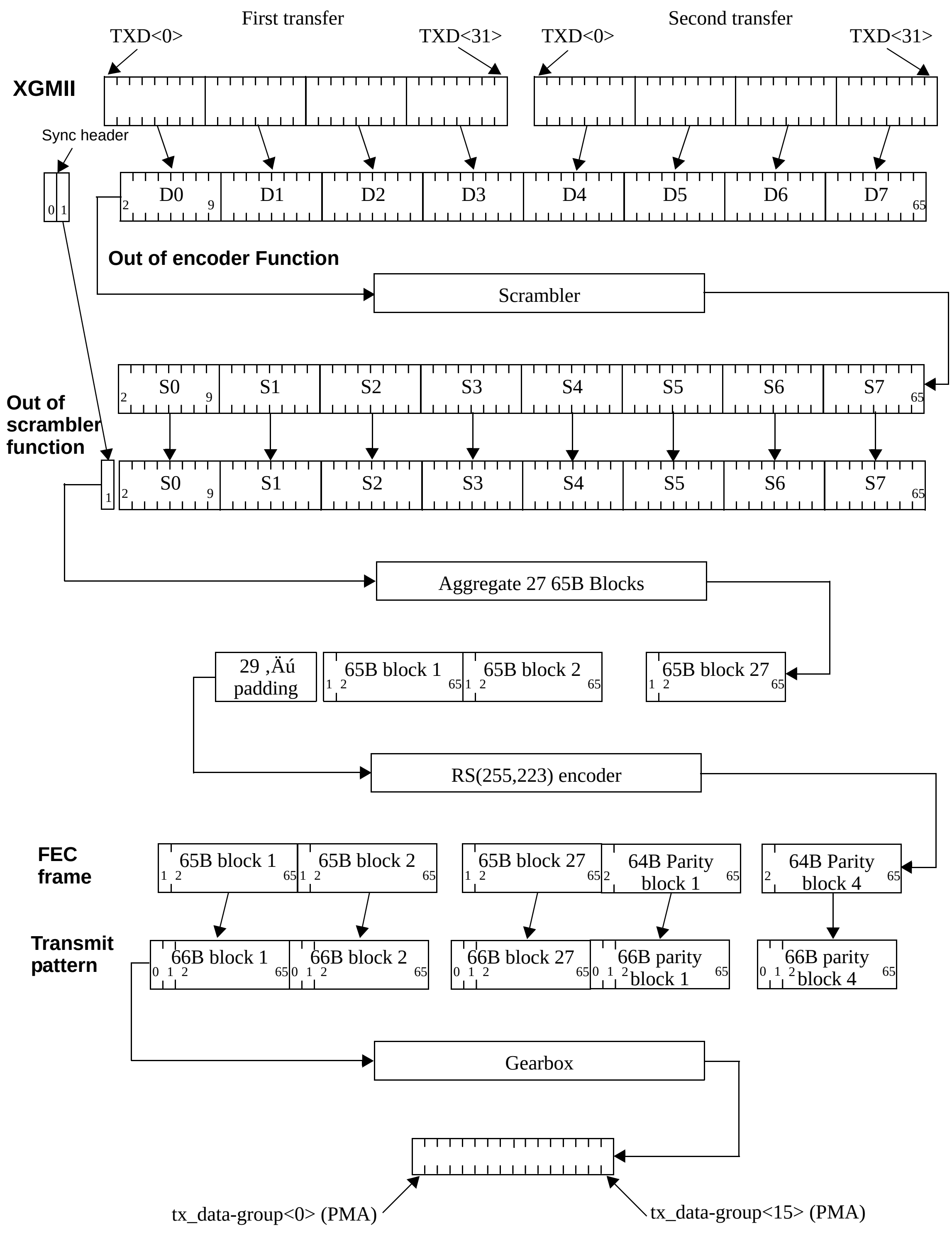


Figure 92–13—PCS Transmit bit ordering

92.2.2.4.3 FEC Transmission Block Formating

As shown in Figure 92–13, after the Reed-Solomon codeword has been computed, the FEC encoder constructs the transmittable FEC frame with the original sequence of 27 66-bit blocks (including the redundant sync bit, but not including the 29 "0" padding bits). The FEC encoder prepends a 2 bit sync header to each group of 64 parity bits to construct a properly formed 66-bit codeword, according to the predefined sync header pattern for the four 64-bit parity blocks: 00 11 11 00. Finally the four 66-bit parity blocks are appended following the 27 66-bit data blocks and transmitted to the PMA.

92.2.2.5 Data Detector and Burst Mode Considerations (ONU only)

To avoid spontaneous emission noise from near ONUs obscuring the signal from a distant ONU, the lasers in ONUs must be turned off between transmissions. To control the laser, the ONU PCS is extended to detect the presence of transmitted data and generate the PMD_SIGNAL.request(tx_enable) primitive to turn the laser on and off at the correct times. This function is performed by the Data Detector shown in the functional block diagram in Figure 92–9.

The DATA DETECTOR contains a delay line (FIFO buffer) storing code-groups to be transmitted. Figure 92–14 shows the relationship of filling the buffer and the generation of laser control. . The length of the FIFO buffer shall be chosen such that the delay introduced by the buffer together with any delay introduced by the PMA sublayer is long enough to turn the laser on and to allow a laser synchronization pattern, Burst Delimiter pattern and a predefined number of IDLE control character to be transmitted. The laser synchronization pattern allows the receiving optical detector to adjust its gain ($T_{receiver\_settling}$) and synchronize its receive clock (T_{cdr}). The Burst Delimiter allows the receiver to easily identify the beginning of FEC protected portion of the ONU transmission. The IDLE control characters are used to synchronize the scrambler and start of packet delineation.

In the OLT, the laser always remains turned on. Correspondingly, therefore, the OLT’s Data Detector does not need a delay line or buffer in the data path for this purpose.

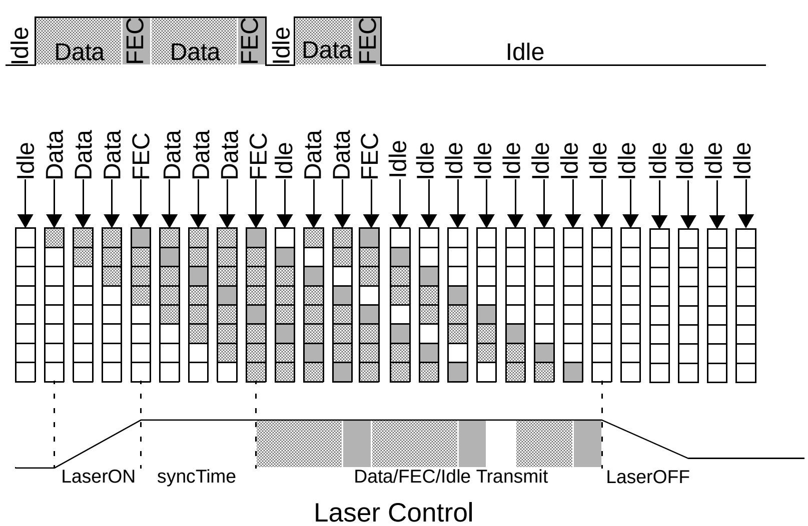


Figure 92–14—Laser control as a function of buffer fill

Upon initialization, the FIFO buffer is filled with IDLE control characters and the laser is turned off. When the first, non-IDLE code group arrives at the buffer, the Data Detector sets the PMD_SIGNAL.request(tx_enable) primitive to the value ON, instructing the PMD sublayer to start the process of turning the laser on.

When the buffer empties of data (i.e., contains only IDLE control characters), the Data Detector sets the PMD_SIGNAL.request(tx_enable) primitive to the value OFF, instructing the PMD sublayer to start the process of turning the laser off. Between packets, IDLE control characters will arrive at the buffer. If the number of these IDLE control characters is insufficient to fill the buffer then the laser is not turned off.

Figure 92–15 illustrates the details of the ONU burst transmitition. In particular, this figure shows the details of the synchronization time and the FEC protected portions of the burst transmision.

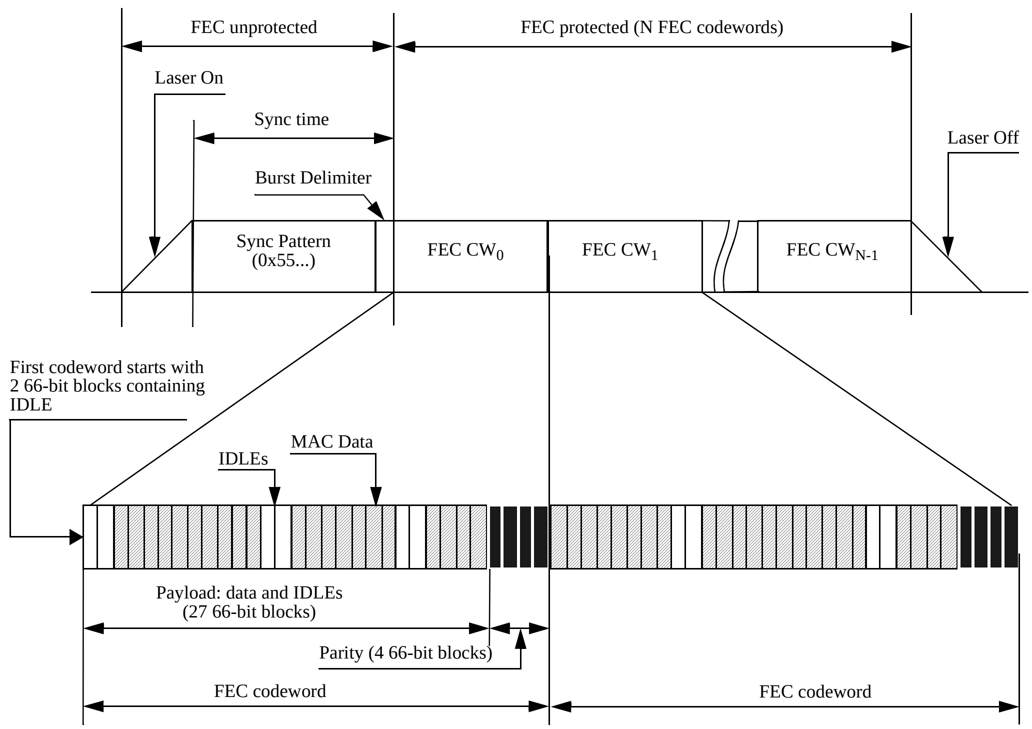


Figure 92–15—Details of burst composition

The ONU burst transmission begins with a synchronization pattern 0x55 (transmission bit sequence 1010 ...), which facilitates receiver clock recovery and gain control at the OLT. To facilitate FEC codeword synchronization, the ONU transmits a 66-bit BURST_DELIMITER (see Figure 92–15). When received at the OLT, the BURST_DELIMITER allows for FEC codeword alignment on the incoming data stream, even in the presence of bit errors. The BURST_DELIMITER is followed by two 66-bit blocks containing IDLE codes. The first 66-bit block is used to synchronize the descrambler and a second 66-bit block is needed to provide IPG at the OLT. These two 66-bit IDLE blocks are part of the first FEC codeword.

The ONU burst transmission ends with a burst terminator pattern of 3 blocks of all zeroes (see Figure 92–

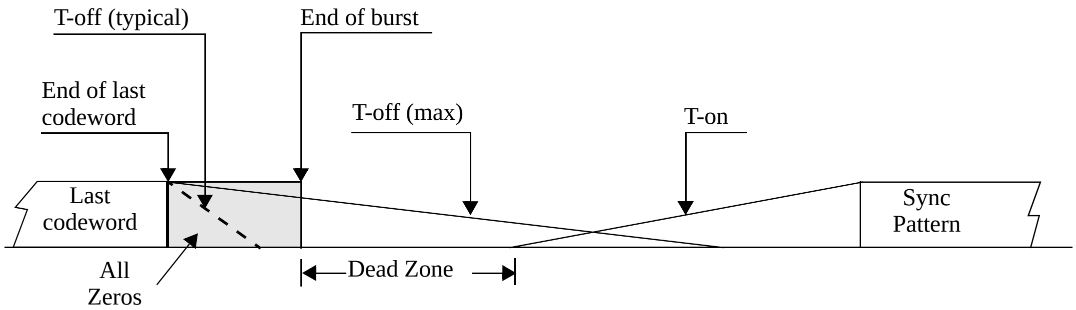


Figure 92–16—ONU burst transmission termination

16). When received at the OLT, the burst terminator allows for the rapid reset of the OLT FEC synchronizer, so that it can search for the next burst. The burst terminator is not part of the last FEC codeword. Note that while the burst terminator is part of the ONU burst transmission, the laser-off commences at the beginning of the burst terminator. This is possible because transmitting all zeroes and turning the laser off are equivalent to the same thing: emit no light.

Two consecutive XGMII transfers provide eight characters that are encoded into one 66-bit transmission block. To increase burst efficiency, the start of a burst is aligned to the first of these two transfers (see Figure 92–11). Otherwise, the burst may occasionally be required to transmit and extra 4 bytes of data, causing the burst to extend into the next grant period. To ensure the start of a burst aligns to lane 0 of the XGMII, the PCS is extended to allow removal of leading IDLE control characters.

The body of this Subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR PCS transmitters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in @@Subclause 21.5@@. State diagram variables follow the conventions of @@Subclause 21.5.2@@ except when the variable has a default value.

92.2.2.5.1 Constants

BURST_DELIMITER
TYPE: 66-bit unsigned
A 66-bit value used to find the beginning of the first FEC codeword in the upstream burst.
Value: 0x 4 97 BA C4 69 F0 4C 88 FD (transmission bit sequence: 10 11101001 01011101 00100011 10010110 00001111 00110010 00010001 10111111)

FEC_DSize
See Subclause 92.2.2.1.1.

SP
Type: 66-bit unsigned
The burst mode synchronization pattern.
Value: 0x4 55 55 55 55 55 55 55 55 (transmission bit sequence 1010...)

92.2.2.5.2 Variables

SYNC_LENGTH
TYPE: 16-bit unsigned
Required number of sync blocks per burst. The value of this variable is derived from the syncTime parameter passed from the OLT to the ONU. See @@93.3.3.2@@ for details.

92.2.2.5.3 Functions

ReceiveNextBlock()
This function is used to receive the next 66-bit block from the scrambler. ReceiveNextBlock() is a blocking function – it does not return until a next block becomes available and is stored in the tail position in the FIFO_DD, as represented by the code FIFO_DD[N] = tx_data<65:0>.

```
ReceiveNextBlock()
   {
      // shift FIFO_DD forward
      FIFO_DD[0] = FIFO_DD[1]
      FIFO_DD[1] = FIFO_DD[2]
         ...
      FIFO_DD[N-1] = FIFO_DD[N]
      // receive next 66-bit block from scrambler
      FIFO_DD[N] = tx_block<65:0>
   }
```

TransmitBlock(tx_block<65:0>)
This function passes its argument to the GearBox for further transmission to the PMA.

92.2.2.5.4 Messages

PMD_SIGNAL.request(tx_enable)
This primitive is used to turn the laser on and off at the PMD sublayer. In the OLT, this primitive shall always take the value ON. In the ONU, the value of this variable is controlled by the Data detector state diagram (see Figure 92–18).

92.2.2.5.5 Counters

IdleBlockCount
TYPE: 16-bit unsigned
The number of consecutive non-data blocks ending with the most recently received block. The non-data blocks are represented by sync header 10 (binary).

ProtectedBlockCount
TYPE: 8-bit unsigned
The number of blocks added to a payload of a current FEC codeword. After reaching the full payload size (27), this variable is reset to 0.

SyncBlockCount
TYPE: tbd
The number of synchronization blocks transmitted in current burst.

UnprotectedBlockCount
TYPE: 8-bit unsigned

This counter is similar to ProtectedBlockCount, but counts payload size outside of grant. This variable is used to determine a number of overhead blocks to be added to maintain proper PHY rate outside the FEC-protected grant area.

92.2.2.5.6 State diagrams

The OLT shall implement the Data Detector as depicted in Figure 92–17. The ONU shall implement the

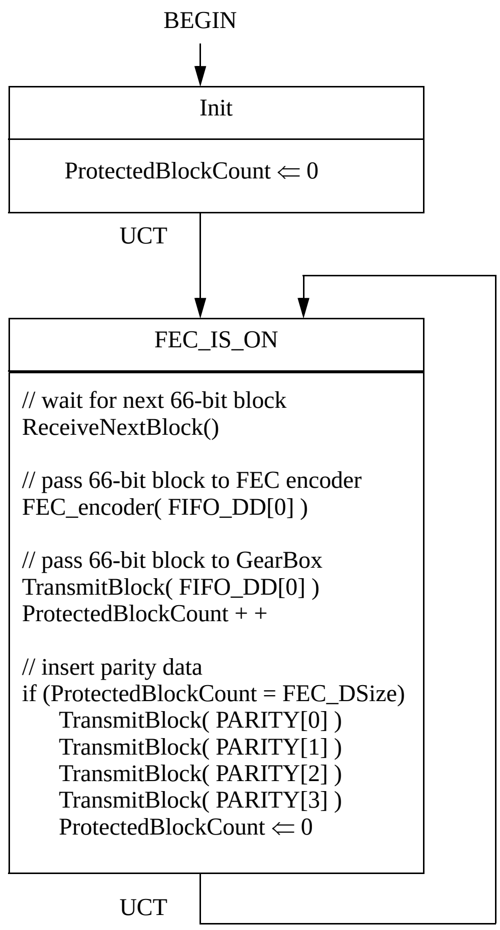


Figure 92–17—OLT Data Detector state diagram

Data Detector as depicted in Figure 92–18.

92.2.2.6 Gearbox

See Subclause @@49.2.7@@ Gearbox.

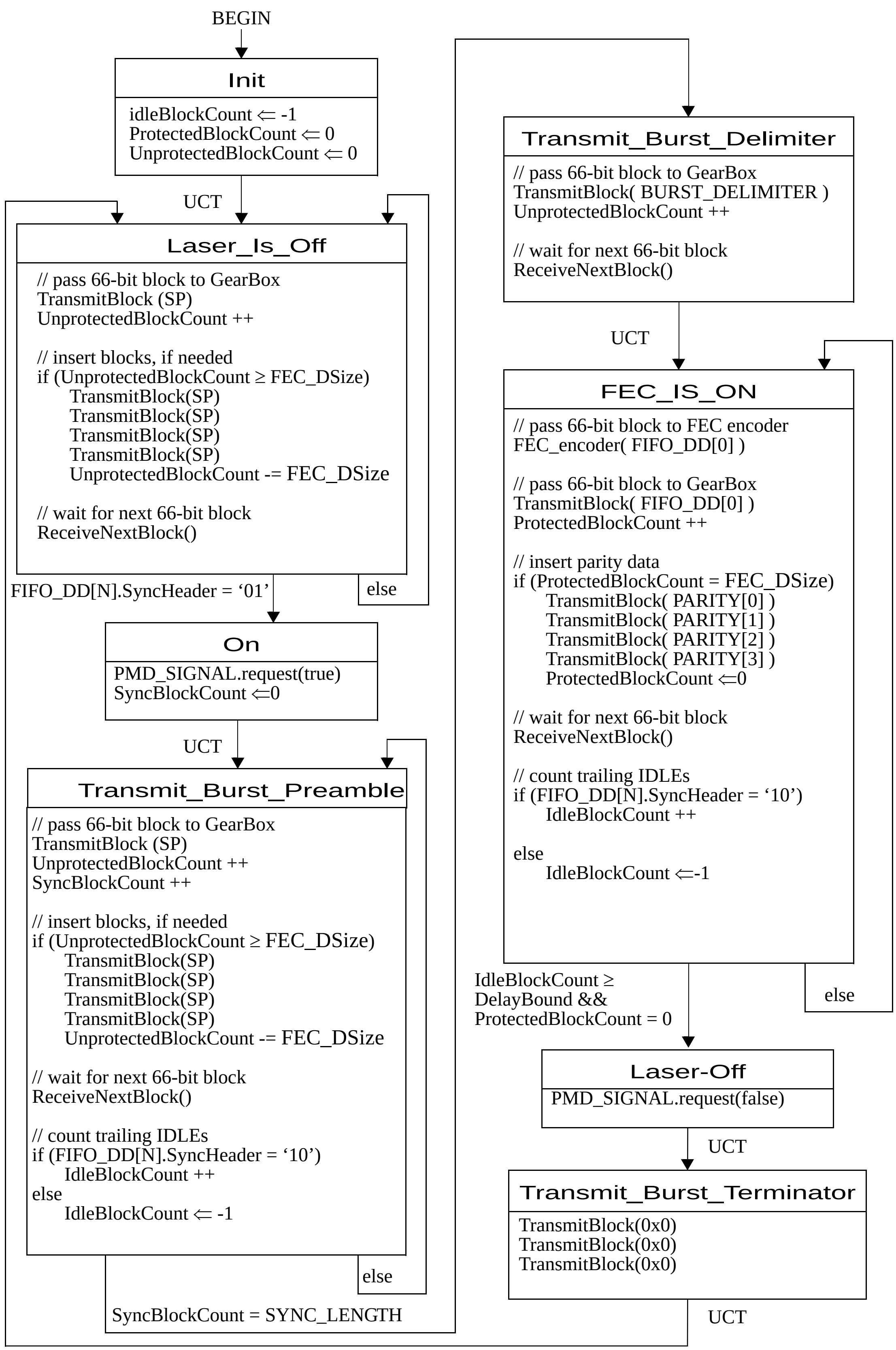


Figure 92–18—ONU Data Decoder state diagram

92.2.3 PCS Receive Function

This subclause defines the receive direction of physical coding sublayers for 10GBASE-PR and 10/1GBASE-PRX. In the ONU, the PCS operates at a 10 Gb/s rate in a continuous mode. In the OLT, the PCS may operate at a 10 Gb/s rate, as specified herein (10GBASE-PR), or at a 1 Gb/s rate, compliant with Clause 65 (10/1GBASE-PRX). For both 10GBASE-PR and 10/1GBASE-PRX, the OLT PCS always operates in burst mode. When operating at the 10 Gb/s rate, the PCS includes a mandatory FEC decoder. The receive direction of ONU PCS is illustrated in Figure 92–8 and receive direction for the OLT PCS is illustrated in Figure 92–9.

92.2.3.1 OLT Synchronizer

The OLT codeword synchronization function receives data via 16-bit PMA_UNITDATA.request primitive.

The OLT synchronizer shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 92–19). It obtains lock to the 31*66-bit blocks in the bit stream by looking for the burst delimiter. Lock is obtained as specified in the codeword lock state diagram shown in Figure 92–19. When in codeword lock, the state diagram accumulates the appropriate contents of the 31 blocks that constitute a codeword in an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword. When in codeword lock, the state diagram looks for the end of the burst. When this is observed, then the state diagram deasserts codeword lock. The state diagram then goes back to searching for the burst delimiter.

92.2.3.1.1 Variables

BD_valid
  TYPE:boolean
  Indication that is set true if received block rx_coded matches the BURST_DELIMITER with less than 12 bits difference, and de-asserted otherwise.

cword_lock
  TYPE: boolean
  Boolean variable that is set true when receiver acquires codeword delineation.

decode_success
  TYPE: boolean
  Indication that is set true if the codeword was successfully decoded by the FEC algorithm, and false otherwise.

EOB_valid
  TYPE:boolean
  Indication that is set true if the last 2 received blocks have less than 11 one bits in total, and deasserted otherwise.

inbuffer[]
  TYPE: array
  An array of 2040 bits.

input_buffer_location
  TYPE:
  An integer that points to the next appending location in the input buffer.

persist_dec_fail
  TYPE: boolean

Indication that is set when three consecutive decoding failures have occured.

reset
This variable is inherited from @@Subclause 49.2.13.2.2@@.

rx_coded<65:0>
This variable is inherited from @@Subclause 49.2.13.2.2@@.

signal_ok
This variable is inherited from @@Subclause 49.2.13.2.2@@.

92.2.3.1.2 Counters

decode_failures
TYPE:
Counter that holds the number of consecutive decoding failures.

sh_cnt
This counter is inherited from @@Subclause 49.2.13.2.4@@.

92.2.3.1.3 Functions

Append_inbuffer()
Appends the newly arrived 66-bit block into the input buffer of the FEC decoding algorithm, taking care to only insert the bits to be protected, and discarding the unwanted bits.

```
Append_inbuffer()
{
   BlockFromGearbox()
   if(rx_coded<0> <> rx_coded<1>){
      inbuffer[input_buffer_location]=rx_coded<1>
      input_buffer_location++
   }
   for(i=2, i<66, i++) {
      inbuffer[input_buffer_location]=rx_coded<i>
      input_buffer_location++
   }
}
```

BlockFromGearbox
Function that accepts the next rx_coded<0..65> block of data from the gearbox. It does not return until the transfer is completed.

Decode()
Triggers the FEC decoding algorithm to accept the contents of the input buffer, and do its decoding work. Note that this function is not blocking, and returns immediately. It is assumed that the FEC decoding algorithm copies the input buffer contents into its own internal memory, so that the input buffer is released to accept the next codeword.

DecodeWhenReady()
Determines if the inbuffer contains a full codeword, and if so, it triggers the Decode function, and then clears the inbuffer for the next codeword.

```
DecodeWhenReady()
{
   if (sh_cnt=0 or sh_cnt=31) {
      if (cword_lock) {
         Decode();
      }
      Flush_inbuffer();
   }
}
```

Flush_inbuffer()

Flushes the input buffer of the FEC decoding algorithm block.

```
Flush_inbuffer()
{
   for(i=0, i<2040, i++) {
      inbuffer[i]=0
   }
   input_buffer_location = 29
}
```

SLIP_One_Bit

Causes the next candidate block sync position to be tested. The next candidate must be exactly one bit later than the previous candidate – no burst alignments may be skipped.

92.2.3.1.4 State diagram

The OLT Synchronizer shall implement the state diagram as depicted in Figure 92–19. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

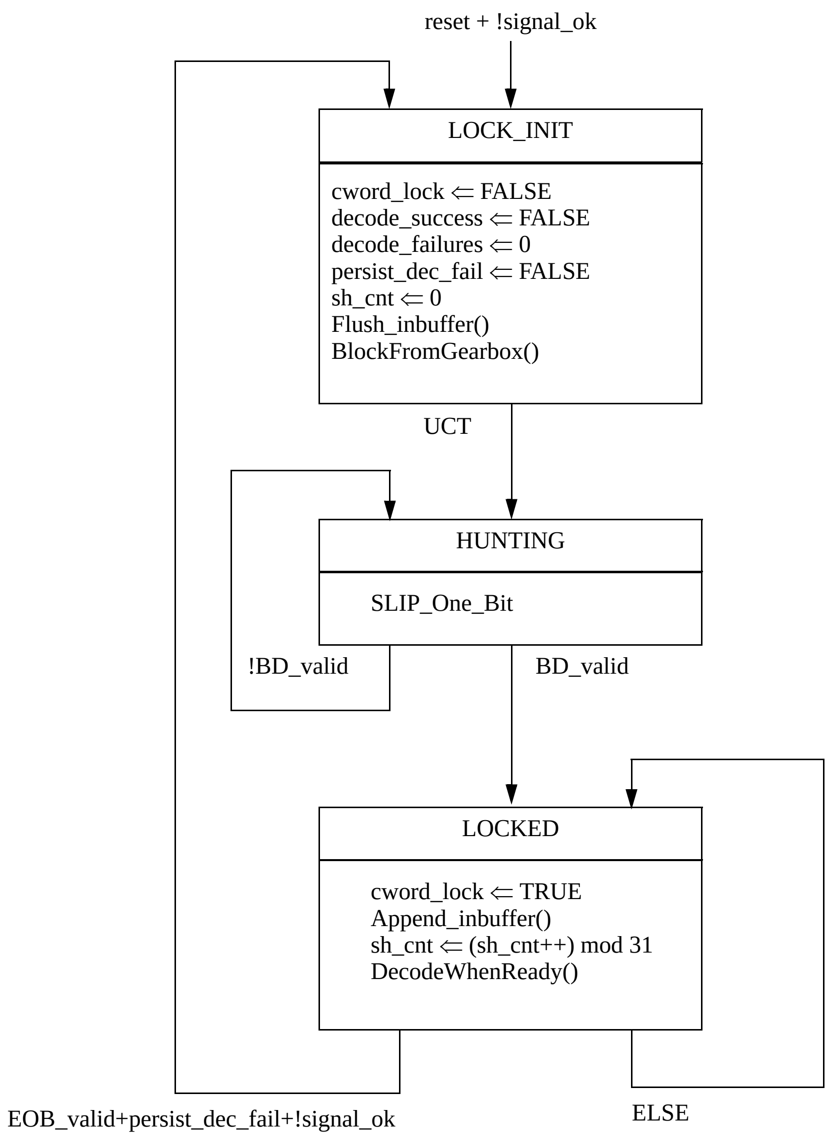


Figure 92–19—OLT Synchronizer state diagram

92.2.3.2 ONU Synchronizer

The codeword synchronization function receives data via 16-bit PMA_UNITDATA.request primitive.

The synchronizer shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 92–20). It obtains lock to the 31*66-bit blocks in the bit stream using the sync headers and outputs 2040-bit codewords to the FEC decoder function. Lock is obtained as specified in the codeword lock state diagram shown in Figure 92–21.

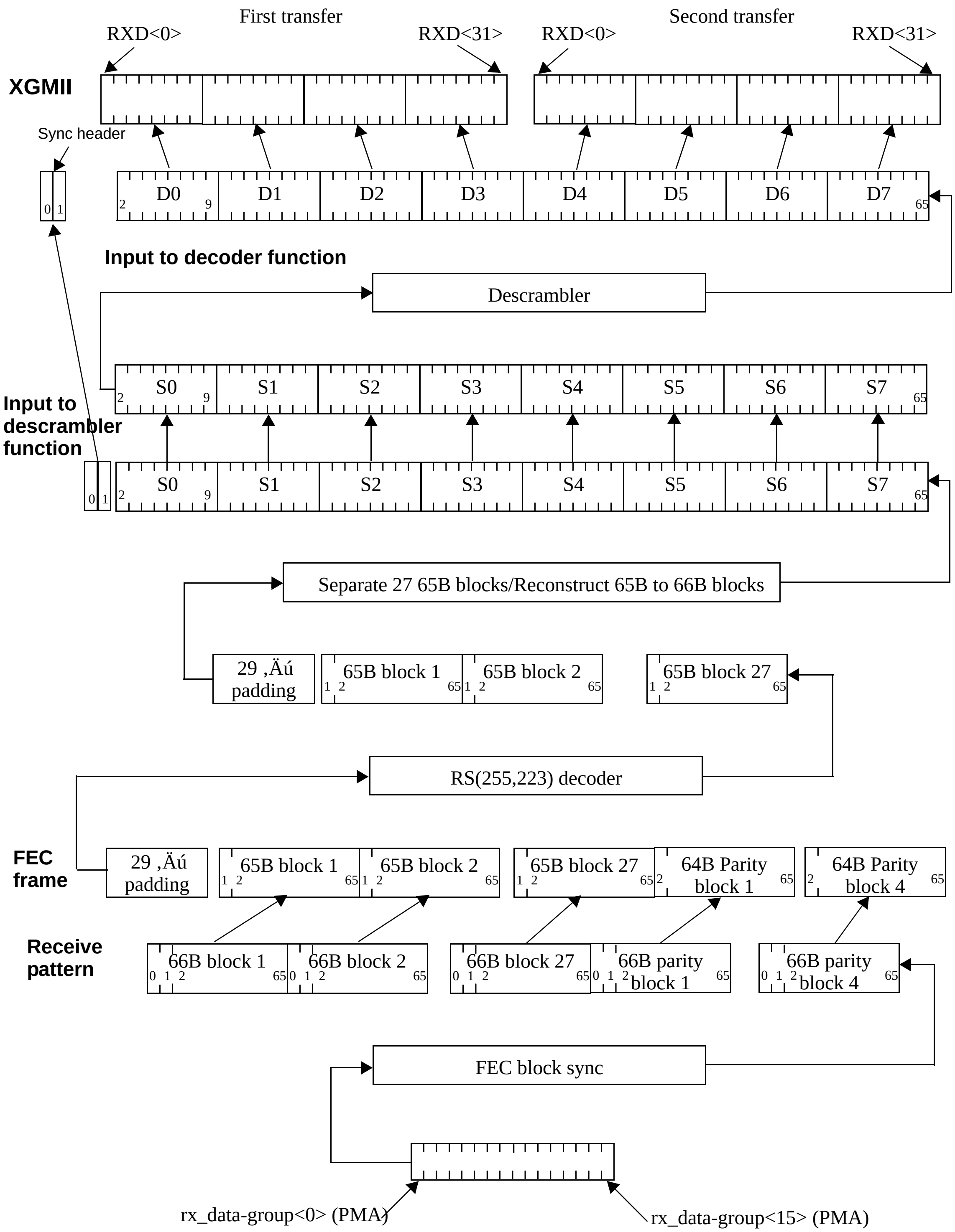


Figure 92–20—PCS Receive bit ordering

The incoming sync header pattern is 27 conventional (Clause 49) sync headers (binary 01 or 10), and then binary 00, 11, 11, and finally binary 00. The state diagram performs a search for this pattern, and when it finds a perfect match of two full codewords (62 blocks), it then asserts codeword lock.

When in codeword lock, the state diagram accumulates the appropriate contents of the 31 blocks that constitute a codeword in an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword.

When in codeword lock, the state diagram continues to check for sync header validity. If 16 or more sync headers in a codeword pair (62 blocks) are invalid, then the state diagram deasserts codeword lock. In addition, if the persist_dec_fail signal becomes set, then codeword lock is deasserted (this check insures that certain false-lock cases are not persistent.)

92.2.3.2.1 Constants

All the relevant constants defined in Subclause @@49.2.13.2.1@@ are inherited. In addition, the following items are defined.

SH_CW_PATTERN[0..30]
TYPE: array of 8-bit unsigned
31 element array of codeword sync header bit counts, where each element is set to the value 1 except for:
Value:
SH_CW_PATTERN[27]=0
SH_CW_PATTERN[28]=2
SH_CW_PATTERN[29]=2
SH_CW_PATTERN[30]=0

92.2.3.2.2 Variables

cword_lock
See Subclause 92.2.3.1.1.

decode_success
See Subclause 92.2.3.1.1.

persist_dec_fail
See Subclause 92.2.3.1.1.

reset
This variable is inherited from @@Subclause 49.2.13.2.2@@.

sh_valid[i]
TYPE: boolean
Indication that is set true if received block rx_coded has valid sync header bits for the supposed current position in the FEC codeword. That is, sh_valid[i] is asserted if (rx_coded<0> + rx_coded<1>) = SH_CW_PATTERN[i mod 31] and de-asserted otherwise.
TYPE: boolean array

signal_ok
This variable is inherited from @@Subclause 49.2.13.2.2@@.

slip_done
This variable is inherited from @@Subclause 49.2.13.2.2@@.

test_sh
This variable is inherited from @@Subclause 49.2.13.2.2@@.

92.2.3.2.3 Counters

decode_failures
See Subclause 92.2.3.1.1.

FEC_cnt
Type:8 bit unsigned
This counter keeps track of the parity sync header index that is currently being tested.

sh_cnt
See Subclause 92.2.3.1.2.

sh_valid_cnt
This counter is inherited from @@Subclause 49.2.13.2.4@@.

92.2.3.2.4 Functions

Append_inbuffer()
See Subclause 92.2.3.1.3.

DecodeWhenReady()
See Subclause 92.2.3.1.3.

SLIP
This function is inherited from @@Subclause 49.2.13.2.3@@.

92.2.3.2.5 State diagram

The ONU Synchronizer shall implement the state diagram as depicted in Figure 92-21. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

92.2.3.3 FEC Decoder

The FEC decoder corrects or confirms the correctness of the 27 66-bit blocks contained in the frame based on the four 66-bit blocks of parity information. The decoder then forwards the 66-bit data blocks to the descrambler and discards the parity blocks. The FEC decoder is also responsible for setting bit <0> of sync header to the inverse of bit <1> of sync header. The handling of data leaving the FEC decoder and going to the descrambler is specified in the FEC-decoder state diagram shown in Figure 92–22.

The synchronizer state diagram accumulates a full codeword in a buffer. If the synchronizer is locked, then the FEC decoding process is triggered. The FEC algorithm then processes the buffer. The algorithm produces two outputs: the decode_success signal and (if successful) the corrected buffer. The data portion of the buffer is then read out to the descrambler logic in 66-bit blocks, as normal. Note that the rate of 66-bit transfers is lower then normal here. This is corrected in the idle insertion step (see Figure 92–27).

If the decode_success is false, then a counter is incremented. If there are three decoding failures in a row, then the Persist_dec_fail signal is asserted. This signal will then reset the synchronizer.

Editors' Note 92-3 (to be removed prior to release):* decode_success *is set to FALSE in Codeword lock state diagram but is never set TRUE.

comment entered, need instructions on how to modify state diagram.

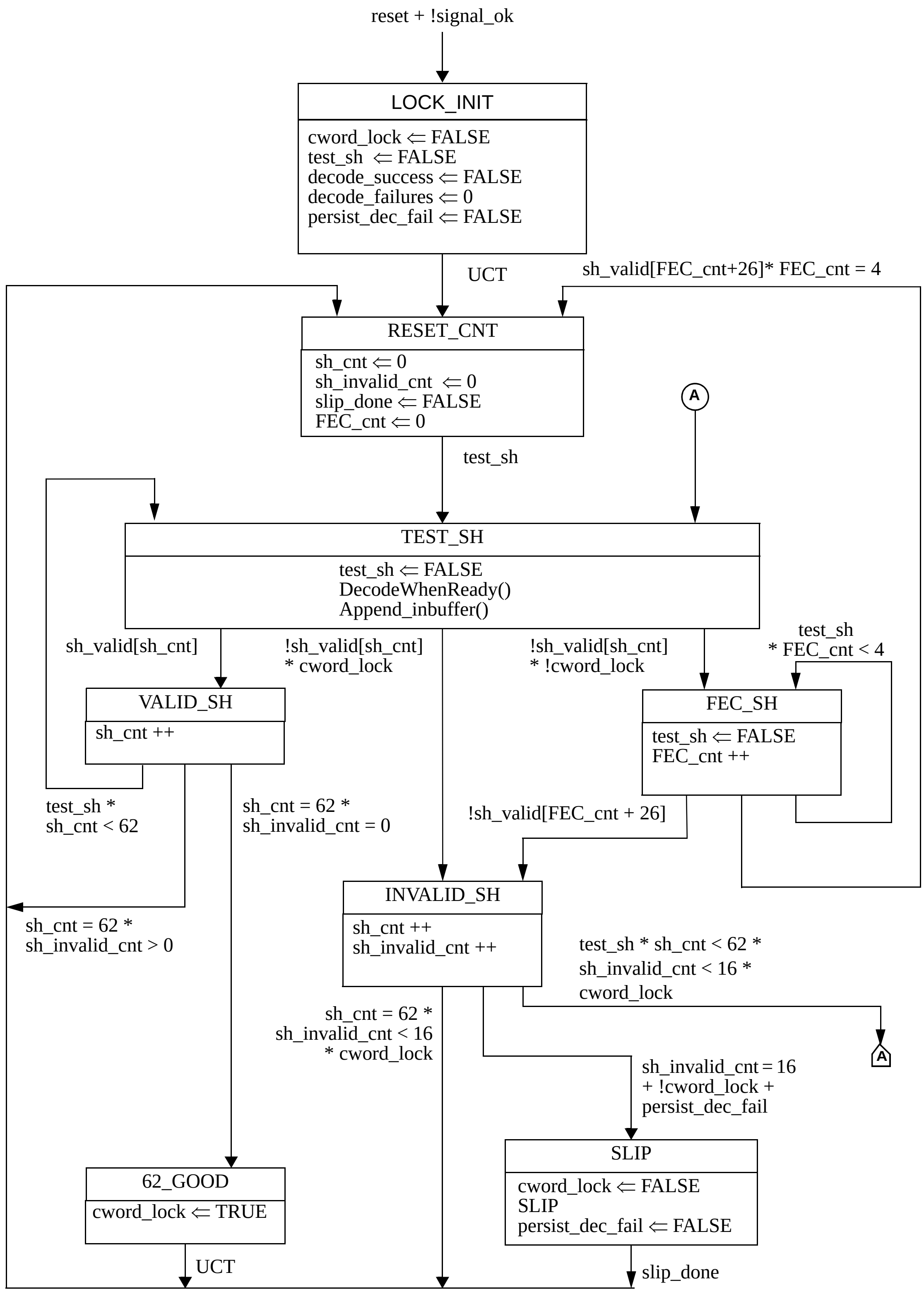


Figure 92–21—Codeword lock state diagram

The FEC decoder provides a user option to indicate an uncorrectable FEC block (due to an excess of symbols containing errors) to the PCS layer. If this option is set to be true, the FEC decoder will check for the value of decode_failures. If the variable decode_failures is set to be 1, then all sync headers for the received payload blocks of the FEC codeword to take a value of {SH.0,SH.1} = 00. However, the data blocks are nevertheless passed to the descrambler to maintain descrambling synchronization.

92.2.3.3.1 Variables

decode_done
TYPE: boolean
Indication that is transiently set when the FEC decoder algorithm has completed its processing and the corrected data is present in the output buffer.

decode_success
See Subclause 92.2.3.1.1.

mark_uncorrectable
TYPE: boolean
Control variable that is set to true if the uncorrectable errors are to be marked.

outbuffer[]
TYPE:
An array of 2040 bits.

persist_dec_fail
See Subclause 92.2.3.1.1.

rx_code_corrected
Type: 66-bit vector
The next block of data to be sent to the scrambler.

92.2.3.3.2 Counters

decode_failures
See Subclause 92.2.3.1.2.

92.2.3.3.3 Functions

All the relevant functions defined in Subclause @@49.2.13.2.3@@ are inherited. In addition, the following items are defined.

BlockFromGearbox
See Subclause 92.2.3.1.3.

BlockToDescrambler
Function that sends the next rx_coded_corrected<0..65> block to the scrambler. It does not return until the transfer is completed.

Flush_inbuffer()
See Subclause 92.2.3.1.3.

Read_outbuffer(i)

Passes output buffer contents to the descrambler, with the appropriate format.

```
Read_outbuffer[i]
{
   int offset = 29+i*65
   for(j=0, j<65, j++) {
      rx_coded_corrected<j+1> = outbuffer[j+offset]
   }
   if (!decode_success AND mark_uncorrectable) {
      rx_coded_corrected<0>=rx_coded_corrected<1>
   } else {
   rx_coded_corrected<0>=!rx_coded_corrected<1>
   }
   BlockToDescrambler()
}
```

SLIP

This function is inherited from @@Subclause 49.2.13.2.3@@.

92.2.3.3.4 State diagrams

The body of this Subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in Subclause @@21.5@@. State diagram variables follow the conventions of Subclause @@21.5.2@@ except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

The FEC Decoding function shall be implemented in the PCS as depicted in Figure 92–22. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

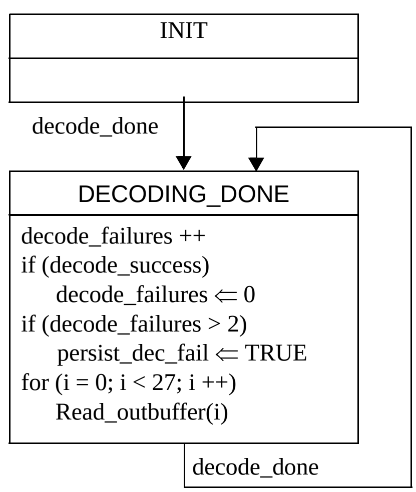


Figure 92–22—FEC Decoder state diagram

92.2.3.4 BER Monitor control

The following objects apply to 10G-EPON PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

The BER monitor is described in Figure 92–25.

The body of this Subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in Subclause @@21.5@@. State diagram variables follow the conventions of Subclause @@21.5.2@@ except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.‘

92.2.3.4.1 Variables

BER_Monitor_Interval
: Indicates the time window associated with the BER monitor function. The timers in the BER monitor state diagram depend on this configurable variable. This value is reflected in MDIO register 3.74.

ber_test_sh
: This variable is inherited from @@Subclause 49.2.13.2.2@@.

BER_Threshold
: Indicates the threshold value of invalid sync headers associated with the BER monitor function. When BER_Threshold bad sync headers are encountered within the BER Monitor_Interval period, the BER Monitor raises the hi_ber flag. When the number of bad sync headers encountered within the BER_Monitor_interval period less than the BER_Threshold, the hi_ber flag is turned off. This value is reflected in MDIO register 3.74.

hi_ber
: This variable is inherited from @@Subclause 49.2.13.2.2@@.

reset
: This variable is inherited from @@Subclause 49.2.13.2.2@@.

ber_test_sh
: This variable is inherited from @@Subclause 49.2.13.2.2@@.

92.2.3.4.2 Timers

state diagram timers follow the conventions of Subclause @@14.2.3.2@@.

interval_timer
: Timer that is triggered every BER_monitor_interval us +1%, -25%.

92.2.3.4.3 Counters

ber_cnt
: This counter is inherited from @@Subclause 49.2.13.2.4@@.

92.2.3.4.4 State diagrams

TThe BER Monitor state machine is present only in the ONU. It is shown in Figure 92–25.

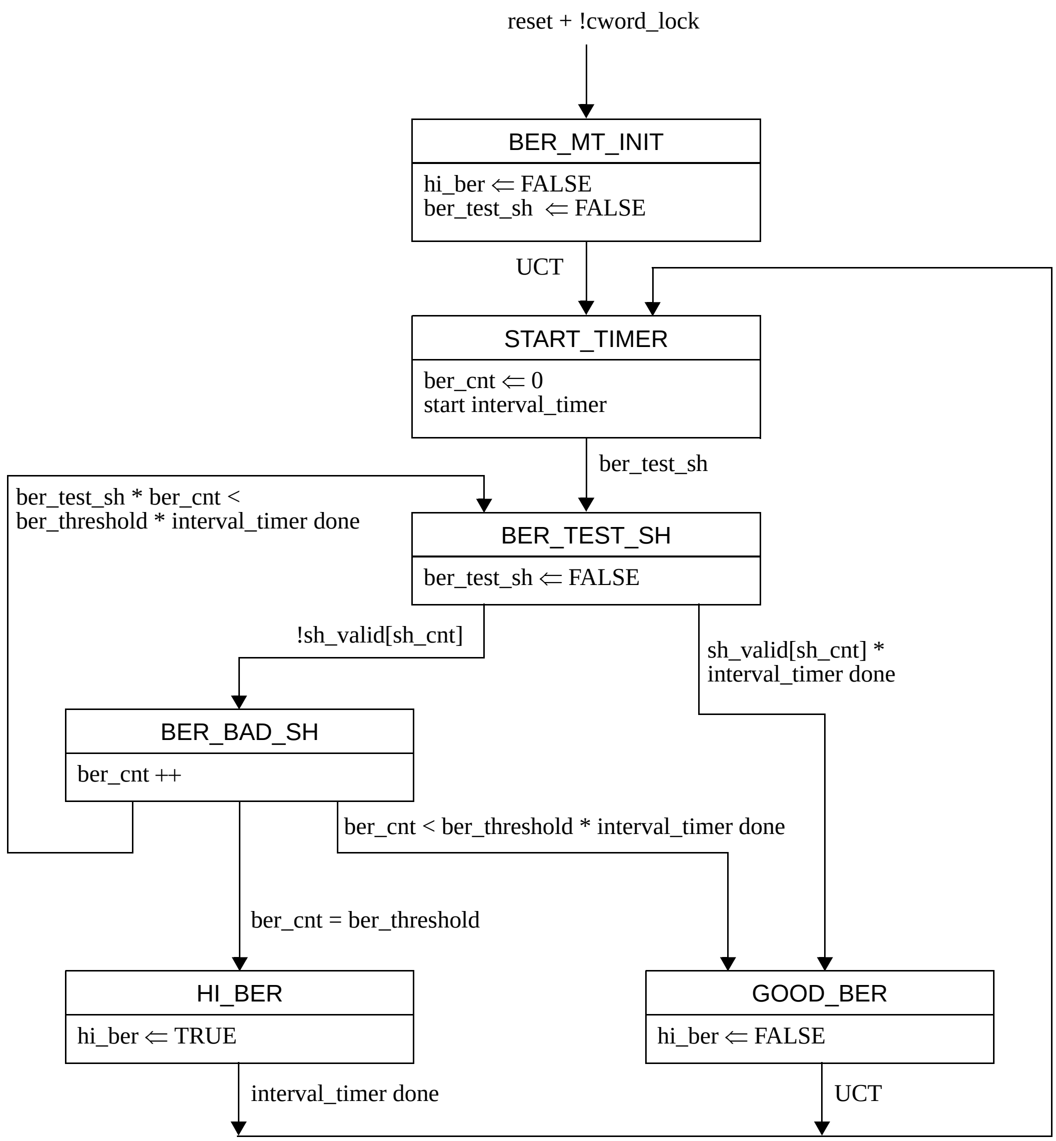


Figure 92–25—BER Monitor state diagram (ONU only)

92.2.3.5 Descrambler

See Subclause @@49.2.10@@ Descrambler.

92.2.3.6 66B/64B Decode

See Subclause @@49.2.11@@ Receive process.

92.2.3.7 Idle Insertion

The receiving PCS must insert the IDLE control characters that need to take the place of the removed FEC parity bytes. The Idle Insertion function is implemeted as two asynchronous processes: input process and the output process. The input process (see Figure 92–26) receives 72-bit vectors from 64B/66B decoder and writes them into Idle Insertion FIFO (called FIFO_II). The output process (see Figure 92–27) reads 72-bit vectors from the FIFO_II and transfers them to XGMII. The input process operates at a slower rate than the normal XGMII rate due to the fact that the FEC parity blocks are removed by the FEC decoder and not put through the descrambler and 64B/66B decoder. The output process operates at the nominal XGMII rate. To match the input and output rates, the output process sometimes inserts additional 72-bit vectors containing IDLE codes. The additional blocks are inserted between MAC frames and not necessarily in the same locations where parity blocks have been removed.

The body of this Subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in Subclause @@21.5@@. State diagram variables follow the conventions of Subclause @@21.5.2@@ except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

92.2.3.7.1 Constants

FEC_DSize
This constant is defined in Subclause 92.2.2.1.1.

FEC_PSize
This constant is defined in Subclause92.2.2.1.1.

92.2.3.7.2 Variables

ExcessIdleCount
TYPE: 16-bit signed
Counts the number of 72-bit idle vectors that need to be inserted by the receiving PCS to take the place of removed FEC parity vectors.

FIFO_II
TYPE: Array of 72-bit vectors received from 64B/66B decoder.
This FIFO is internal to the Idle Insertion function and is shared by input on output processes of Idle Insertion. Upon initialization, all elements of this array are set to contain 72-bit vectors representing /I/ characters. FIFO_II is a zero-based array of size sufficient to hold maximum size frame.

FrameReadyCount
TYPE: 16-bit unsigned
Counts the number of frames that are waiting in the receive FIFO.

rx_raw_in<71:0>
TYPE: 72-bit binary
Vector received from the output of the 64B/66B decoder containing two successive XGMII transfers. RXC<0> through RXC<3> for the first transfer are placed in rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are placed in rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are placed in rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

rx_raw_out<71:0>
TYPE: 72-bit binary

72-bit vector passed from the Idle Insertion process to XGMII. The vector is mapped to two XGMII transfers as follows:

Bits rx_raw<3:0> are mapped to RXC<3:0> for the first transfer;
Bits rx_raw<7:4> are mapped to RXC<3:0> for the second transfer;
Bits rx_raw<39:8> are mapped to RXD<31:0> for the first transfer;
Bits rx_raw<71:40> are mapped to RXD<31:0> for the second transfer.

RxVectorCount
TYPE: 16-bit unsigned
Counts the number of of 72-bit vectors removed from the FIFO_II.

92.2.3.7.3 Functions

AddToFIFO(rx_raw_in<71:0>)
This function appends a new 72-bit vector to the end of FIFO_II.

```
AddToFIFO(tx_raw_in<71:0>)
{
   FIFO_II_size++
   FIFO_II[FIFO_II_size-1] = tx_raw_in<71:0>
}
```

InitializeFIFO()
This function sets all the elements of FIFO_II array to 72-bit vectors representing /I/ characters.

SendFromFIFO()
This function return the value of the first element (72-bit vector) in the FIFO_II and removes this element from the FIFO_II.

```
SendFromFIFO()
{
   ret_vector = FIFO_II[0]
   // shift FIFO forward
   FIFO_II[0] = FIFO_II[1]
   FIFO_II[1] = FIFO_II[2]
   ...
   FIFO_II[FIFO_II_size-2] = FIFO_II[FIFO_II_size-1]
   FIFO_II_size--
   return ret_vector
}
```

T_TYPE(rx_raw)
This function is defined in @@49.2.13.2.3@@.

92.2.3.7.4 Messages

DECODER_UNITDATA.indicate(rx_raw_in<71:0>)
A signal sent by the PCS Receive process conveying the next code-group received and decoded.

DUDI
Alias for DECODER_UNITDATA.indicate(rx_raw_in<71:0>).

92.2.3.7.5 State diagrams

The PCS Idle Insertion function shall implement the input process state diagram as shown in Figure 92–26 and the output process state diagram, as shown in Figure 92–27. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

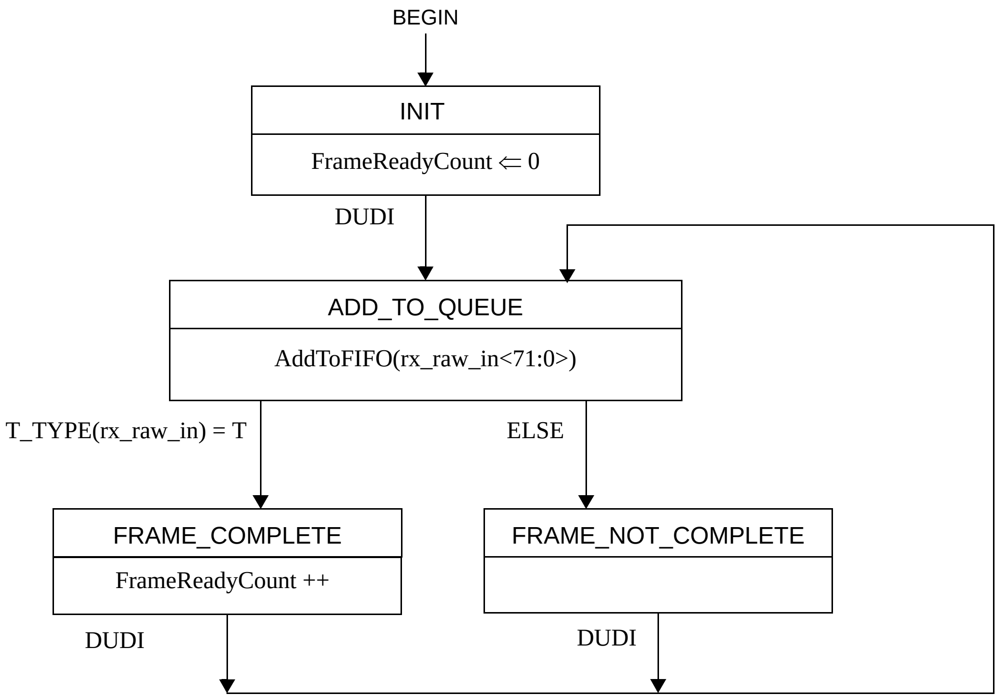


Figure 92–26—PCS Idle Insertion, input process state diagram

92.3 Extensions to PMA for 10GBASE-PR and 10/1GBASE-PRX

The 10GBASE-PR PMA is derived from the 10GBASE-R PMA defined in Clause 51. This clause specifies 10GBASE-R extensions necessary to support P2MP operation. The 10/1GBASE-PRX PMA conceptually consists of a combination of transmit and receive functions specified for 10GBASE-PR and 1000BASEPX, as shown in Table 92-5.

Table 92–5—Derivation of PMA transmit and receive functions for 10GBASE-PR and 10/1GBASE-PRX

PMA	Transmit Function	Receive Function
10GBASE-PR-U	As specified in Clause 51 with extensions defined in @@92.3.1@@ below.	
10/1GBASE-PRX-U	Identical to 1000BASE-PX-U. See @@65.3.1@@.	As specified in Clause 51 with extensions defined in @@92.3.1@@ below
10GBASE-PR-U	As specified in Clause 51 with extensions defined in @@92.3.2@@ below.	
10/1GBASE-PRX-D	Identical to 10GBASE-PR-D.	Identical to 1000BASE-PX-D. See @@65.3.2@@.

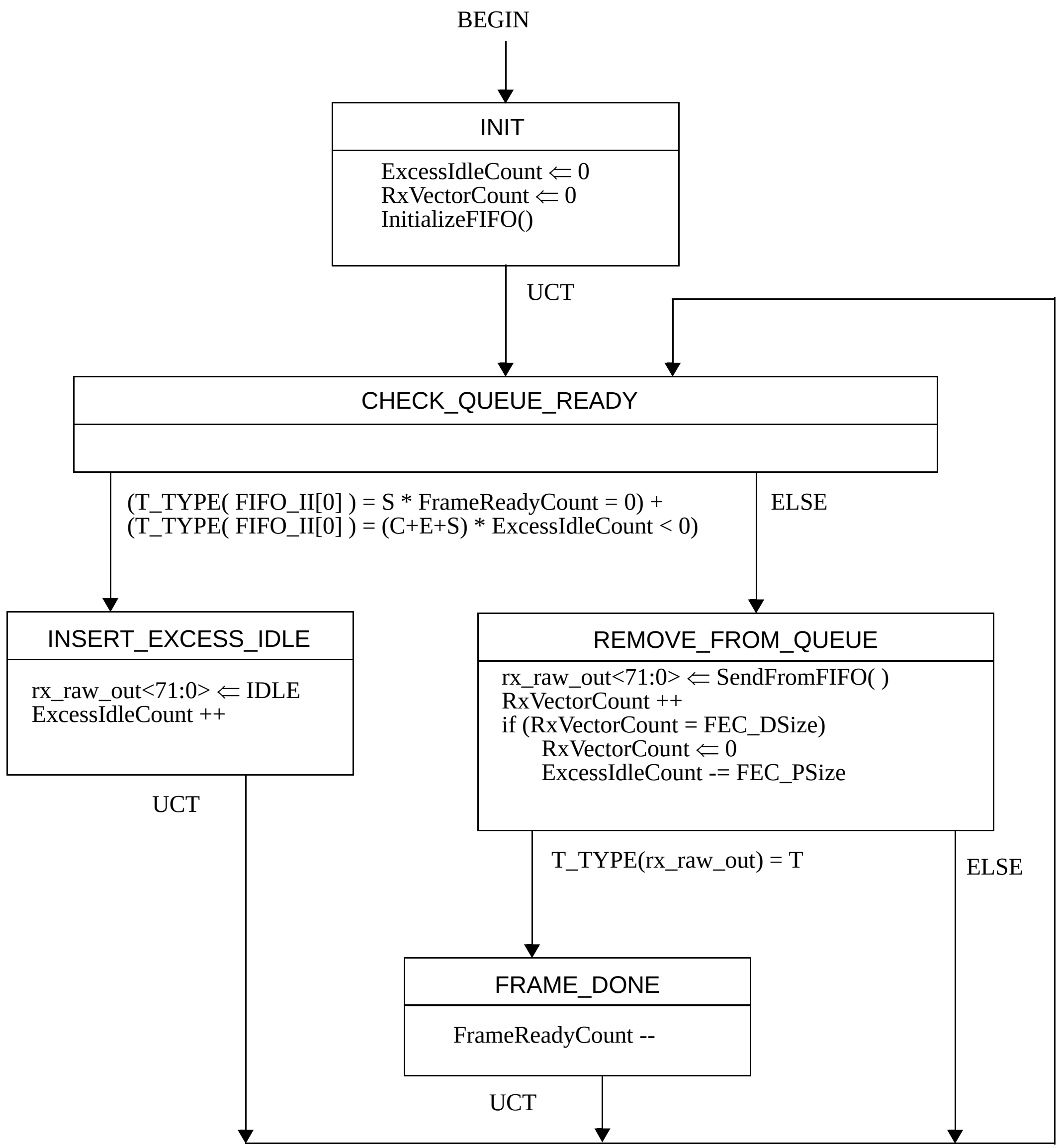


Figure 92–27—PCS Idle Insertion, output process state diagram

92.3.1 Extensions for 10GBASE-PR-U and 10/1GBASE-PRX-U

92.3.1.1 Physical Medium Attachment (PMA) sublayer interfaces

In addition to the primitives of Clause 51, the following primitive is defined:

PMD_SIGNAL.request(tx_enable)

This primitive controls PMD emission of light. It is generated by the PCS's data detector (see 92.2.2.8.4) and the effect of its receipt is defined in 91.3.1.4. This primitive is received from the PCS and passed in timely fashion and without modification to the PMD. It takes the following parameter:

tx_enable

The tx_enable parameter can take one of two values, ON or OFF.

92.3.1.2 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU TX clock tracks the ONU RX clock and in turn locks to OLT TX clock. Jitter transfer masks are defined in Subcause@@91.8@@.

For the 10/1GBASE-PRX-U devices, the received clock PMA_RX_CLK is 644.53125 MHz (10.3125 GBd/16), however, the transmit clock PMA_TX_CLK is 125 MHz (1.25GBd/10). The loop timing is achieved by multiplying the PMA_RX_CLK by 32 and dividing by 165.

92.3.2 Extensions for 10GBASE-PR-D and 10/1GBASE-PRX-D

92.3.2.1 CDR lock timing measurement for the upstream direction

CDR lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase and frequency lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when electrical signal after the PMD at TP4, as illustrated in @@Figure 91-3@@ and @@Figure 91-4@@, reaches the conditions specified in @@Subclause 91.9.16@@ for receiver settling time to the moment when the phase and frequency are recovered and jitter is maintained for a network with BER of no more than 10^{-3}.

A PMA instantiated in an OLT becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (0x55…) at TP4.

92.3.2.1.1 Test specification

@@Figure 91-3@@ and @@Figure 91-4@@ illustrate the tests setup for the OLT PMA receiver (upstream) T_{CDR} time. The test assumes that there is an optical PMD transmitter at the ONU with well known parameters, having a fixed known T_{ON} time as defined in @@Subclause 91.9.15@@, and an optical PMD receiver at the OLT with well-known parameters, having a fixed known $T_{receiver\_settling}$ time as defined in @@Subclause 60.7.13.2@@. After $T_{ON} + T_{receiver\_settling}$ time, the parameters at TP4 reach within 15% of their steady state values.

Measure T_{CDR} as the time from the TX_ENABLE assertion, minus the known $T_{ON} + T_{receiver\_settling}$ time, to the time the electrical signal at the output of the PMA reaches up to the phase difference from the input signal of the transmitting PMA assuring BER of 10^{-3}, and maintaining its jitter specifications. The signal throughout this test is the synchronization pattern, as illustrated in Figure 92-15.

A non-rigorous way to describe this test setup would be (using a transmitter PMD at the ONU, with a known T_{ON} time and a receiver PMD at the OLT, with a known $T_{receiver\_settling}$ time):

For a tested PMA receiver with a declared T_{CDR} time, measure the phase and jitter of the recovered PMA receiver signal after T_{CDR} time from the TX_ENABLE trigger minus the reference $T_{ON} + T_{receiver\_settling}$ time, reassuring synchronization to the ONU PMA input signal and conformance to the specified steady state phase, frequency, and jitter values for BER of 10^{-3}.

92.4 Protocol implementation conformance statement (PICS) proforma for Clause 92, Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) for 10GBASE-PR-D1, 10GBASE-PR-D2, 10GBASE-PR-D3, 10/1GBASE-PRX-D1, 10/1GBASE-PRX-D2, 10/1GBASE-PRX-D3, 10GBASE-PR-U1, 10GBASE-PR-U3, 10/1GBASE-PRX-U1, 10/1GBASE-PRX-U2, 10/1GBASE-PRX-U3 for point-to-multipoint media[a]

92.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 92, Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point–to–point media, types 10GBASE–PR and 10/1GBASE–PRX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

92.4.2 Identification

92.4.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

[a]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this Subclause so that it can be used for its intended purpose and may further publish the completed PICS.

92.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3–2008, Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point–to–point media, types 10GBASE–PR and 10/1GBASE–PRX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3–2008)	
Date of Statement	

92.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	92.1.1	Device supports functionality required for OLT	O.1	Yes [ ] No [ ]
*ONU	ONU functionality	92.1.1	Device supports functionailty required for ONU	O.1	Yes [ ] No [ ]
*FECEncoder	Operation of forward error correction encoder	92.1.2.4	Device supports FEC encoding for multipoint optical links	O	Yes [ ] No [ ]
*FEC-Decoder	Operation of forward error correction decoder	92.2.3.2	Device supports FEC decoding for multipoint optical links	O	Yes [ ] No [ ]

92.4.4 PICS proforma tables for Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point–to–multipoint media, types 10GBASE–PR and 10/1GBASE–PRX

92.4.4.1 Operating modes of OLT MACs

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Unidirectional mode	92.1.3	Device operates in unidirectional transmission mode	OLT:M	Yes [ ]
OM2	Dual-rate mode	92.1.2.3	Device operates in dual-rate mode	OLT:O	Yes [ ] No [ ]

92.4.4.2 ONU and OLT variables

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	enable variable	92.1.6.2	True for ONU MAC, TRUE for OLT MAC if enabled, FALSE for OLT MAC if not enabled	M	Yes [ ]
FS2	mode variable	92.1.6.2.1	0 for ONU MAC, 0 or 1 for enabled OLT MAC	M	Yes [ ]
FS3	logical_link_id variable	92.1.6.2.1	Set to 0x7FFE until ONU MAC is registered Set to any value for enabled OLT MAC. Set to any value other then 0x7FFE for registered ONU MAC	M	Yes [ ]

92.4.4.3 Preamble mapping and replacement

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	CRC-8 generation	92.1.6.2.2	CRC calculation produces same result as serial implementation	M	Yes [ ] No [ ]
PM2	CRC-8 initial value	92.1.6.2.2	CRC shift register initialized to 0x00 before each new calculations	M	Yes [ ] No [ ]
PM3	SLD parsing	92.1.6.2.3.1	If SLD is not found then discard packet	M	Yes [ ] No[ ]
PM4	SLD replacement	92.1.6.2.3.1	Replace SLD with preamble	M	Yes [ ] No [ ]
PM5	LLID matching	92.1.6.2.3.2	If LLID does not match then discard packet	M	Yes [ ] No [ ]
PM6	LLID Replacement	92.1.6.2.3.2	Replace LLID with preamble	M	Yes [ ] No [ ]
PM7	CRC-8 checking	92.1.6.2.3.3	If CRC does not match then discard packet	M	Yes [ ] No [ ]
PM8	CRC-8 replacement	92.1.6.2.3.3	Replace CRC with preamble	M	Yes [ ] No [ ]

92.4.4.4 Data detection

Item	Feature	Subclause	Value/Comment	Status	Support
DD1	Buffer depth	92.2.2.5	Depth sufficient to turn on laser and send laser synchronization pattern, Burst Delimiter pattern and a predefined number of IDLE control character (receiver settle).	ONU:M	Yes [ ] No [ ]
DD2	OLT laser control	92.2.2.5.3	Always takes the value ON	OLT:M	Yes [ ] No [ ]
DD3	State diagrams	92.2.2.5.6	Meets the requirements of Figure 92–18	ONU:M	Yes [ ] No[ ]

92.4.4.5 Alignment and IDLE control character deletion

Item	Feature	Subclause	Value/Comment	Status	Support
AIC1	IDLE control character deletion	92.2.2.1	If the minimum IPG was transmitted after a frame, then 4 IDLE control character are deleted for every 27 vectors transmitted.	ONU:M	Yes [ ] No [ ]
AIC2	Alignment and Idle Detection function implementation in ONU	92.2.2.1	Meets the requirements of Figure 92–11	ONU:M	Yes [ ] No [ ]
AIC3	Alignment and Idle Detection function implementation in OLT	92.2.2.1	Meets the requirements of Figure 92–10	OLT:M	Yes [ ] No [ ]

92.4.4.6 FEC requirements

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	FEC Coding Choice	92.2.2.4	Reed-Solomon (RS) code (255,223)	FEC:M	Yes [ ] No [ ]
FE2	Uncorrectable block indication	92.2.3.2	Mark all code-groups in an uncorrectable block by setting all sync headers for the received payload blocks of the FEC codeword to the value of {SH.0,SH.1} = 00.	FEC:O	Yes [ ] No [ ]

92.4.4.7 FEC state machines

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Transmit		Meets the requirements of Figure 92–12	FEC:M	Yes [ ]
SM2	Receive synchronization	92.2.3.1	Meets the requirements of Figure 92–21	FEC:M	Yes [ ]
SM3	Bit stream forming process during receive	92.2.3.1	Meets the requirements of Figure 92–21.	FEC:M	Yes [ ]
SM4	Receive	92.2.3.3	Meets the requirements of Figure 92–22	FEC:M	Yes [ ]

92.4.4.8 PMA

Item	Feature	Subclause	Value/Comment	Status	Support
BMC1	Loop Timing	92.3.1.2	ONU RX clock tracks OLT TX clock	ONU:M	Yes [ ] No [ ]

92.4.4.9 Delay variation

Item	Feature	Subclause	Value/Comment	Status	Support
DV1	Delay variation	@@92.3.3 @@	Combined delay variation through RS, PCS, and PMA sublayers is limited to 16 bit times	M	Yes [ ] No [ ]

Annex 92A

(informative)

FEC Frame Encoding example

Editors' Note 92-1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

Editing instructions are shown in 8 point arial Bold red italic font. Four editing instructions are used: ***change***, ***delete***, ***insert****, and* ***replace****.*
Change *is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using strikethrough (to remove old material) or underscore (to add new material).*
Delete *removes existing material.*
Insert *adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction.*
Replace *is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions*
To simplify the addition of new tables, tables in this amendment clause are numbered based on their relationship to tables in the base document (IEEE P802.3ay D2.2). For example, Table 45-BB in this amendment would be renumbered Table-CC when the amendment is merged with IEEE P802.3ay D2.2. Continuing the example, a Table-AAb would then be renumbered Table-DD. All original table numbers in the base document can then be incremented after the merge.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.:

Editors' Note 92-2 (to be removed prior to release): Draft revision history for Clause (informative)

Draft	*Date*	*Comment*
D1.3	*May 2008*	*Initial draft for Task Force review due to comment resolution from April 2008 meeting.*
D1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting.*

92A.2 Introduction and rationale

This Annex provides an example of FEC frame encoding with RS (255,223) code. See @@Subclause 92.2.2.4.3@@ for the format of the FEC frame.

92A.3 64B/66B Block Input

Table 92A-1 provides an example of a 64B/66B block stream received at the input to the RS (255,223) encoder. The example shows a stream of 27 scrambled 64B/66B blocks generated from the output of PCS layer when the link was sending out IDLEs.

The 66-bit blocks in the Table 92A-1 are transmitted from left to right within each row and from top to bottom between rows. The 64 bit payload portion of the 66-bit block is described as a series of hexadecimal octets - the leftmost octet of each payload portion is transmitted first. Bits within each octet of the payload are transmitted in least-significant-bit-first order (ie. the rightmost bit of each octet is transmitted first).

Thus, the first ten bits transmitted will be: 10 0100 0000 …

Table 92A-1—Example 64B/66B block stream at the input to FEC encode

Sync [0:1]	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]
10	02-57-78-ee-77-cb-80-37	10	b5-5a-dc-1f-b6-59-f3-3a	10	7b-aa-d3-a1-fb-f0-3e-05	10	67-33-ff-71-41-48-8d-63
10	6b-dc-63-c3-90-00-60-1c	10	0e-c7-0d-73-0c-07-92-be	10	3b-b1-cf-78-c3-d5-22-89	10	66-df-89-9c-13-38-cb-de
10	ad-2e-ee-2b-0f-7a-6c-40	10	31-bf-92-0a-48-29-5e-8c	10	e7-ee-3e-0f-63-0b-46-01	10	22-4a-39-2f-2d-09-a0-14
10	a1-73-b8-e4-ae-50-6b-d8	10	a2-b6-3a-8e-2e-fc-3a-96	10	83-fd-46-a7-3b-2a-26-ad	10	3b-06-88-7d-7e-85-b7-2a
10	38-9f-34-a2-00-42-e5-fa	10	33-d2-29-70-f5-8c-02-db	10	ee-dd-86-54-5e-fd-02-f8	10	43-b4-2c-78-09-2aba-19
10	73-b6-f5-f8-24-d1-bd-b6	10	bb-44-0b-cd-9f-aa-78-6b	10	ea-62-61-c3-9f-97-1c-19	10	74-4a-46-f1-52-48-41-73
10	4f-30-61-eb-98-22-55-8d	10	aa-c8-3c-c9-cc-01-51-34	10	58-15-a4-1b-1d-e8-db-b2		

92A.4 66-bit Block Input in Binary format

Table 92A-2—Example 64B/66B block stream at the input to FEC encoder (binary)

Sync [0:1]	64bit payload (transmitted from left to right)
10	0100 0000 1110 1010 0001 1110 0111 0111 1110 1110 1101 0011 0000 0001 1110 1100
10	1010 1101 0101 1010 0011 1011 1111 1000 0110 1101 1001 1010 1100 1111 0101 1100
10	1101 1110 0101 0101 1100 1011 1000 0101 1101 1111 0000 1111 0111 1100 1010 0000
10	1110 0110 1100 1100 1111 1111 1000 1110 1000 0010 0001 0010 1011 0001 1100 0110
10	1101 0110 0011 1011 1100 0110 1100 0011 0000 1001 0000 0000 0000 0110 0011 1000
10	0111 0000 1110 0011 1011 0000 1100 1110 0011 0000 1110 0000 0100 1001 0111 1101
10	1101 1100 1000 1101 1111 0011 0001 1110 1100 0011 1010 1011 0100 0100 1001 0001
10	0110 0110 1111 1011 1001 0001 0011 1001 1100 1000 0001 1100 1101 0011 0111 1011
10	1011 0101 0111 0100 0111 0111 1101 0100 1111 0000 0101 1110 0011 0110 0000 0010
10	1000 1100 1111 1101 0100 1001 0101 0000 0001 0010 1001 0100 0111 1010 0011 0001
10	1110 0111 0111 0111 0111 1100 1111 0000 1100 0110 1101 0000 0110 0010 1000 0000
10	0100 0100 0101 0010 1001 1100 1111 0100 1011 0100 1001 0000 0000 0101 0010 1000
10	1000 0101 1100 1110 0001 1101 0010 0111 0111 0101 0000 1010 1101 0110 0001 1011
10	0100 0101 0110 1101 0101 1100 0111 0001 0111 0100 0011 1111 0101 1100 0110 1001
10	1100 0001 1011 1111 0110 0010 1110 0101 1101 1100 0101 0100 0110 0100 1011 0101
10	1101 1100 0110 0000 0001 0001 1011 1110 0111 1110 1010 0001 1110 1101 0101 0100
10	0001 1100 1111 1001 0010 1100 0100 0101 0000 0000 0100 0010 1010 0111 0101 1111
10	1100 1100 0100 1011 1001 0100 0000 1110 1010 1111 0011 0001 0100 0000 1101 1011
10	0111 0111 1011 1011 0110 0001 0010 1010 0111 1010 1011 1111 0100 0000 0001 1111
10	1100 0010 0010 1101 0011 0100 0001 1110 1001 0000 0101 0100 0101 1101 1001 1000
10	1100 1110 0110 1101 1010 1111 0001 1111 0010 0100 1000 1011 1011 1101 0110 1101
10	1101 1101 0010 0010 1101 0000 1011 0011 1111 1001 0101 0101 0001 1110 1101 0110
10	0101 0111 0100 0110 1000 0110 1100 0011 1111 1001 1110 1001 0011 1000 1001 1000
10	0010 1110 0101 0010 0110 0010 1000 1111 0100 1010 0001 0010 1000 0010 1100 1110
10	1111 0010 0000 1100 1000 0110 1101 0111 0001 1001 0100 0100 1010 1010 1011 0001
10	0101 0101 0001 0011 0011 1100 1001 0011 0011 0011 1000 0000 1000 1010 0010 1100
10	0001 1010 1010 1000 0010 0101 1101 1000 1011 1000 0001 0111 1101 1011 0100 1101

92A.5 RS(255, 223) Input Buffer in Binary Format

The input buffer to the RS function begins with 29 ‘0’ bits followed by the 27 65-bit inputs as illustrated in @@Figure 92-12@@ and @@Figure 92-13@@:

Table 92A-3—Input buffer to the FEC encoder (binary)

0000 0000 0000 0000 0000 0000 0000 0001 0000 0011 1010 1000 0111 1001 1101 1111
1011 1011 0100 1100 0000 0111 1011 0001 0101 1010 1011 0100 0111 0111 1111 0000

1101 1011 0011 0101 1001 1110 1011 1000 1101 1110 0101 0101 1100 1011 1000 0101
1101 1111 0000 1111 0111 1100 1010 0000 0111 0011 0110 0110 0111 1111 1100 0111
0100 0001 0000 1001 0101 1000 1110 0011 0011 0101 1000 1110 1111 0001 1011 0000
1100 0010 0100 0000 0000 0001 1000 1110 0000 1110 0001 1100 0111 0110 0001 1001
1100 0110 0001 1100 0000 1001 0010 1111 1010 1101 1100 1000 1101 1111 0011 0001
1110 1100 0011 1010 1011 0100 0100 1001 0001 0011 0011 0111 1101 1100 1000 1001
1100 1110 0100 0000 1110 0110 1001 1011 1101 1010 1101 0101 1101 0001 1101 1111
0101 0011 1100 0001 0111 1000 1101 1000 0000 1001 0001 1001 1111 1010 1001 0010
1010 0000 0010 0101 0010 1000 1111 0100 0110 0010 1110 0111 0111 0111 0111 1100
1111 0000 1100 0110 1101 0000 0110 0010 1000 0000 0010 0010 0010 1001 0100 1110
0111 1010 0101 1010 0100 1000 0000 0010 1001 0100 0010 0001 0111 0011 1000 0111
0100 1001 1101 1101 0100 0010 1011 0101 1000 0110 1100 1000 1010 1101 1010 1011
1000 1110 0010 1110 1000 0111 1110 1011 1000 1101 0010 1100 0001 1011 1111 0110
0010 1110 0101 1101 1100 0101 0100 0110 0100 1011 0101 0110 1110 0011 0000 0000
1000 1101 1111 0011 1111 0101 0000 1111 0110 1010 1010 0000 0111 0011 1110 0100
1011 0001 0001 0100 0000 0001 0000 1010 1001 1101 0111 1101 1001 1000 1001 0111
0010 1000 0001 1101 0101 1110 0110 0010 1000 0001 1011 0110 0111 0111 1011 1011
0110 0001 0010 1010 0111 1010 1011 1111 0100 0000 0001 1111 0110 0001 0001 0110
1001 1010 0000 1111 0100 1000 0010 1010 0010 1110 1100 1100 0011 0011 1001 1011
0110 1011 1100 0111 1100 1001 0010 0010 1110 1111 0101 1011 0101 1011 1010 0100
0101 1010 0001 0110 0111 1111 0010 1010 1010 0011 1101 1010 1100 0101 0111 0100
0110 1000 0110 1100 0011 1111 1001 1110 1001 0011 1000 1001 1000 0001 0111 0010
1001 0011 0001 0100 0111 1010 0101 0000 1001 0100 0001 0110 0111 0011 1100 1000
0011 0010 0001 1011 0101 1100 0110 0101 0001 0010 1010 1010 1100 0100 1010 1010
0010 0110 0111 1001 0010 0110 0110 0111 0000 0001 0001 0100 0101 1000 0001 1010
1010 1000 0010 0101 1101 1000 1011 1000 0001 0111 1101 1011 0100 1101

92A.6 RS(255, 223) Input Buffer

Table 92A-4 illustrates the 223 octets of the input buffer constructed by the RS(255, 223) encoder prior to computation of the parity octets. The octets of the buffer are formed from the input 66-bit blocks according to the procedure depicted in @@Figure 92-12@@ and @@Figure 92-13@@.

Note that in @@Figure 92-12@@ and @@Figure 92-13@@ the rightmost bit of each formed octet is the most significant, whereas Table 92A-4 lists the octets in the more typical notation ie. the least significant bit appears on the right.

Table 92A-4—223 octet input buffer within FEC encoder before computation of parity octets

	Dn	Dn -1	Dn -2	Dn -3	Dn -4	Dn -5	Dn -6	Dn -7	Dn -8	Dn -9	Dn -10	Dn -11	Dn -12	Dn -13	Dn -14	Dn -15
n= 222	0x 00	0x 00	0x 00	0x 80	0x C0	0x 15	0x 9E	0x FB	0x DD	0x 32	0x E0	0x 8D	0x 5A	0x 2D	0x EE	0x 0F
n= 206	0x DB	0x AC	0x 79	0x 1D	0x 7B	0x AA	0x D3	0x A1	0x FB	0x F0	0x 3E	0x 05	0x CE	0x 66	0x FE	0x E3
n= 190	0x 82	0x 90	0x 1A	0x C7	0x AC	0x 71	0x 8F	0x 0D	0x 43	0x 02	0x 80	0x 71	0x 70	0x 38	0x 6E	0x 98
n= 174	0x 63	0x 38	0x 90	0x F4	0x B5	0x 13	0x FB	0x 8C	0x 37	0x 5C	0x 2D	0x 92	0x C8	0x EC	0x 3B	0x 91
n= 158	0x 73	0x 02	0x 67	0x D9	0x 5B	0x AB	0x 8B	0x FB	0x CA	0x 83	0x 1E	0x 1B	0x 90	0x 98	0x 5F	0x 49
n= 142	0x 05	0x A4	0x 14	0x 2F	0x 46	0x E7	0x EE	0x 3E	0x 0F	0x 63	0x 0B	0x 46	0x 01	0x 44	0x 94	0x 72
n= 126	0x 5E	0x 5A	0x 12	0x 40	0x 29	0x 84	0x CE	0x E1	0x 92	0x BB	0x 42	0x AD	0x 61	0x 13	0x B5	0x D5
n= 110	0x 71	0x 74	0x E1	0x D7	0x B1	0x 34	0x D8	0x 6F	0x 74	0x BA	0x A3	0x 62	0x D2	0x 6A	0x C7	0x 00
n= 94	0x B1	0x CF	0x AF	0x F0	0x 56	0x 05	0x CE	0x 27	0x 8D	0x 28	0x 80	0x 50	0x B9	0x BE	0x 19	0x E9
n= 78	0x 14	0x B8	0x 7A	0x 46	0x 81	0x 6D	0x EE	0x DD	0x 86	0x 54	0x 5E	0x FD	0x 02	0x F8	0x 86	0x 68
n= 62	0x 59	0x F0	0x 12	0x 54	0x 74	0x 33	0x CC	0x D9	0x D6	0x E3	0x 93	0x 44	0x F7	0x DA	0x DA	0x 25
n= 46	0x 5A	0x 68	0x FE	0x 54	0x C5	0x 5B	0x A3	0x 2E	0x 16	0x 36	0x FC	0x 79	0x C9	0x 91	0x 81	0x 4E
n= 30	0x C9	0x 28	0x 5E	0x 0A	0x 29	0x 68	0x CE	0x 13	0x 4C	0x D8	0x 3A	0x A6	0x 48	0x 55	0x 23	0x 55
n= 14	0x 64	0x 9E	0x 64	0x E6	0x 80	0x 28	0x 1A	0x 58	0x 15	0x A4	0x 1B	0x 1D	0x E8	0x DB	0x B2	

92A.7 Parity Symbol Output

Table 92A-5 illustrates the 32 parity octets computed by the RS(255, 223) encoder for the inputs given above.

Note that in @@Figure 92-12@@ and @@Figure 92-13@@ the rightmost bit of each parity octet is the most significant, whereas Table 92A-5 lists the octets in the more typical notation ie. the least significant bit is on the right.

Table 92A-5—32 parity octets computed by FEC encoder

	Pn	Pn-1	Pn-2	Pn-3	Pn-4	Pn-5	Pn-6	Pn-7	Pn-8	Pn-9	Pn-10	Pn-11	Pn-12	Pn-13	Pn-14	Pn-15
n=31	0x 7E	0x 62	0x 35	0x FB	0x DB	0x 9F	0x 5E	0x 8E	0x FD	0x B2	0x 81	0x 3E	0x F9	0x 1D	0x 9B	0x 1A
n=15	0x 32	0x 1E	0x 70	0x CF	0x DD	0x C2	0x 2C	0x 54	0x 43	0x F1	0x 00	0x 78	0x 3C	0x 4F	0x BD	0x F4

92A.8 Parity Symbols in Binary Format

As with the input buffer, this is written with least significant bit leftmost to correspond with :

Table 92A-6—32 parity octets computed by FEC encoder (binary)

0111 1110 0100 0110 1010 1100 1101 1111 1101 1011 1111 1001 0111 1010 0111 0001
1011 1111 0100 1101 1000 0001 0111 1100 1001 1111 1011 1000 1101 1001 0101 1000
0100 1100 0111 1000 0000 1110 1111 0011 1011 1011 0100 0011 0011 0100 0010 1010
1100 0010 1000 1111 0000 0000 0001 1110 0011 1100 1111 0010 1011 1101 0010 1111

92A.9 64B/66B Parity Blocks for Transmit

Table 92A-7 illustrates the 64B/66B blocks carrying parity that are generated by the RS (255, 223) encoder for the input blocks in Table 92A-6 above. The RS (255, 223) encoder inserts the parity blocks into the transmission stream to the gearbox subsequent to its transmission of the corresponding input 66-bit blocks (as described in 92.2.3.4).

The 66-bit blocks in the Table 92A-7 are transmitted from left to right within each row and from top to bottom between rows. The 64 bit payload portion of the 66-bit block is described as a series of hexadecimal octets - the leftmost octet of each payload portion is transmitted first. Bits within each octet of the payload are transmitted in least-significant-bit-first order (ie. the rightmost bit of each octet is transmitted first).

Thus, the first 18 bits of the parity blocks transmitted will be: 00 0111 1110 0100 0110 …

Table 92A-7—64B/66B blocks carrying 32 parity octets generated by FEC encoder

Sync [0:1]	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]	**Sync [0:1]**	**64bit payload** [7:0]- [15:8]- [23:16]- [31:24]- [39:32]- [47:40]- [55:48]- [63:56]
00	7E-62-35-FB-DB-9F-5E-8E	11	FD-B2-81-3E-F9-1D-9B-1A	11	32-1E-70-CF-DD-C2-2C-54	00	43-F1-00-78-3C-4F-BD-F4

92A.10 Parity 66-bit blocks in Binary Format

Table 92A-8—64B/66B blocks carrying 32 parity octets generated by FEC encoder (binary)

Sync [0:1]	64bit payload (transmitted from left to right)
00	0111 1110 0100 0110 1010 1100 1101 1111 1101 1011 1111 1001 0111 1010 0111 0001
11	1011 1111 0100 1101 1000 0001 0111 1100 1001 1111 1011 1000 1101 1001 0101 1000
11	0100 1100 0111 1000 0000 1110 1111 0011 1011 1011 0100 0011 0011 0100 0010 1010
00	1100 0010 1000 1111 0000 0000 0001 1110 0011 1100 1111 0010 1011 1101 0010 1111

93. Multipoint MAC Control for 10G–EPON

Editors' Note #1 (to be removed prior to release): This amendment is based on the current edition of IEEE P802.3ay (D2.2). The editing instructions define how to merge the material contained in this amendment into the base document set to form the new comprehensive standard as created by the addition of IEEE P802.3av.

This amendment is new material to be added to IEEE P802.3ay (D2.2). The material contained in this amendment forms the new comprehensive standard as created by the addition of IEEE P802.3av.
External cross references are marked with double "@" signs (for example Clause @@1.1.1@@) and will be converted to hyperlinks in the later release of the draft.

Editors' Note #2 (to be removed prior to release): Draft revision history for Clause 93

Draft	*Date*	*Comment*
Draft 1.1	*Feb 2008*	*Draft for Task Force review with comment resolution from January 2008 meeting* *First version of Clause 93 draft available*
Draft 1.2	*Apr 2008*	*Draft for Task Force review with comment resolution from March 2008 meeting*
Draft 1.3	*May 2008*	*Draft for Task Force review with comment resolution from April 2008 meeting*
Draft 1.8023	*Jun 2008*	*Draft for Task Force review with comment resolution from May 2008 meeting*

93.1 Overview

This clause deals with the mechanism and control protocols required in order to reconcile the 10 Gb/s P2MP topology into the Ethernet framework. The P2MP medium is a passive optical network (PON), an optical network with no active elements in the signal's paths from source to destination. The only interior elements used in a PON are passive optical components, such as optical fiber, splices, and splitters. When combined with the Ethernet protocol, such a network is referred to as Ethernet passive optical network (EPON).

P2MP is an asymmetrical medium based on a tree (or tree–and–branch) topology. The DTE connected to the trunk of the tree is called optical line terminal (OLT) and the DTEs connected at the branches of the tree are called optical network units (ONU). The OLT typically resides at the service provider's facility, while the ONUs are located at the subscriber premises.

In the downstream direction (from the OLT to an ONU), signals transmitted by the OLT pass through a 1:N passive splitter (or cascade of splitters) and reach each ONU. In the upstream direction (from the ONUs to the OLT), the signal transmitted by an ONU would only reach the OLT, but not other ONUs. To avoid data collisions and increase the efficiency of the subscriber access network, ONU's transmissions are arbitrated. This arbitration is achieved by allocating a transmission window (grant) to each ONU. An ONU defers transmission until its grant arrives. When the grant arrives, the ONU transmits frames at wire speed during its assigned time slot.

A simplified P2MP topology example is depicted in Figure 93–1. Clause 67 provides additional examples of P2MP topologies.

Topics dealt with in this clause include allocation of upstream transmission resources to different ONUs, discovery and registration of ONUs into the network, and reporting of congestion to higher layers to allow for dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

This clause does not deal with topics including bandwidth allocation strategies, authentication of end–devices, quality–of–service definition, provisioning, or management.

This clause specifies the multipoint control protocol (MPCP) to operate an optical multipoint network by defining a Multipoint MAC Control sublayer as an extension of the MAC Control sublayer defined in @@Clause 31@@, and supporting current and future operations as defined in @@Clause 31@@ and annexes.

Each PON consists of a node located at the root of the tree assuming the role of OLT, and multiple nodes located at the tree leaves assuming roles of ONUs. The network operates by allowing only a single ONU to transmit in the upstream direction at a time. The MPCP located at the OLT is responsible for timing the different transmissions. Reporting of congestion by the different ONUs may assist in optimally allocating the bandwidth across the PON.

Automatic discovery of end stations is performed, culminating in registration through binding of an ONU to an OLT port by allocation of a Logical Link ID (see LLID in @@Subclause 92.1.6.2.3.2@@), and dynamic binding to a MAC connected to the OLT.

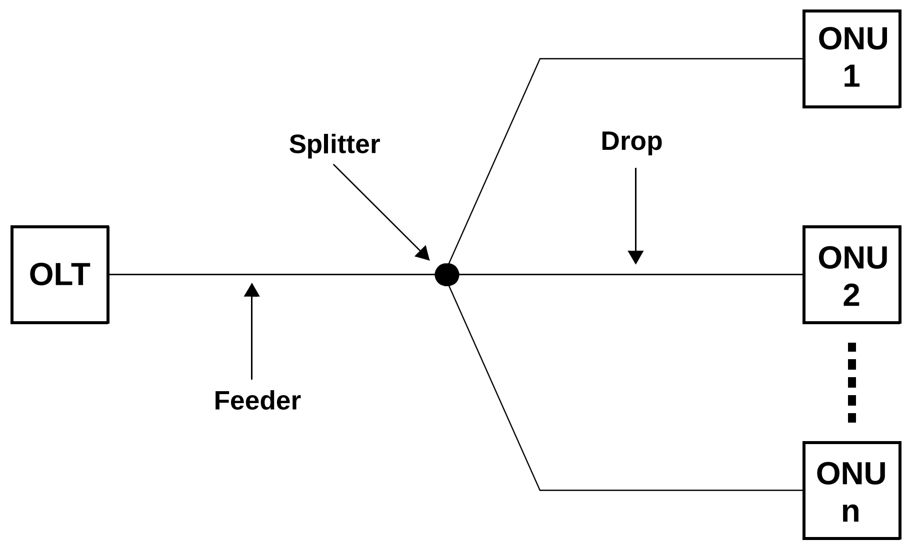


Figure 93–1—PON topology example

The Multipoint MAC Control functionality shall be implemented for subscriber access devices containing point–to–multipoint Physical Layer devices defined in @@Clause 91@@.

93.1.1 Goals and objectives

The goals and objectives of this clause are the definition of a point–to–multipoint Ethernet network utilizing an optical medium.

Specific objectives met include:

a) Support of Point–to–Point Emulation (P2PE) as specified
b) Support multiple LLIDs and MAC Clients at the OLT
c) Support a single LLID per ONU
d) Support a mechanism for single copy broadcast
e) Flexible architecture allowing dynamic allocation of bandwidth
f) Use of 32 bit timestamp for timing distribution
g) MAC Control based architecture
h) Ranging of discovered devices for improved network performance
i) Continuous ranging for compensating round trip time variation

93.1.2 Position of Multipoint MAC Control within the IEEE 802.3 hierarchy

Multipoint MAC Control defines the MAC control operation for optical point–to–multipoint networks. Figure 93–2.a and Figure 93–2.b depict the architectural positioning of the Multipoint MAC Control sublayer with respect to the MAC and the MAC Control client. The Multipoint MAC Control sublayer takes the place of the MAC Control sublayer to extend it to support multiple clients and additional MAC control functionality.

Multipoint MAC Control is defined using the mechanisms and precedents of the MAC Control sublayer. The MAC Control sublayer has extensive functionality designed to manage the real–time control and manipulation of MAC sublayer operation. This clause specifies the extension of the MAC Control mechanism to manipulate multiple underlying MACs simultaneously. This clause also specifies a specific protocol implementation for MAC Control.

The Multipoint MAC Control sublayer is specified such that it can support new functions to be implemented and added to this standard in the future. MultiPoint Control Protocol (MPCP), the management protocol for P2MP is one of these protocols. Non–real–time, or quasi–static control (e.g., configuration of MAC operational parameters) is provided by Layer Management. Operation of the Multipoint MAC Control sublayer is transparent to the MAC.

As depicted in Figure 93–2.a and Figure 93–2.b, the layered system instantiates multiple MAC entities, using a single Physical Layer. The individual MAC instances offer a point–to–point emulation service between the OLT and the ONU. An additional MAC is instantiated to communicate to all 10G–EPON ONUs at once. This instance takes maximum advantage of the broadcast nature of the downstream channel by sending a single copy of a frame that is received by all 10G–EPON ONUs. This MAC instance is referred to as Single Copy Broadcast (SCB).

The ONU only requires one MAC instance since frame filtering operations are done at the RS layer before reaching the MAC. Therefore, MAC and layers above are emulation–agnostic at the ONU (see @@Subclause 92.1.6.2.3@@).

Although Figure 93–2.a and Figure 93–2.b and supporting text describe multiple MACs within the OLT, a single unicast MAC address may be used by the OLT. Within the EPON Network, MACs are uniquely identified by their LLID which is dynamically assigned by the registration process.

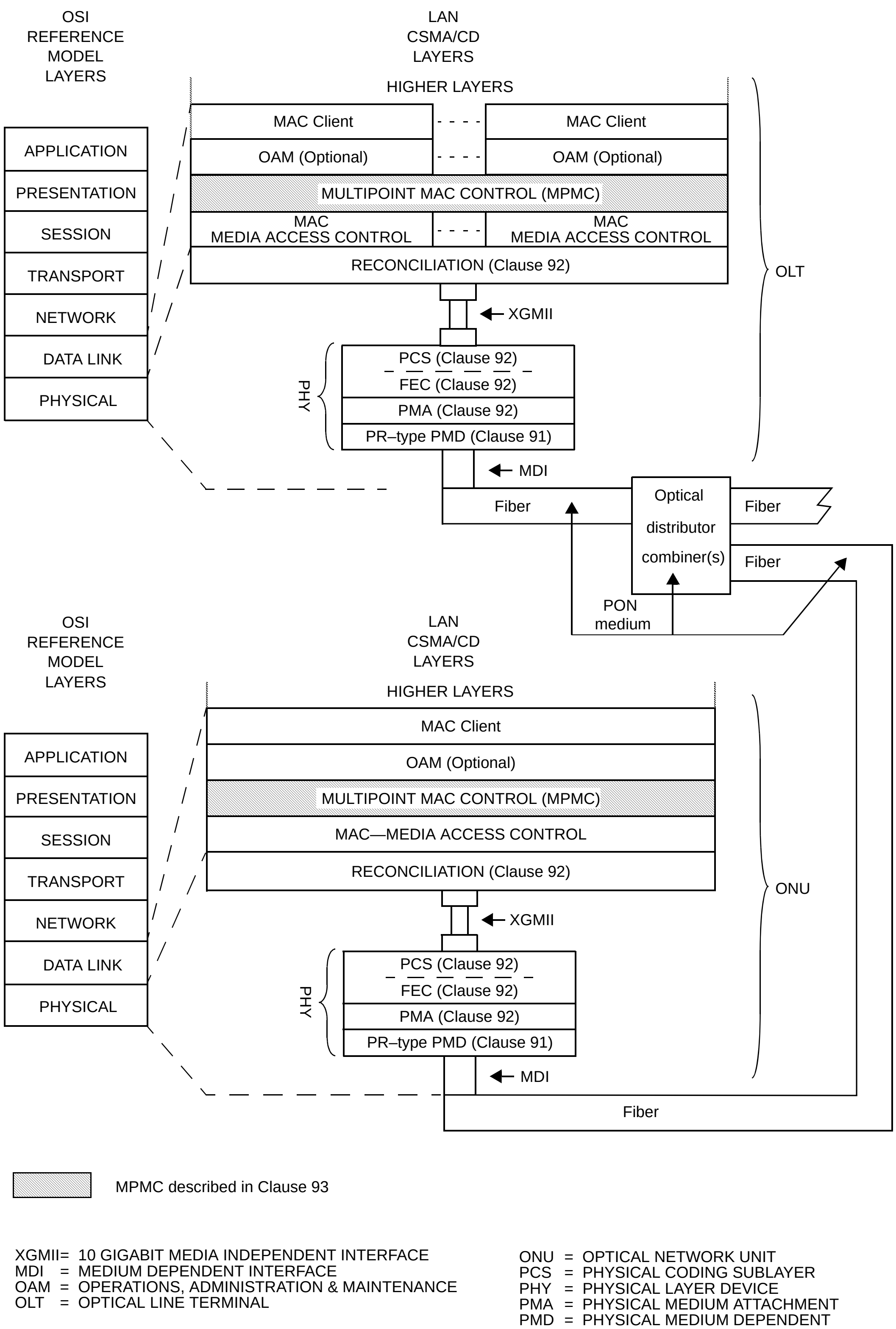
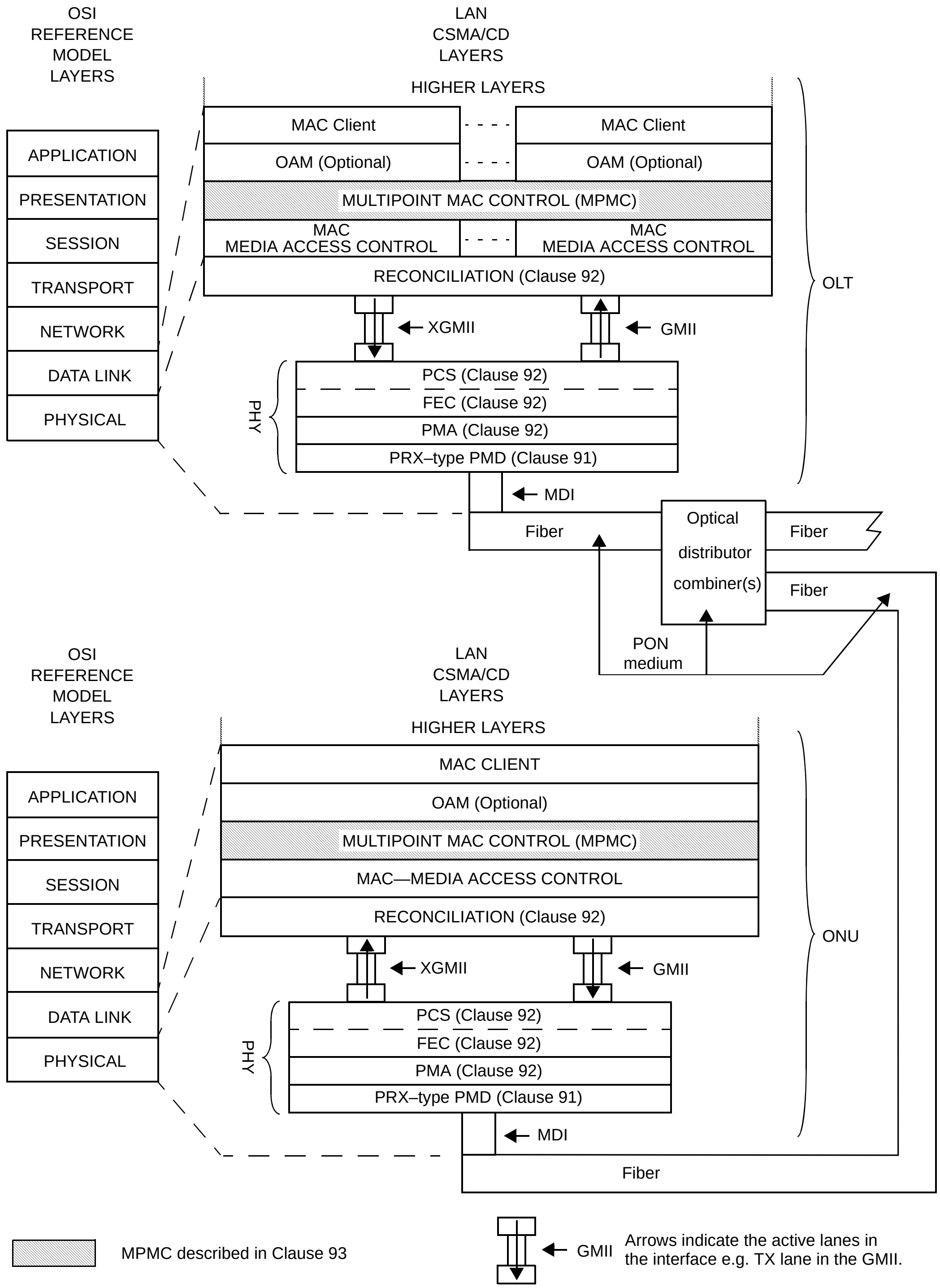


Figure 93–2a—Relationship of Multipoint MAC Control and the OSI protocol stack for 10 Gb/s symmetric PON (10 Gb/s downstream and 10 Gb/s upstream)



XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 93–2b—Relationship of Multipoint MAC Control and the OSI protocol stack for 10/1 Gb/s asymmetric PON (10 Gb/s downstream and 1 Gb/s upstream).

93.1.3 Functional block diagram

Figure 93–3 provides a functional block diagram of the Multipoint MAC Control architecture.

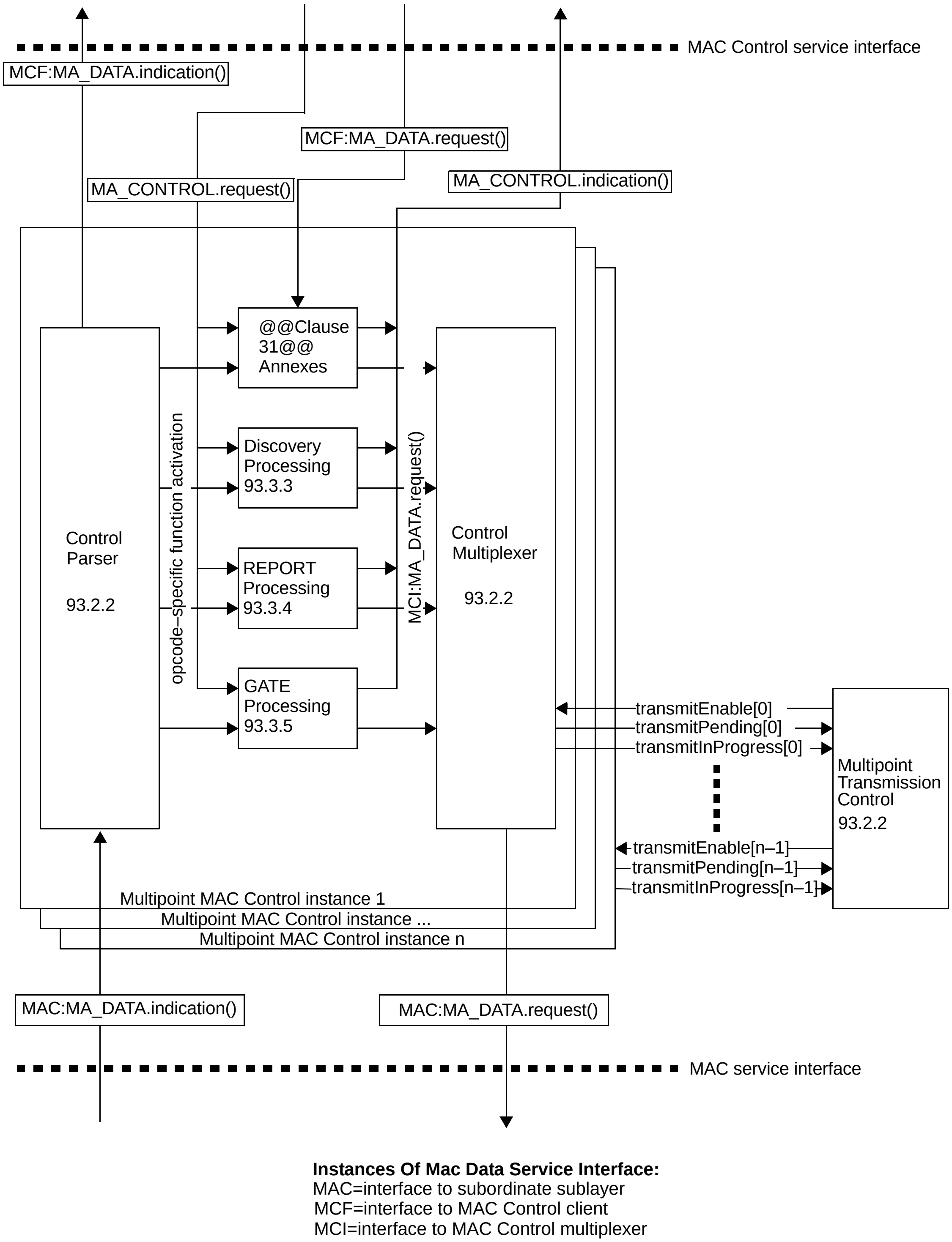


Figure 93–3—Multipoint MAC Control functional block diagram

93.1.4 Service interfaces

The MAC Client communicates with the Control Multiplexer using the standard service interface specified in @@Subclause 2.3@@. Multipoint MAC Control communicates with the underlying MAC sublayer using the standard service interface specified in @@Annex 4A.3.2@@. Similarly, Multipoint MAC Control communicates internally using primitives and interfaces consistent with definitions in @@Clause 31@@.

93.1.5 State diagram conventions

The body of this standard comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of @@Subclause 21.5@@. State diagram timers follow the conventions of @@Subclause 14.2.3.2@@ augmented as follows:

a) [start x_timer, y] sets expiration of *y* to timer *x_timer*.
b) [stop x_timer] aborts the timer operation for *x_timer* asserting *x_timer_not_done* indefinitely.

The state diagrams use an abbreviation MACR as a shorthand form for MA_CONTROL.request and MACI as a shorthand form for MA_CONTROL.indication.

The vector notations used in the state diagrams for bit vector use 0 to mark the first received bit and so on (for example data[0:15]), following the conventions of @@Subclause 3.1@@ for bit ordering. When referring to an octet vector, 0 is used to mark the first received octet and so on (for example m_sdu[0..1]).

$a < b$: A function that is used to compare two (cyclic) time values. Returned value is true when b is larger than a allowing for wrap around of a and b. The comparison is made by subtracting b from a and testing the MSB. When MSB(a–b) = 1 the value true is returned, else false is returned. In addition, the following functions are defined in terms of $a < b$:
$a > b$ is equivalent to !($a < b$ or $a = b$)
$a \geq b$ is equivalent to !($a < b$)
$a \leq b$ is equivalent to !($a > b$)

93.2 Multipoint MAC Control operation

As depicted in Figure 93–3, the Multipoint MAC Control functional block comprises the following functions:

a) *Multipoint Transmission Control*. This block is responsible for synchronizing Multipoint MAC Control instances associated with the Multipoint MAC Control. This block maintains the Multipoint MAC Control state and controls the multiplexing functions of the instantiated MACs.
b) *Multipoint MAC Control Instance n*. This block is instantiated for each MAC and respective MAC and MAC Control clients associated with the Multipoint MAC Control. It holds all the variables and state associated with operating all MAC Control protocols for the instance.
c) *Control Parser*. This block is responsible for parsing MAC Control frames, and interfacing with @@Clause 31@@ entities, the opcode specific blocks, and the MAC Client.
d) *Control Multiplexer*. This block is responsible for selecting the source of the forwarded frames.
e) *@@Clause 31@@ Annexes*. This block holds MAC Control actions as defined in @@Clause 31@@ annexes for support of legacy and future services.
f) *Discovery, Report and Gate Processing*. These blocks are responsible for handling the MPCP in the context of the MAC.

93.2.1 Principles of Multipoint MAC Control

As depicted in Figure 93–3, Multipoint MAC Control sublayer may instantiate multiple Multipoint MAC Control instances in order to interface multiple MAC and MAC Control clients above with multiple MACs below. A unique unicast MAC instance is used at the OLT to communicate with each ONU. The individual MAC instances utilize the point–to–point emulation service between the OLT and the ONU as defined in @@Subclause 92.1@@.

At the ONU, a single MAC instance is used to communicate with a MAC instance at the OLT. In that case, the Multipoint MAC Control contains only a single instance of the Control Parser/Multiplexer function.

Multipoint MAC Control protocol supports several MAC and client interfaces. Only a single MAC interface and Client interface is enabled for transmission at a time. There is a tight mapping between a MAC service interface and a Client service interface. In particular, the assertion of the MAC:MA_DATA.indication primitive in MAC *j* leads to the assertion of the MCF:MA_DATA.indication primitive to Client *j*. Conversely, the assertion of the request service interface in Client *i* leads to the assertion of the MAC:MA_DATA.request primitive of MAC *i*. Note that the Multipoint MAC sublayer need not receive and transmit packets associated with the same interface at the same time. Thus the Multipoint MAC Control acts like multiple MAC Controls bound together with common elements.

The scheduling algorithm is implementation dependent, and is not specified for the case where multiple transmit requests happen at the same time.

The reception operation is as follows. The Multipoint MAC Control instances generate MAC:MA_DATA.indication service primitives continuously to the underlying MAC instances. Since these MACs are receiving frames from a single PHY only one frame is passed from the MAC instances to Multipoint MAC Control. The MAC instance responding to the MAC:MA_DATA.indication is referred to as the enabled MAC, and its service interface is referred to as the enabled MAC interface. The MAC passes to the Multipoint MAC Control sublayer all valid frames. Invalid frames, as specified in @@Subclause 3.4@@, are not passed to the Multipoint MAC Control sublayer in response to a MAC:MA_DATA.indication service primitive.

The enabling of a transmit service interface is performed by the Multipoint MAC Control instance in collaboration with the Multipoint Transmission Control. Frames generated in the MAC Control are given priority over MAC Client frames, in effect, prioritizing the MA_CONTROL primitive over the MCF:MA_DATA primitive, and for this purpose MCF:MA_DATA.request primitives may be delayed, discarded or modified in order to perform the requested MAC Control function. For the transmission of this frame, the Multipoint MAC Control instance enables forwarding by the MAC Control functions, but the MAC Client interface is not enabled. The reception of a frame in a MAC results in generation of the MAC:MA_DATA.indication primitive on that MAC's interface. Only one receive MAC interface will be enabled at any given time since there is only one PHY interface.

The information of the enabled interfaces is stored in the controller state variables, and accessed by the Multiplexing Control block.

The Multipoint MAC Control sublayer uses the services of the underlying MAC sublayer to exchange both data and control frames.

Receive operation (MAC:MA_DATA.indication) at each instance:

a) A frame is received from the underlying MAC.
b) The frame is parsed according to Length/Type field
c) MAC Control frames are demultiplexed according to opcode and forwarded to the relevant processing functions
d) Data frames (see @@Subclause 31.5.1@@) are forwarded to the MAC Client by asserting MCF:MA_DATA.indication primitives

Transmit operation (MAC:MA_DATA.request) at each instance:

e) The MAC Client signals a frame transmission by asserting MCF:MA_DATA.request, or
f) A protocol processing block attempts to issue a frame, as a result of a previous MA_CONTROL.request or as a result of an MPCP event that generates a frame.
g) When allowed to transmit by the Multipoint Transmission Control block, the frame is forwarded.

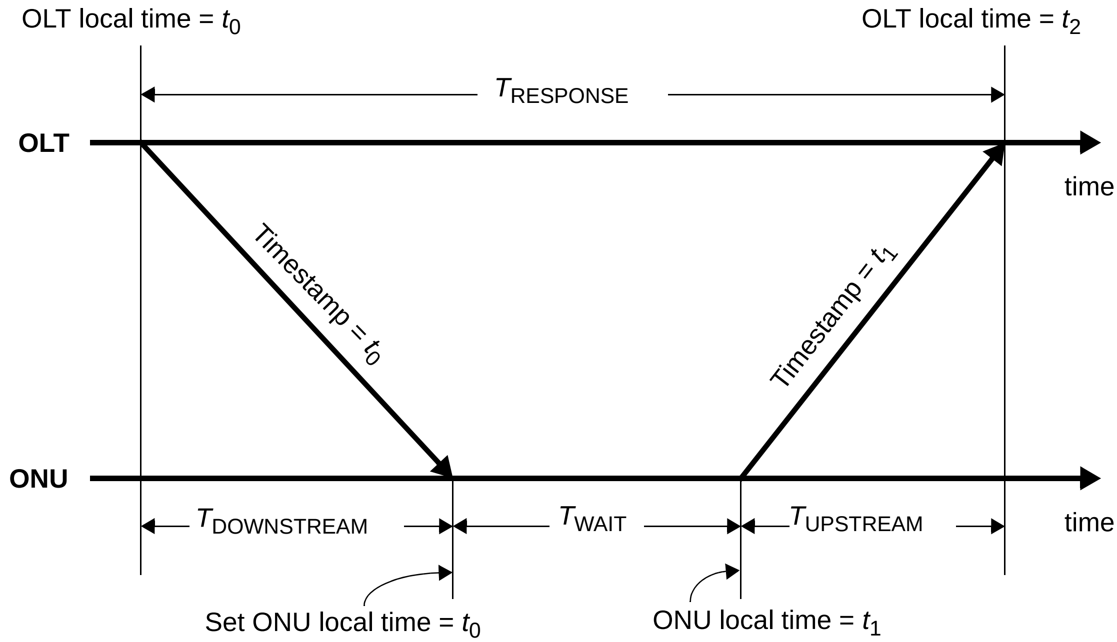
93.2.1.1 Ranging and Timing Process

Both the OLT and the ONU have 32–bit counters that increment every 16 ns. These counters provide a local time stamp. When either device transmits an MPCPDU, it maps its counter value into the timestamp field. The time of transmission of the first octet of the MPCPDU frame from the MAC Control to the MAC is taken as the reference time used for setting the timestamp value.

When the ONU receives MPCPDUs, it sets its counter according to the value in the timestamp field in the received MPCPDU.

When the OLT receives MPCPDUs, it uses the received timestamp value to calculate or verify a round trip time between the OLT and the ONU. The Round Trip Time (RTT) is equal to the difference between the timer value and the value in the timestamp field. The calculated RTT is notified to the client via the MA_CONTROL.indication primitive. The client can use this RTT for the ranging process.

A condition of *timestamp drift error* occurs when the difference between OLT's and ONU's clocks exceeds some predefined threshold. This condition can be independently detected by the OLT or an ONU. The OLT detects this condition when an absolute difference between new and old RTT values measured for a given ONU exceeds the value of guardThresholdOLT (see Subclause 93.2.2.1), as shown in Figure 93–10. An ONU detects the timestamp drift error condition when absolute difference between a timestamp received in an MPCPDU and the localTime counter exceeds guardThresholdONU (see Subclause 93.2.2.1), as is shown in Figure 93–11.



$T_{DOWNSTREAM}$ = downstream propagation delay

$T_{UPSTREAM}$ = upstream propagation delay

T_{WAIT} = wait time at ONU = $t_1 - t_0$

$T_{RESPONSE}$ = response time at OLT = $t_2 - t_0$

$$RTT = T_{DOWNSTREAM} + T_{UPSTREAM} = T_{RESPONSE} - T_{WAIT} = (t_2 - t_0) - (t_1 - t_0) = t_2 - t_1$$

Figure 93–4—Round trip time calculation

93.2.2 Multipoint transmission control, Control Parser, and Control Multiplexer

The purpose of the multipoint transmission control is to allow only one of the multiple MAC clients to transmit to its associated MAC and subsequently to the RS layer at one time by only asserting one transmitEnable signal at a time.

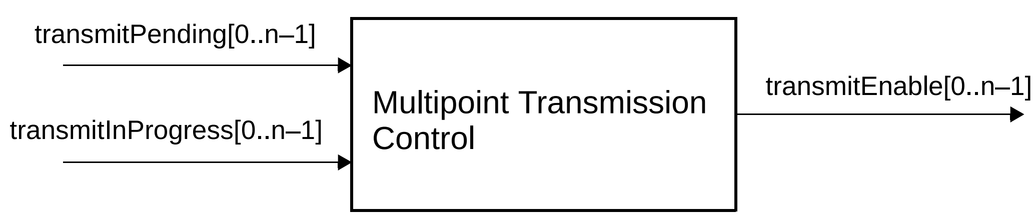


Figure 93–5—Multipoint Transmission Control Service Interfaces

Multipoint MAC Control Instance n function block communicates with the Multipoint Transmission Control using transmitEnable[n], transmitPending[n], and transmitInProgress[n] state variables (see Figure 93–3).

The Control Parser is responsible for opcode independent parsing of MAC frames in the reception path. By identifying MAC Control frames, demultiplexing into multiple entities for event handling is possible. Interfaces are provided to existing @@Clause 31@@ entities, functional blocks associated with MPCP, and the MAC Client.

The Control Multiplexer is responsible for forwarding frames from the MAC Control opcode–specific functions and the MAC Client to the MAC. Multiplexing is performed in the transmission direction. Given multiple MCF:MA_DATA.request primitives from the MAC Client, and MA_CONTROL.request primitives from the MAC Control Clients, a single MAC:MA_DATA.request service primitive is generated for transmission. At the OLT, multiple MAC instances share the same Multipoint MAC Control, as a result, the transmit block is enabled based on an external control signal housed in Multipoint Transmission Control for transmission overlap avoidance. At the ONU the Gate Processing functional block interfaces for upstream transmission administration.

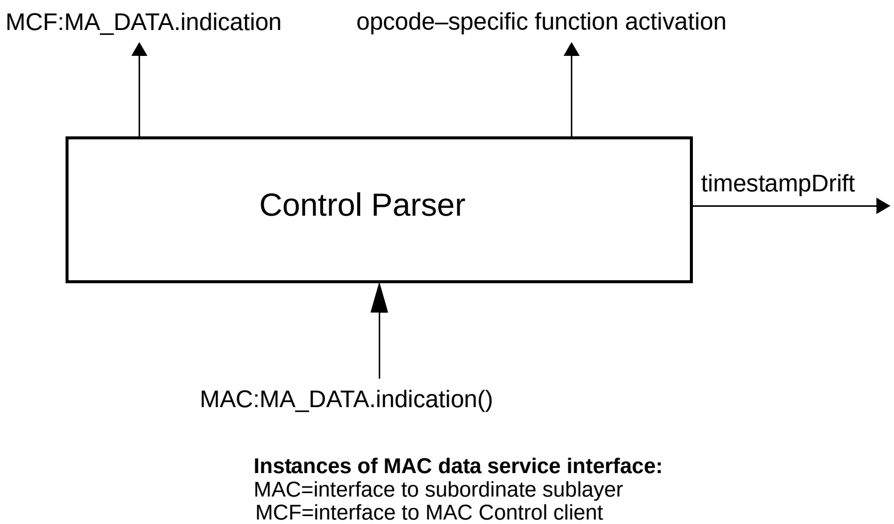
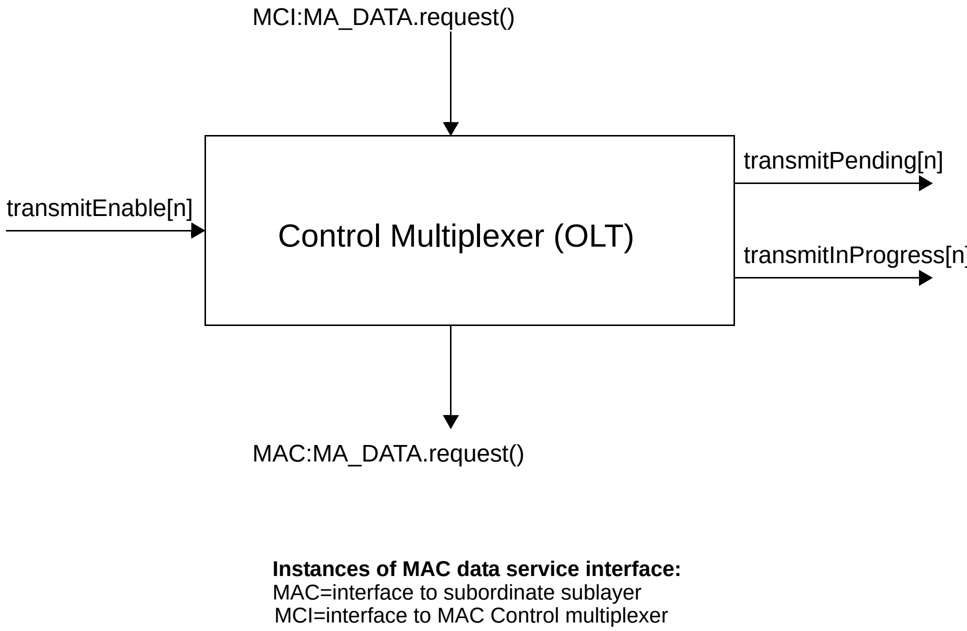
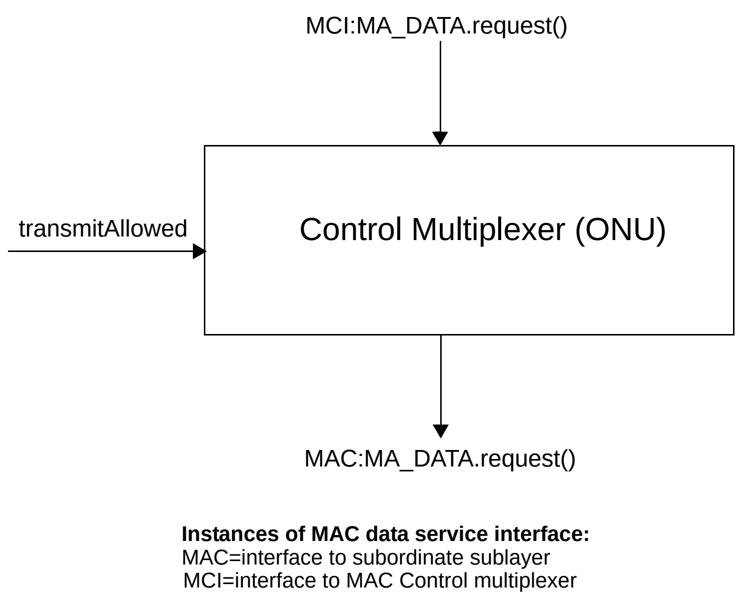


Figure 93–6—Control Parser service interfaces



NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 93–7—OLT Control Multiplexer service interfaces



NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 93–8—ONU Control Multiplexer service interfaces

93.2.2.1 Constants

blockSize

TYPE: 8 bit unsigned

This constant represents the size of a FEC block in columns.

VALUE: 54

colSize

TYPE: 8 bit unsigned

This constant represents the size of a column in bytes.

VALUE: 4

guardThresholdOLT

TYPE: integer

This constant holds the maximum amount of drift allowed for a timestamp received at the OLT. This value is measured in units of time_quantum.

VALUE: 12

guardThresholdONU

TYPE: integer

This constant holds the maximum amount of drift allowed for a timestamp received at the ONU. This value is measured in units of time_quantum.

VALUE: 8

ipgLen

TYPE: 8 bit unsigned

This constant represents the size of the IPG in bytes.

VALUE: 12

MAC_Control_type

TYPE: integer

The value of the Length/Type field as defined in @@Subclause 31.4.1.3@@.

VALUE: 0x8808

parityRatio

TYPE: 8 bit unsigned

This constant represents the size of the parity block in columns.

VALUE: 8

preLen

TYPE: 8 bit unsigned

This constant represents the size of preamble in bytes.

VALUE: 8

tailGuard

TYPE: integer

This constant holds the value used to reserve space at the end of the upstream transmission at the ONU in addition to the size of last MAC service data unit (m_sdu) in units of octets. Space is reserved for the MAC overheads including: preamble, SFD, DA, SA, Length/Type, FCS, and minimum inter–packet gap. The sizes of the above listed MAC overhead items are described in @@Subcause 3.1.1@@. The size of the minimum IPG is described in @@Subclause 36.2.4.14@@.

VALUE: 42

time_quantum

TYPE: integer

The unit of time_quantum is used by all mechanisms synchronized to the advancement of the localTime variable. All variables that represent counters and time intervals are defined using time_quantum. Each time_quantum is 16 ns.

VALUE: 16

tqSize

TYPE: integer

This constant represents time_quantum in octet transmission times.

VALUE: 20

93.2.2.2 Counters

localTime

TYPE: 32 bit unsigned

This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 62.5MHz, and counts in time_quanta. At the OLT the counter shall track the transmit clock, while at the ONU the counter shall track the receive clock. For accuracy of receive clock see @@Subclause 92.3.1.2@@. It is reloaded with the received timestamp value (from the OLT) by the Control Parser (see Figure 93–13). Changing the value of this variable while running using Layer Management is highly undesirable and is unspecified.

93.2.2.3 Variables

BEGIN

TYPE: Boolean

This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

data_rx

TYPE: bit array

This variable represents a 0–based bit array corresponding to the payload of a received MPCPDU. This variable is used to parse incoming MPCPDU frames.

data_tx

TYPE: bit array

This variable represents a 0–based bit array corresponding to the payload of an MPCPDU being transmitted. This variable is used to access payload of outgoing MPCPDU frames, for example to set the timestamp value.

frameLen

TYPE: 16 bit unsigned

This variable represents the size of the frame in bytes.

newRTT

TYPE: 16 bit unsigned

This variable temporary holds a newly–measured Round Trip Time to the ONU. The new RTT value is represented in units of time_quanta.

nextTxTime

TYPE: 16 bit unsigned

This variable represents a total transmission time of next packet and is used to check whether the next packet fits in the remainder of ONU’s transmission window. The value of nextTxTime includes packet transmission time, tailGuard defined in Subclause 93.2.2.1, and FEC parity data overhead. This variable is measured in units of time_quanta.

opcode_rx
TYPE: 16 bit unsigned
This variable holds an opcode of the last received MPCPDU.

opcode_tx
TYPE: 16 bit unsigned
This variable holds an opcode of an outgoing MPCPDU.

packet_initiate_delay
TYPE: 16 bit unsigned
This variable is used to set the time–out interval for packet_initiate_timer defined in 93.2.2.5. The packet_initiate_delay value is represented in units of bytes.

RTT
TYPE: 16 bit unsigned
This variable holds the measured Round Trip Time to the ONU. The RTT value is represented in units of time_quanta.

stopTime
TYPE: 32 bit unsigned
This variable holds the value of the localTime counter corresponding to the end of the nearest grant. This value is set by the Gate Processing function as described in Subclause 93.3.5.

timestamp
TYPE: 32 bit unsigned
This variable holds the value of timestamp of the last received MPCPDU frame.

timestampDrift
TYPE: Boolean
This variable is used to indicate whether an error is signaled as a result of uncorrectable timestamp drift.

transmitAllowed
TYPE: Boolean
This variable is used to control PDU transmission at the ONU. It is set to true when the transmit path is enabled, and is set to false when the transmit path is being shut down. transmitAllowed changes its value according to the state of the Gate Processing functional block.

transmitEnable[j]
TYPE: Boolean
These variables are used to control the transmit path in a Multipoint MAC Control instance at the OLT. Setting them to on indicates that the selected instance is permitted to transmit a frame. Setting it to off inhibits the transmission of frames in the selected instance. Only one of transmitEnable[j] should be set to on at a time.

transmitInProgress[j]
TYPE: Boolean
This variable indicates that the Multipoint MAC Control instance *j* is in a process of transmitting a frame.

transmitPending[j]
TYPE: Boolean
This variable indicates that the Multipoint MAC Control instance *j* is ready to transmit a frame.

93.2.2.4 Functions

abs(n)
This function returns the absolute value of the parameter n.

Opcode–specific function(opcode)
Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

FEC_Overhead_Max(length)
This function calculates the maximum size of additional overhead to be added by the FEC encoder while encoding a frame of size length. As described in @@Subclause 92.2.3@@, FEC encoder adds 32 parity octets for each block of 216 data or control octets. This is equivalent to an overhead of 4 time_quanta for every 27 time_quanta transmitted. Table 93–1 presents the value of the FEC_Overhead_Max function for various frame lengths. The following formula is used to calculate the overhead:

$$\text{FEC\_Overhead\_Max}(\text{length}) = \text{FEC\_Overhead\_Min}(\text{length}) + (\text{parityRatio} \times \text{colSize})$$

FEC_Overhead_Min(length)
This function calculates the minimum size of additional overhead to be added by the FEC encoder while encoding a frame of size length. As described in @@Subclause 92.2.3@@, FEC encoder adds 32 parity octets for each block of 216 data or control octets. This is equivalent to an overhead of 4 time_quanta for every 27 time_quanta transmitted. Table 93–1 presents the value of the FEC_Overhead_Min function for various frame lengths. The following formula is used to calculate the overhead:

$$\text{FEC\_Overhead\_Min}(\text{length}) = \left\lfloor \frac{\text{frameLen} + \text{preLen} + \text{ipgLen}}{\text{colSize} \times \text{blockSize}} \right\rfloor \times \text{parityRatio}$$

NOTE–The notation $\lfloor x \rfloor$ represents a *floor* function, which returns the value of its argument x rounded down to the nearest integer.

Table 93–1—Minimum and maximum FEC_Overhead for various frame lengths

Frame length [bytes]		FEC Overhead [bytes]	
Min	**Max**	**Min**	**Max**
64	195	0	32
196	411	32	64
412	627	64	96
628	843	96	128
844	1059	128	160
1060	1275	160	192
1276	1491	192	224
1492	1707	224	256
1708	1923	256	288
1924	2000	288	320

select

This function selects the next Multipoint MAC Control instance allowed to initiate transmission of a frame. The function returns an index to the transmitPending array for which the value is not false. The selection criteria in the presence of multiple active elements in the list is implementation dependent.

SelectFrame()

This function enables the interface, which has a pending frame. If multiple interfaces have frames waiting at the same time, only one interface will be enabled. The selection criteria is not specified, except for the case when some of the pending frames have Length/Type = MAC_Control. In this case, one of the interfaces with a pending MAC Control frame shall be enabled.

sizeof(sdu)

This function returns the size of the sdu in octets.

transmissionPending()

This function returns true if any of the Multipoint MAC Control instances has a frame waiting to be transmitted. The function can be represented as:

```
transmissionPending() =
   transmitPending[0] +
   transmitPending[1] +
   ... +
   transmitPending[n–1]
```

where n is the total number of Multipoint MAC Control instances.

93.2.2.5 Timers

packet_initiate_timer

This timer is used to delay frame transmission from MAC Control to avoid variable MAC delay while MAC enforces IPG after a previous frame. In addition, this timer increases interframe spacing just enough to accommodate the extra parity data to be added by the FEC encoder.

93.2.2.6 Messages

MA_DATA.indication(DA, SA, m_sdu, receiveStatus)

The service primitive is defined in @@Subclause 2.3.2@@.

MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in @@Subclause 2.3.2@@.

93.2.2.7 State Diagrams

The Multipoint transmission control function in the OLT shall implement state diagram shown in Figure 93–9. Control parser function in the OLT shall implement state diagram shown in Figure 93–10. Control parser function in the ONU shall implement state diagram shown in Figure 93–11. Control multiplexer function in the OLT shall implement state diagram shown in Figure 93–12. Control multiplexer function in the ONU shall implement state diagram shown in Figure 93–13.

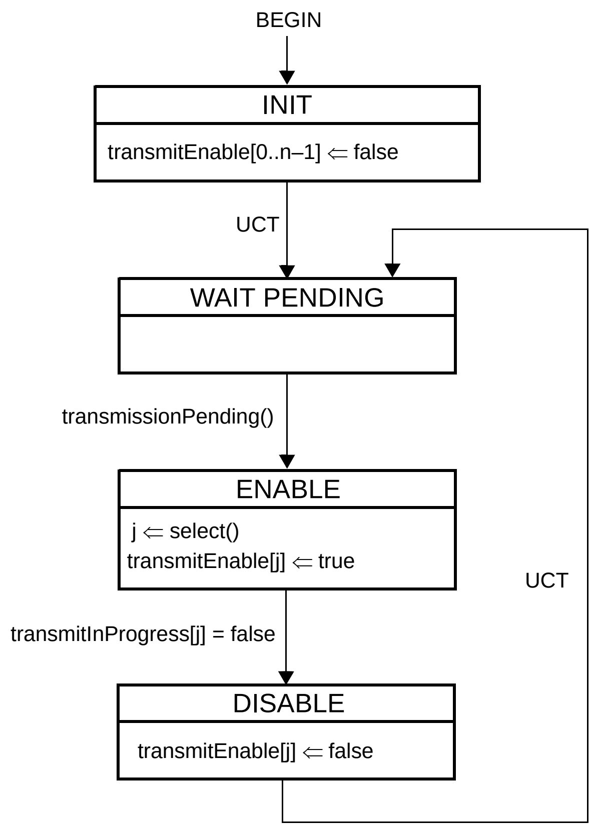


Figure 93–9—OLT Multipoint Transmission Control state diagram

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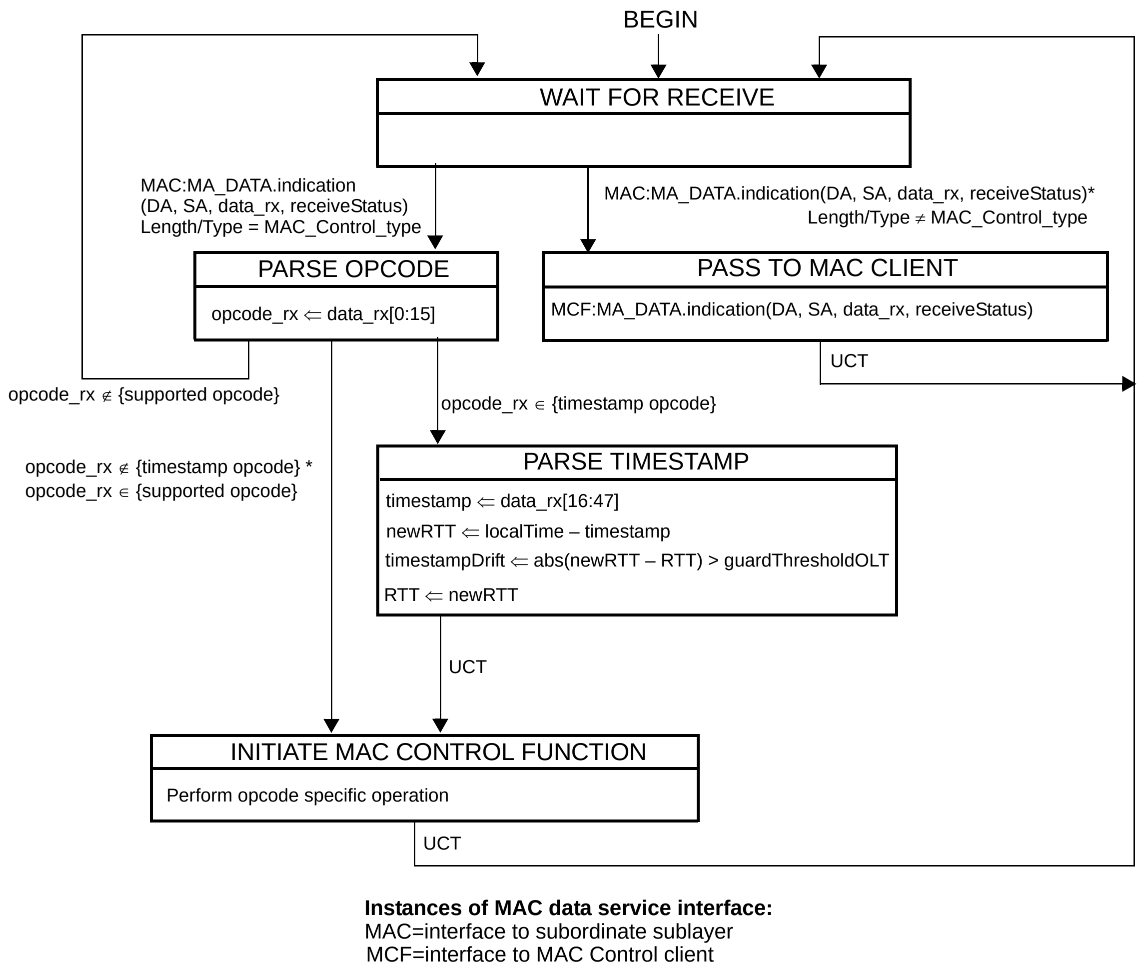
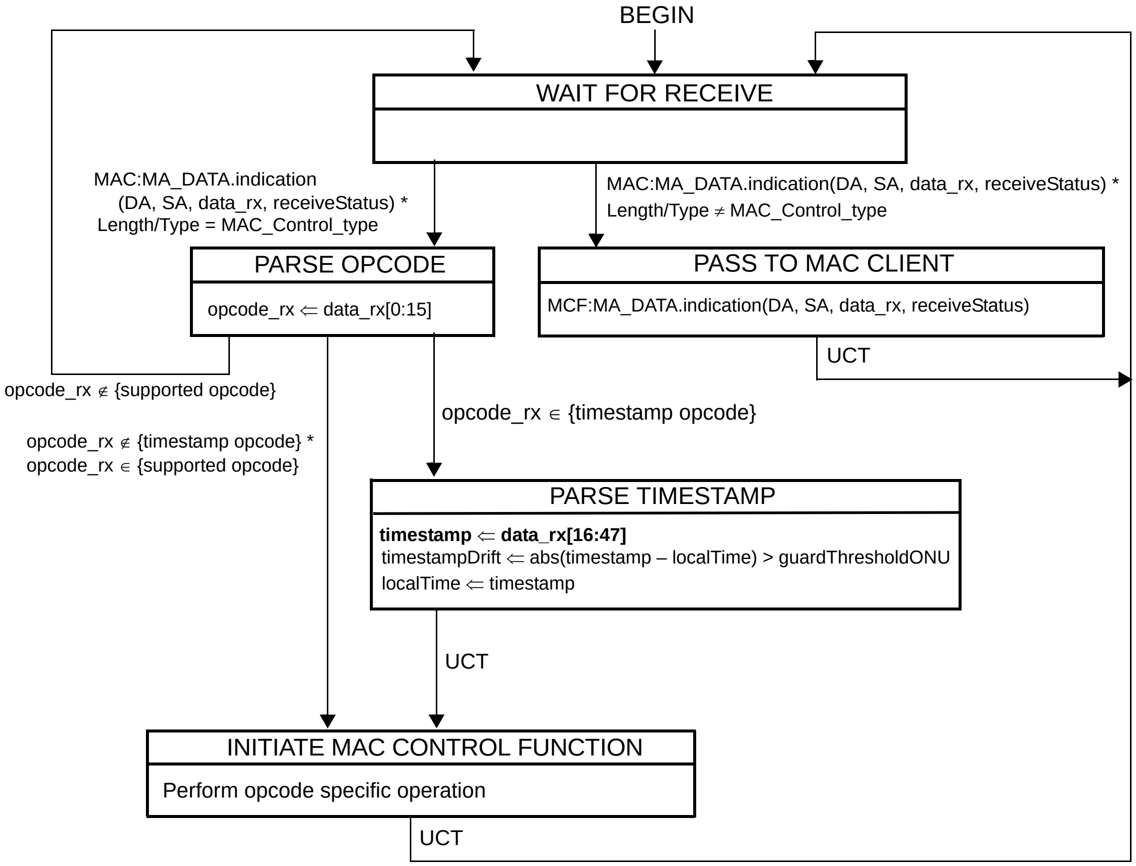


NOTE–The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 93–10—OLT Control Parser state diagram



Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCF=interface to MAC Control client

NOTE—The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to @@Annex 31A@@ for list of supported opcodes and timestamp opcodes.

Figure 93–11—ONU Control Parser state diagram

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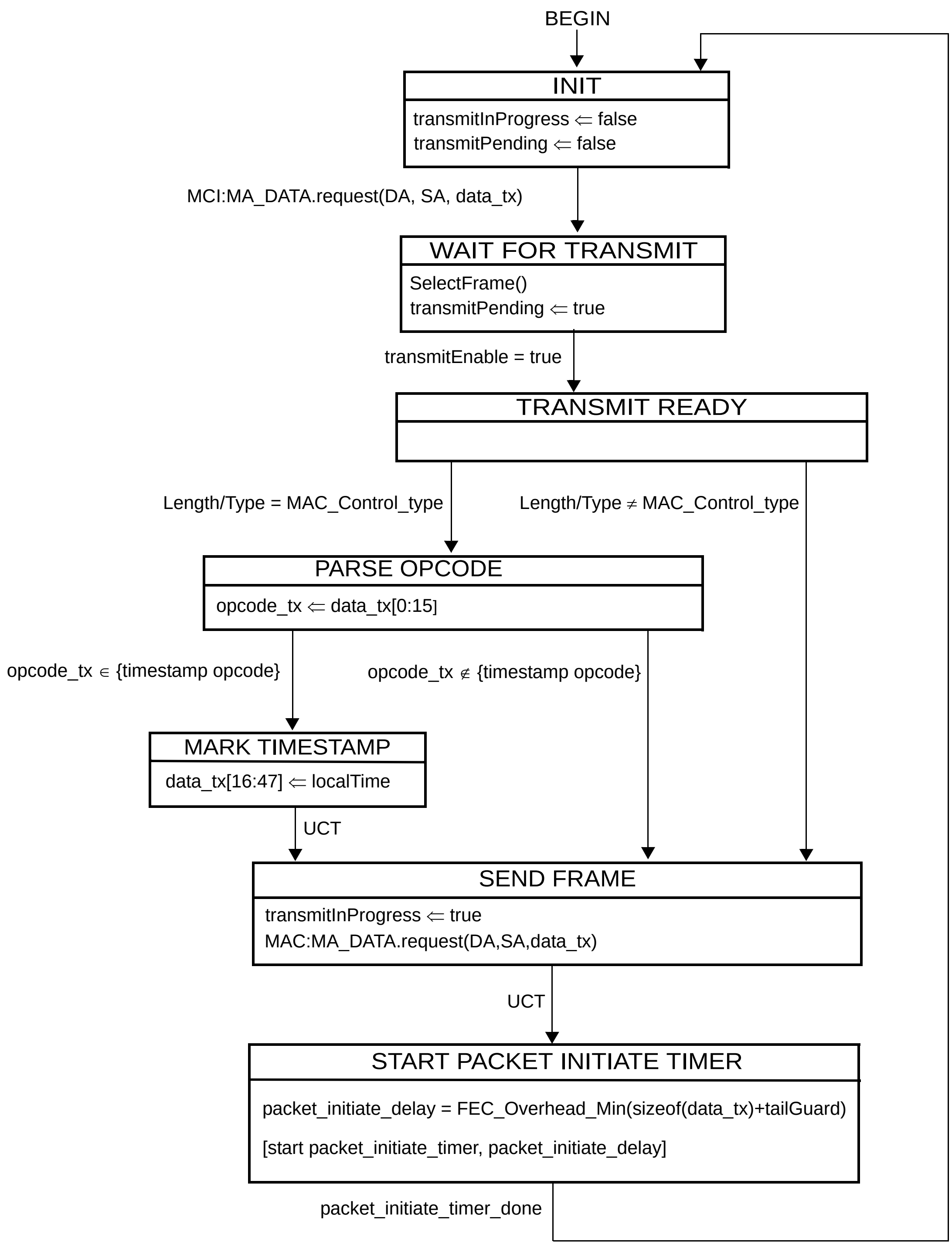


Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCI=interface to MAC Control multiplexer

Figure 93–12—OLT Control Multiplexer state diagram

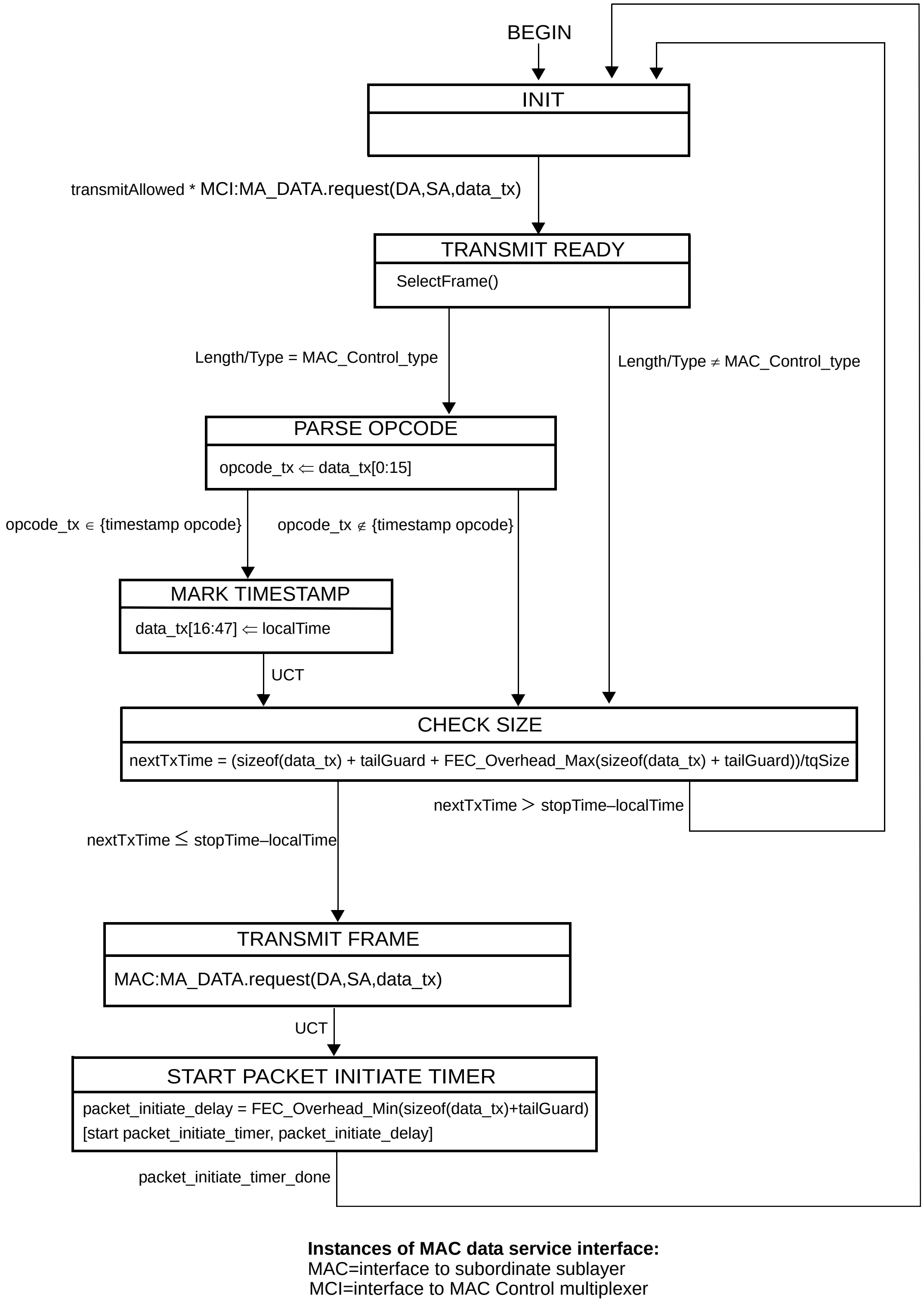


Figure 93–13—ONU Control Multiplexer state diagram

93.3 Multipoint Control Protocol (MPCP)

As depicted in Figure 93–3, the Multipoint MAC Control functional block comprises the following functions:

a) *Discovery Processing*. This block manages the discovery process, through which an ONU is discovered and registered with the network while compensating for RTT.
b) *Report Processing*. This block manages the generation and collection of report messages, through which bandwidth requirements are sent upstream from the ONU to the OLT.
c) *Gate Processing*. This block manages the generation and collection of gate messages, through which multiplexing of multiple transmitters is achieved.

As depicted in Figure 93–3, the layered system may instantiate multiple MAC entities, using a single Physical Layer. Each instantiated MAC communicates with an instance of the opcode specific functional blocks through the Multipoint MAC Control. In addition some global variables are shared across the multiple instances. Common state control is used to synchronize the multiple MACs using MPCP procedures. Operation of the common state control is generally considered outside the scope of this document.

93.3.1 Principles of Multipoint Control Protocol

Multipoint MAC Control enables a MAC Client to participate in a point–to–multipoint optical network by allowing it to transmit and receive frames as if it was connected to a dedicated link. In doing so, it employs the following principles and concepts:

a) A MAC client transmits and receives frames through the Multipoint MAC Control sublayer.
b) The Multipoint MAC Control decides when to allow a frame to be transmitted using the client interface Control Multiplexer.
c) Given a transmission opportunity, the MAC Control may generate control frames that would be transmitted in advance of the MAC Client’s frames, utilizing the inherent ability to provide higher priority transmission of MAC Control frames over MAC Client frames.
d) Multiple MACs operate on a shared medium by allowing only a single MAC to transmit upstream at any given time across the network using a time–division multiple access (TDMA) method.
e) Such gating of transmission is orchestrated through the Gate Processing function.
f) New devices are discovered in the network and allowed transmission through the Discovery Processing function.
g) Fine control of the network bandwidth distribution can be achieved using feedback mechanisms supported in the Report Processing function.
h) The operation of P2MP network is asymmetrical, with the OLT assuming the role of master, and the ONU assuming the role of slave.

93.3.2 Compatibility considerations

93.3.2.1 PAUSE operation

Even though MPCP is compatible with flow control, optional use of flow control may not be efficient in the case of large propagation delay. If flow control is implemented, then the timing constraints in @@Clause 31B@@ supplement the constraints found at Subclause 93.3.2.4.

NOTE—MAC at an ONU can receive frames from unicast channel and SCB channel. If the SCB channel is used to broadcast data frames to multiple ONUs, the ONU’s MAC may continue receiving data frames from SCB channel even after the ONU has issued a PAUSE request to its unicast remote–end.

93.3.2.2 Optional Shared LAN Emulation

By combining P2PE, suitable filtering rules at the ONU, and suitable filtering and forwarding rules at the OLT, it is possible to emulate an efficient shared LAN. Support for shared LAN emulation is optional, and requires an additional layer above the MAC, which is out of scope for this document. Thus, shared LAN emulation is introduced here for informational purposes only.

Specific behaviour of the filtering layer at the RS is specified in @@Subclause 92.1.6.2.3@@.

93.3.2.3 Multicast and single copy broadcast support

In the downstream direction, the PON is a broadcast medium. In order to make use of this capability for forwarding broadcast frames from the OLT to multiple recipients without frame duplication for each ONU, the SCB support is introduced.

The OLT has at least one MAC associated with every ONU. In addition one more MAC at the OLT is marked as the SCB MAC. The SCB MAC handles all downstream broadcast traffic, but is never used in the upstream direction for client traffic, except for client registration. Optional higher layers may be implemented to perform selective broadcast of frames. Such layers may require additional MACs (multicast MACs) to be instantiated in the OLT for some or all ONUs increasing the total number of MACs beyond the number of ONUs + 1.

When connecting the SCB MAC to an 802.1D bridge port it is possible that loops may be formed due to the broadcast nature. Thus it is recommended that this MAC not be connected to an 802.1D bridge port.

Configuration of SCB channels as well as filtering and marking of frames for support of SCB is defined in Clause @@92.1.2.3.3.2@@ for 10G–EPON compliant Reconciliation Sublayers.

93.3.2.4 Delay requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent, however, a complying implementation shall maintain a delay variation of no more than 1 time_quantum through the implemented MAC stack.

The OLT shall not grant less than 1024 time_quanta into the future, in order to allow the ONU processing time when it receives a gate message. The ONU shall process all messages in less than this period. The OLT shall not issue more than one message every 1024 time_quanta to a single ONU. The unit of time_quantum is defined in Subclause 93.2.2.1.

93.3.3 Discovery Processing

Discovery is the process whereby newly connected or off–line ONUs are provided access to the PON. The process is driven by the OLT, which periodically makes available Discovery Windows during which off–line ONUs are given the opportunity to make themselves known to the OLT. The periodicity of these windows is unspecified and left up to the implementor. The OLT signifies that a discovery period is occurring by broadcasting a discovery GATE MPCPDU, which includes the starting time and length of the discovery window, along with the Discovery Information flag field, as defined in Clause 93.3.6.1. With the appropriate settings of individual flags contained in this 16 bit wide field, the OLT notifies all the ONUs about its upstream and downstream channel transmission capabilities. Note that the OLT may simultaneously support more than one data rate in the given transmission direction.

Off–line ONUs, upon receiving a Discovery GATE MPCPDU, wait for the period to begin and then transmit a REGISTER_REQ MPCPDU to the OLT. Discovery windows are unique in that they are the only times where multiple ONUs can access the PON simultaneously, and transmission overlap can occur. In order to reduce transmission overlaps, a contention algorithm is used by all ONUs. Measures are taken to reduce the probability for overlaps by artificially simulating a random distribution of distances from the OLT. Each ONU waits a random amount of time before transmitting the REGISTER_REQ MPCPDU that is shorter than the length of the discovery window. It should be noted that multiple valid REGISTER_REQ MPCPDUs can be received by the OLT during a single discovery window. Included in the REGISTER_REQ MPCPDU is the ONU's MAC address and number of maximum pending grants. Additionally, a registering ONU notifies the OLT on its transmission capabilities in the upstream and downstream channels by setting appropriately the flags in the Discovery Information field, as specified in Subclause 93.3.6.3.

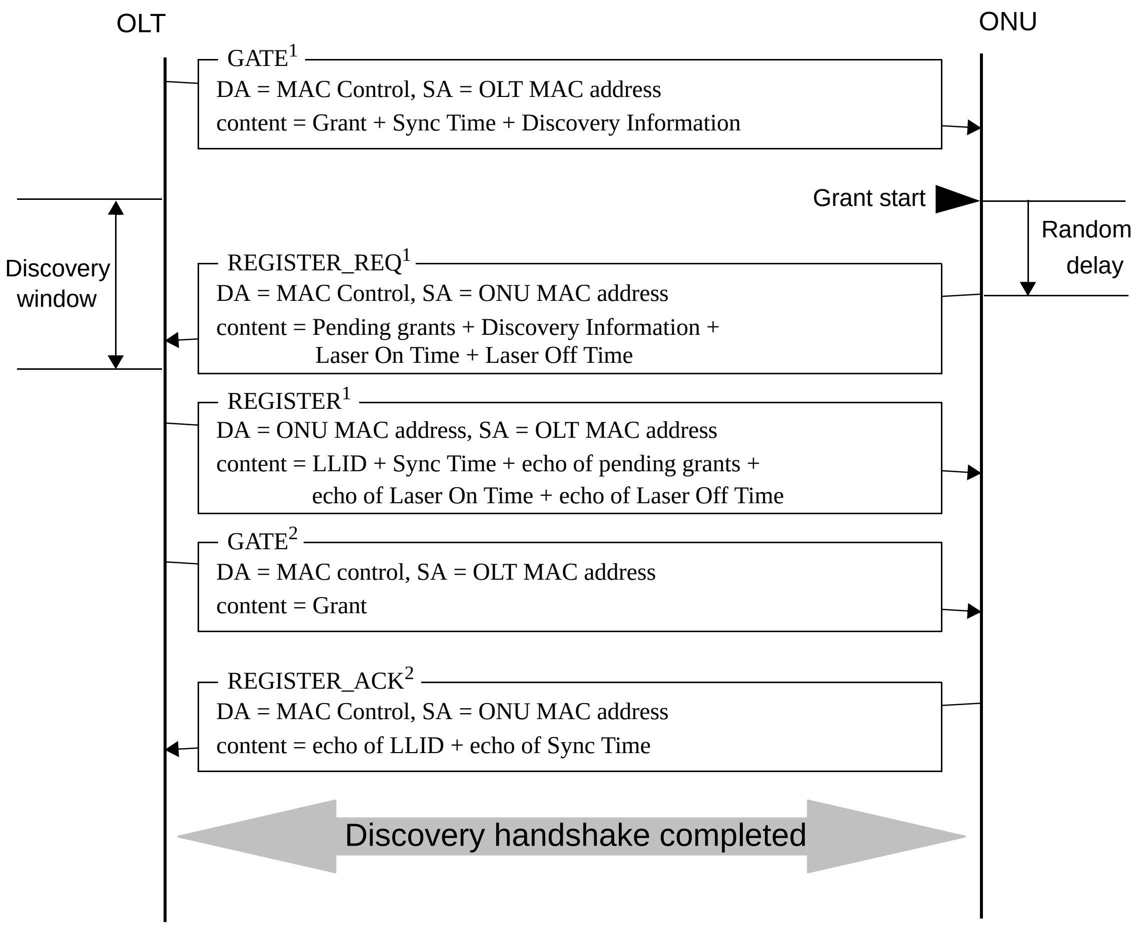
Note that even though a compliant ONU is not prohibited from supporting more than one data rate in any transmission channel, it is expected that a single supported data rate for upstream and downstream channel will be indicated in the Discovery Information field. Moreover, in order to assure maximum utilization of the upstream channel and to decrease the required size of the guard band between individual data bursts, the registering ONU notifies the OLT of the laser on / off times, by setting appropriate values in the Laser On Time and Laser Off Time fields, where both values are expressed in the units of time_quanta.

Upon receipt of a valid REGISTER_REQ MPCPDU, the OLT registers the ONU, allocating and assigning new port identities (LLIDs), and bonding corresponding MACs to the LLIDs.

The next step in the process is for the OLT to transmit a REGISTER MPCPDU to the newly discovered ONU, which contains the ONU's LLID, and the OLT's required synchronization time. Also, the OLT echoes the maximum number of pending grants, laser on time and laser off time. Note that the echoed parameter values i.e. required OLT synchronization time and laser on/off times are delivered to the registering ONU for confirmation purposes only and their utilization is not prescribed in this specification.

The OLT now has enough information to schedule the ONU for access to the PON and transmits a standard GATE message allowing the ONU to transmit a REGISTER_ACK. Upon receipt of the REGISTER_ACK, the discovery process for that ONU is complete, the ONU is registered and normal message traffic can begin. It is the responsibility of Layer Management to perform the MAC bonding, and start transmission from/to the newly registered ONU. The discovery message exchange is illustrated in Figure 93–14.

There may exist situations when the OLT requires that an ONU go through the discovery sequence again and reregister. Similarly, there may be situations where an ONU needs to inform the OLT of its desire to deregister. The ONU can then reregister by going through the discovery sequence. For the OLT, the REGISTER message may indicate a value, Reregister or Deregister, that if either is specified will force the receiving ONU into reregistering. For the ONU, the REGISTER_REQ message contains the Deregister bit that signifies to the OLT that this ONU should be deregistered.



[1] Messages sent on a broadcast channel
[2] Messages sent on unicast channels

Figure 93–14—Discovery Handshake Message Exchange

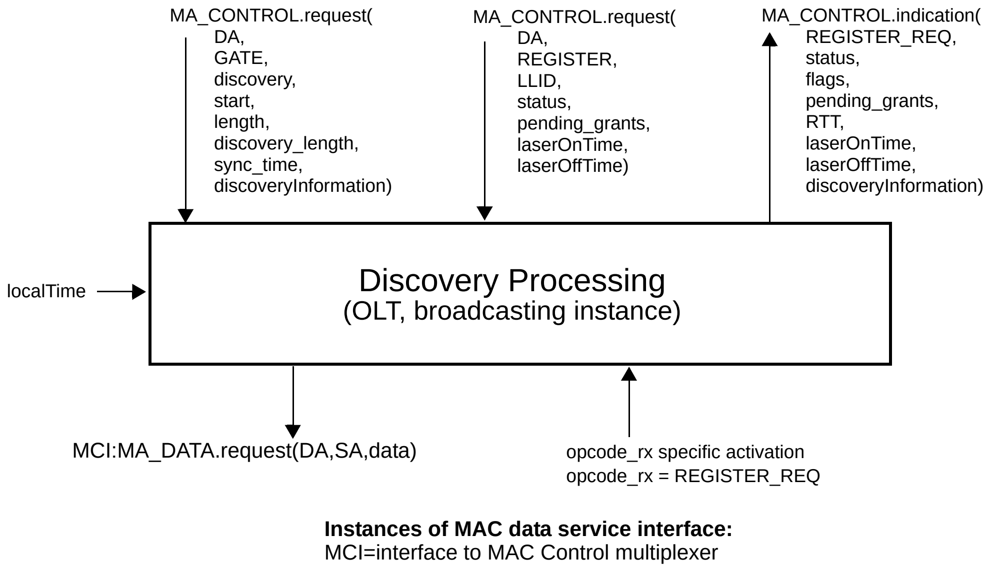


Figure 93–15—Discovery Processing Service Interfaces (OLT, broadcasting instance)

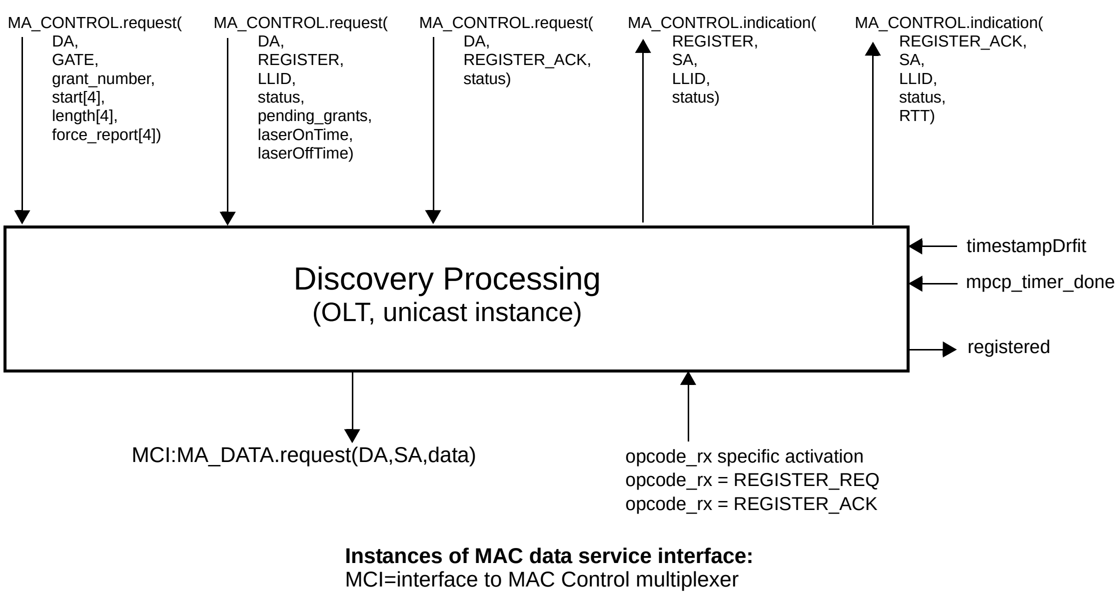


Figure 93–16—Discovery Processing Service Interfaces (OLT, unicasting instance)

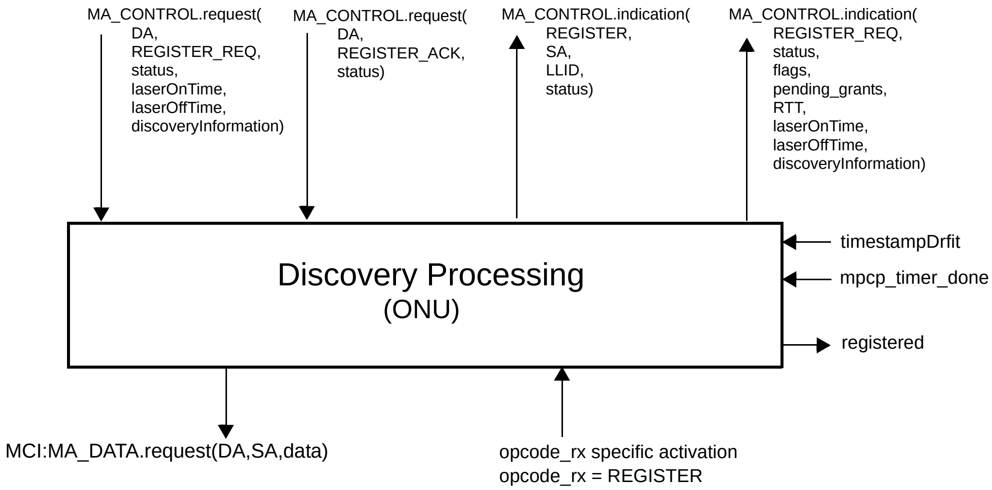


Figure 93–17—Discovery Processing Service Interfaces (ONU)

93.3.3.1 Constants

laserOffTimeCapability

TYPE: 8 bit unsigned

This constant represents the time required to terminate the laser, in units of time_quantum. While the default value corresponds to a maximum allowed T_{off} (as specified in @@Table 91-8@@ and @@Table 91-9@@), implementations may set it to the actual value time period required for turning off the PMD, as specified in @@Subclause 91.9.15@@.

VALUE: 0x20 (512 ns, default value)

laserOnTimeCapability

TYPE: 8 bit unsigned

This constant represents the time required to terminate the laser, in units of time_quantum. While the default value corresponds to a maximum allowed T_{on} (as specified in @@Table 91-8@@ and @@Table 91-9@@), implementations may set it to the actual value time period required for turning off the PMD, as specified in @@Subclause 91.9.15@@.

VALUE: 0x20 (512 ns, default value)

93.3.3.2 Variables

BEGIN

This variable is defined in Subclause 93.2.2.3.

data_rx

This variable is defined in Subclause 93.2.2.3.

data_tx

This variable is defined in Subclause 93.2.2.3.

grantEndTime

TYPE: 32 bit unsigned

This variable holds the time at which the OLT expects the ONU grant to complete. Failure of a REGISTER_ACK message from an ONU to arrive at the OLT before grantEndTime is a fatal error in the discovery process, and causes registration to fail for the specified ONU, who may then retry to register. The value of grantEndTime is measured in units of time_quantum.

insideDiscoveryWindow
TYPE: Boolean
This variable holds the current status of the discovery window. It is set to true when the discovery window opens, and is set to false when the discovery window closes.

laserOffTime
TYPE: 8 bit unsigned
This variable holds the time required to terminate the laser. It counts in time_quanta units the time period required for turning off the PMD, as specified in @@Subclause 91.9.15@@.
VALUE: 0x20 (512 ns, default value)

laserOnTime
TYPE: 8 bit unsigned
This variable holds the time required to initiate the PMD. It counts in time_quanta units the time period required for turning on the PMD, as specified in @@Subclause 91.9.15@@.
VALUE: 0x20 (512 ns, default value)

localTime
This variable is defined in Subclause 93.2.2.2.

opcode_rx
This variable is defined in Subclause 93.2.2.3.

opcode_tx
This variable is defined in Subclause 93.2.2.3.

pendingGrants
TYPE: 16 bit unsigned
This variable holds the maximum number of pending grants that an ONU is able to queue.

registered
TYPE: Boolean
This variable holds the current result of the Discovery Process. It is set to true once the discovery process is complete and registration is acknowledged.

syncTime
TYPE: 16 bit unsigned
This variable holds the time required to stabilize the receiver at the OLT. It counts time_quanta units from the point where transmission output is stable to the point where synchronization has been achieved. The value of syncTime includes gain adjustment interval ($T_{receiver\_settling}$), clock synchronization interval (T_{cdr}), and code–group alignment interval ($T_{code\_group\_align}$), as specified in @@Subclause 91.9.15@@. The OLT conveys the value of syncTime to ONUs in Discovery GATE and REGISTER messages. During the synchronization time an asymmetric 10/1 Gb/s ONU transmits only IDLE patterns, and a symmetric 10 Gb/s ONU sends a synchronization pattern of 0x55 (transmission bit sequence 1010 ...) followed by a burst delimiter and idle blocks as defined in Subclause @@92.2.3.5@@.

timestampDrift

This variable is defined in Subclause 93.2.2.3.

93.3.3.3 Functions

None.

93.3.3.4 Timers

discovery_window_size_timer

This timer is used to wait for the event signaling the end of the discovery window.

VALUE: The timer value is set dynamically based on the parameters received in a DISCOVERY GATE message.

mpcp_timer

This timer is used to measure the arrival rate of MPCP frames in the link. Failure to receive frames is considered a fatal fault and leads to deregistration.

93.3.3.5 Messages

MA_DATA.indication(DA, SA, m_sdu, receiveStatus)

The service primitive is defined in @@Subclause 2.3.2@@.

MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in @@Subclause 2.3.2@@.

MA_CONTROL.request(DA, GATE, discovery, start, length, discovery_length, sync_time, discoveryInformation)

The service primitive used by the MAC Control client at the OLT to initiate the Discovery Process. This primitive takes the following parameters:

DA: multicast or unicast MAC address.
GATE: opcode for GATE MPCPDU as defined in @@Table 31A–1@@.
discovery: flag specifying that the given GATE message is to be used for discovery only.
start: start time of the discovery window.
length: length of the grant given for discovery.
discovery_length: length of the discovery window process.
sync_time: the time interval required to stabilize the receiver at the OLT.
discoveryInformation: this parameter represents the Discovery Information field in GATE MPCPDU as specified in @@Subclause 93.3.6.1@@, defining the speed(s) the OLT is capable of receiving and speed(s) at which the discovery window will open for.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])

This service primitive is used by the MAC Control client at the OLT to issue the GATE message to an ONU. This primitive takes the following parameters:

DA: multicast MAC Control address as defined in @@Annex 31B@@.
GATE: opcode for GATE MPCPDU as defined in @@Table 31A–1@@.
grant_number: number of grants issued with this GATE message. The number of grants ranges from 0 to 4.
start[4]: start times of the individual grants. Only the first grant_number elements of the array are used.
length[4]: lengths of the individual grants. Only the first grant_number elements of the array are used.

force_report[4]: flags indicating whether a REPORT message should be generated in the corresponding grant. Only the first grant_number elements of the array are used.

MA_CONTROL.request(DA, REGISTER_REQ, status, laserOnTime, laserOffTime, discoveryInformation)

The service primitive used by a client at the ONU to request the Discovery Process to perform a registration. This primitive takes the following parameters:

DA: multicast MAC Control address as defined in @@Annex 31B@@.

REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in @@Table 31A–1@@.

status: This parameter takes on the indication supplied by the flags field in the REGISTER_REQ MPCPDU as defined in Table 93–6.

laserOnTime: this parameter holds the laserOnTime value, expressed in units of time_quanta, as reported by MAC client and specified in @@Subclause 93.3.6.3@@.

laserOffTime: this parameter holds the laserOffTime value, expressed in units of time_quanta, as reported by MAC client and specified in @@Subclause 93.3.6.3@@.

discoveryInformation: this parameter represents the Discovery Information field, as specified in @@Subclause 93.3.6.3@@, defining the speed(s) the ONU is capable of transmitting and speed(s) at which the registration attempt shall be made.

MA_CONTROL.indication(REGISTER_REQ, status, flags, pending_grants, RTT, discoveryInformation, laserOnTime, laserOffTime)

The service primitive issued by the Discovery Process to notify the client and Layer Management that the registration process is in progress. This primitive takes the following parameters:

REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in @@Table 31A–1@@.

status: This parameter holds the values incoming or retry. Value incoming is used at the OLT to signal that a REGISTER_REQ message was received successfully. The value retry is used at the ONU to signal to the client that a registration attempt failed and will be repeated.

flags: This parameter holds the contents of the flags field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process is in the OLT.

pending_grants: This parameters holds the contents of the pending_grants field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

RTT: The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

laserOnTime: This parameter holds the contents of the laserOnTime field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

laserOffTime: This parameter holds the contents of the laserOffTime field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

discoveryInformation: this parameter holds the contents of the Discovery Information field in the REGISTER_REQ MPCPDU. This parameter holds a valid value only when the primitive is generated by the Discovery process in the OLT.

MA_CONTROL.request(DA, REGISTER, LLID, status, pending_grants, laserOnTime, laserOffTime)

The service primitive used by the MAC Control client at the OLT to initiate acceptance of an ONU. This primitive takes the following parameters:

DA: unicast MAC address or multicast MAC Control address as defined in @@Annex 31B@@.
REGISTER: opcode for REGISTER MPCPDU as defined in @@Table 31A–1@@.
LLID: this parameter holds the logical link identification number assigned by the MAC Control client.
status: this parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 93–8.
pending_grants: this parameters echoes back the pending_grants field that was previously received in the REGISTER_REQ message.
laserOnTime: this parameter echoes back the laserOnTime field that was previously received in the REGISTER_REQ MPCPDU from the same MAC. This parameter has the default value of 0.
laserOffTime: this parameter echoes back the laserOffTime field that was previously received in the REGISTER_REQ MPCPDU from the same MAC. This parameter has the default value of 0.

MA_CONTROL.indication(REGISTER, SA, LLID, status)

This service primitive is issued by the Discovery Process at the OLT or an ONU to notify the MAC Control client and Layer Management of the result of the change in registration status. This primitive takes the following parameters:
REGISTER: opcode for REGISTER MPCPDU as defined in @@Table 31A–1@@.
SA: This parameter represents is the MAC address of the OLT.
LLID: This parameter holds the logical link identification number assigned by the MAC Control client.
status: This parameter holds the value of accepted/denied/deregistered/reregistered.

MA_CONTROL.request(DA, REGISTER_ACK, status)

This service primitive is issued by the MAC Control clients at the ONU and the OLT to acknowledge the registration. This primitive takes the following parameters:
DA: multicast MAC Control address as defined in @@Annex 31B@@.
REGISTER_ACK: opcode for REGISTER_ACK MPCPDU as defined in @@Table 31A–1@@.
status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 93–9.

MA_CONTROL.indication(REGISTER_ACK, SA, LLID, status, RTT)

This service primitive is issued by the Discovery Process at the OLT to notify the client and Layer Management that the registration process has completed. This primitive takes the following parameters:
REGISTER_ACK: opcode for REGISTER_ACK MPCPDU as defined in @@Table 31A–1@@.
SA: This parameter represents the MAC address of the reciprocating device (ONU address at the OLT, and OLT address at the ONU).
LLID: This parameter holds the logical link identification number assigned by the MAC Control client.
status: This parameter holds the value of accepted/denied/reset/deregistered.
RTT: The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the invoking Discovery Process is in the OLT

Opcode–specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

93.3.3.6 State Diagram

Discovery Process in the OLT shall implement the discovery window setup state diagram shown in Figure 93–18, request processing state diagram as shown in Figure 93–19, register processing state diagram as shown in Figure 93–20, and final registration state diagram as shown in Figure 93–21. The discovery process in the ONU shall implement registration state diagram as shown in Figure 93–22.

Instantiation of state diagrams as described in Figure 93–18, Figure 93–19, and Figure 93–20 is performed only at the Multipoint MAC Control instances attached to the appropriate broadcast LLID(s) (0x7FFF and/or 0x7FFE for EPON and 10G–EPON, respectively). Instantiation of state diagrams as described in Figure 93–21 and Figure 93–22 is performed for every Multipoint MAC Control instance, except the instance attached to the broadcast channel.

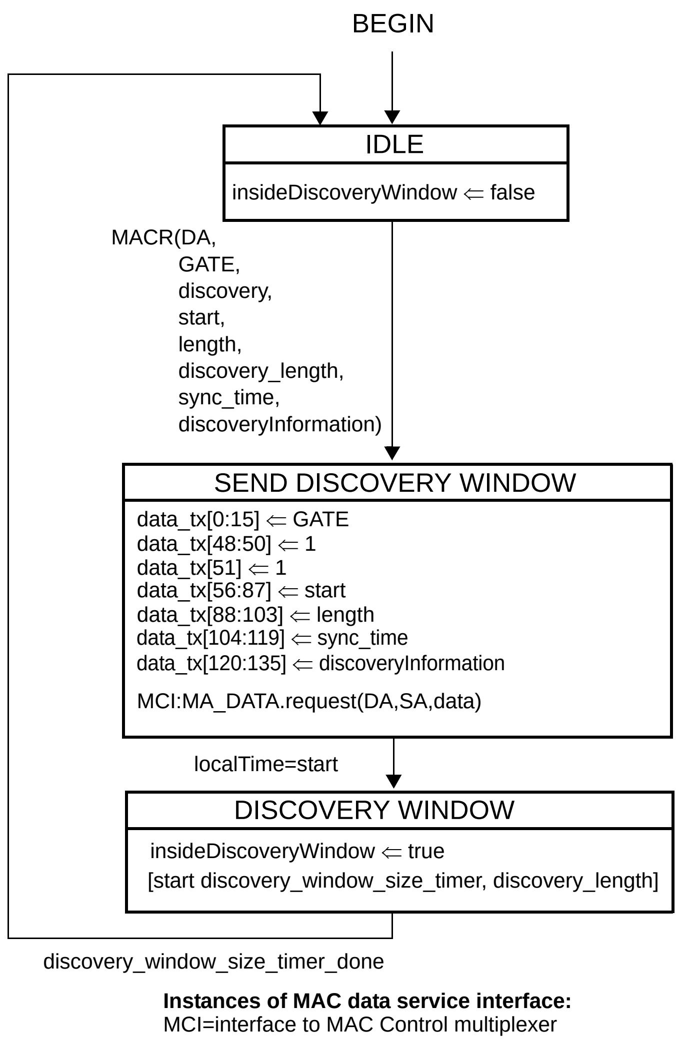


Figure 93–18—Discovery Processing OLT Window Setup state diagram

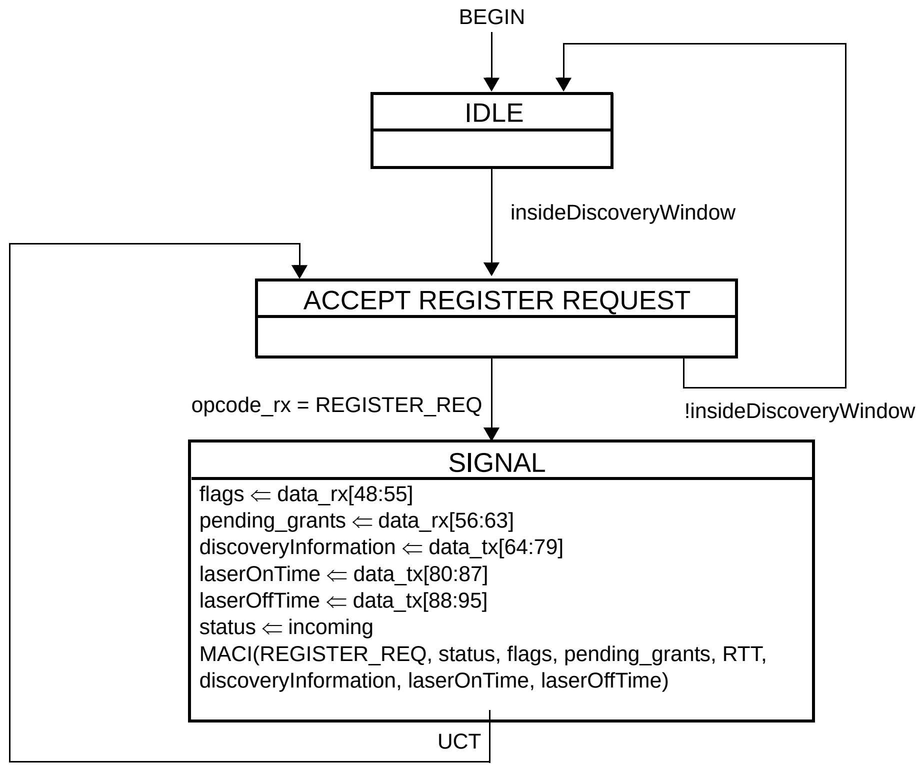
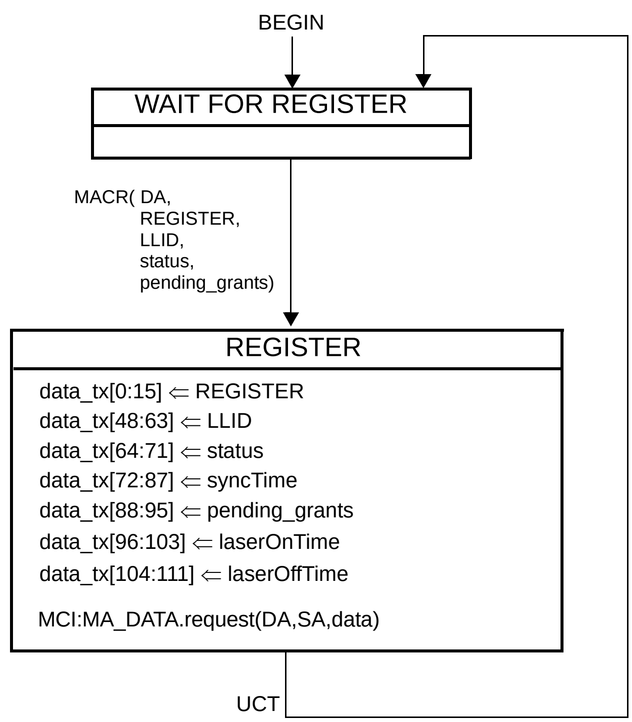
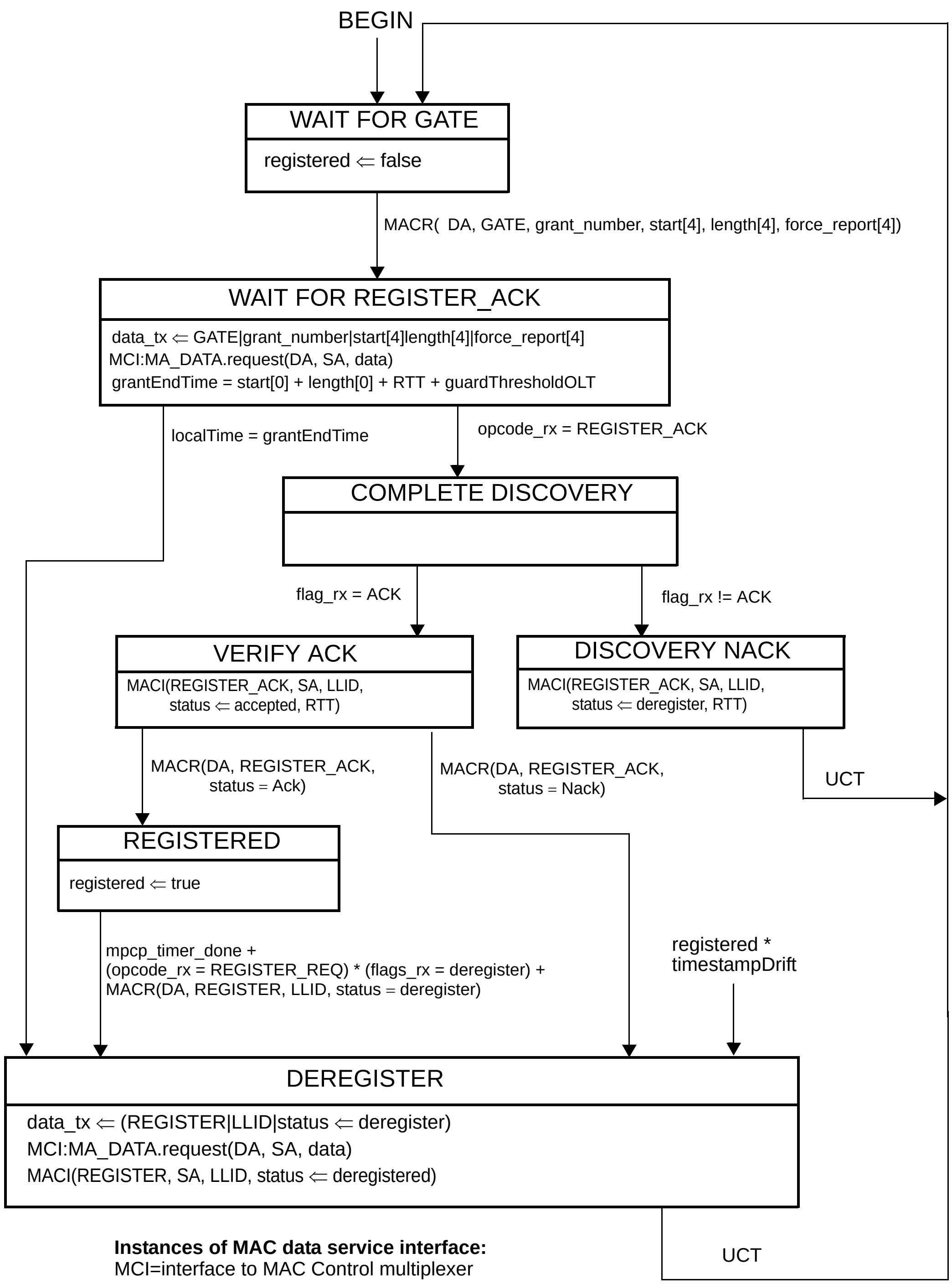


Figure 93–19—Discovery Processing OLT Process Requests state diagram



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 93–20—Discovery Processing OLT Register state diagram



NOTE— The MAC Control Client issues the grant following the REGISTER message, taking the ONU processing delay of REGISTER message into consideration.

Figure 93–21—Discovery Processing OLT Final Registration state diagram

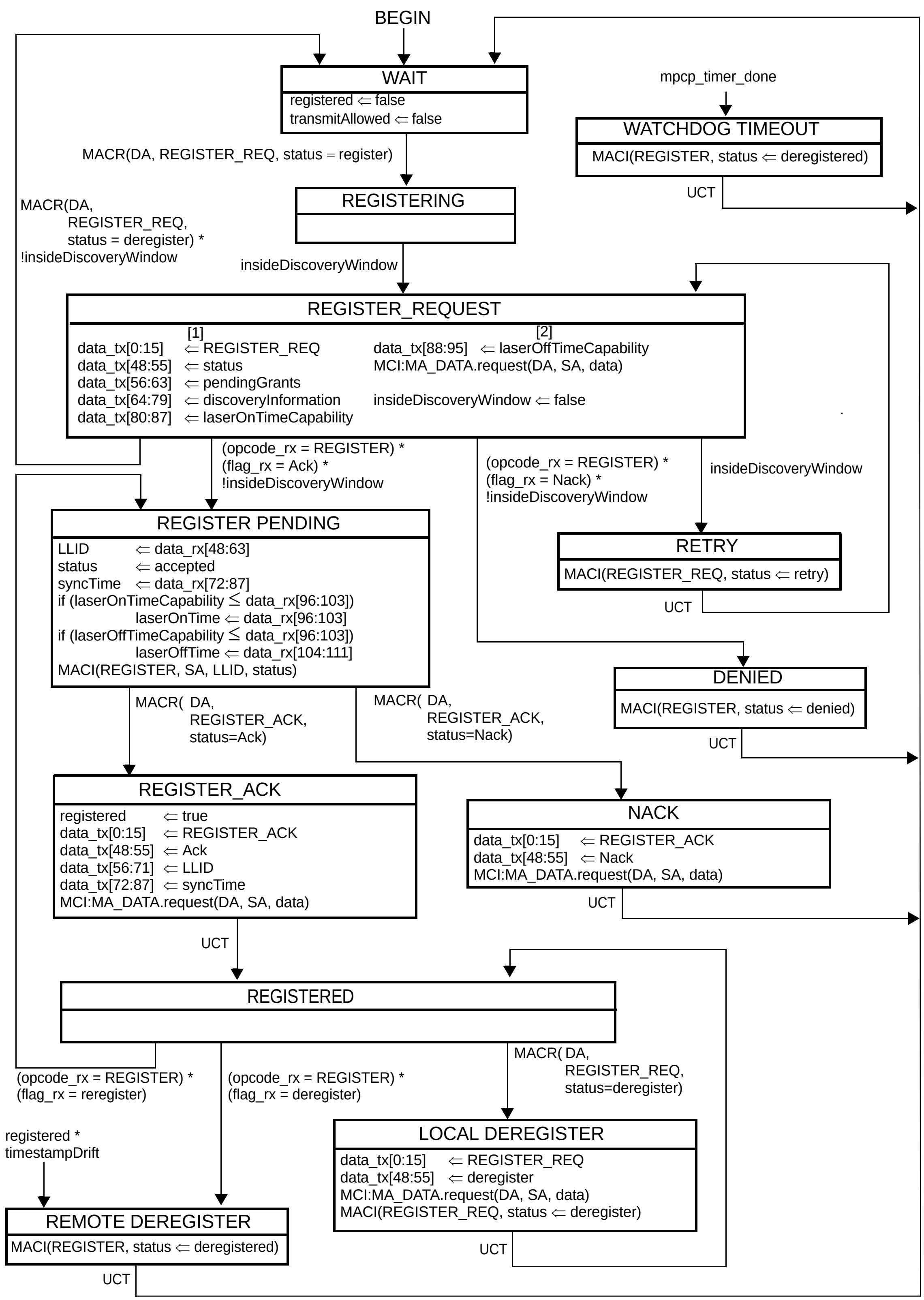


Figure 93–22—Discovery Processing ONU Registration state diagram

93.3.4 Report Processing

The Report Processing functional block has the responsibility of dealing with queue report generation and termination in the network. Reports are generated by higher layers and passed to the MAC Control sublayer by the MAC Control clients. Status reports are used to signal bandwidth needs as well as for arming the OLT watchdog timer.

Reports shall be generated periodically, even when no request for bandwidth is being made. This keeps a watchdog timer in the OLT from expiring and deregistering the ONU. For proper operation of this mechanism the OLT shall grant the ONU periodically.

The Report Processing functional block, and its MPCP protocol elements are designed for use in conjunction with an IEEE 802.1P capable bridge.

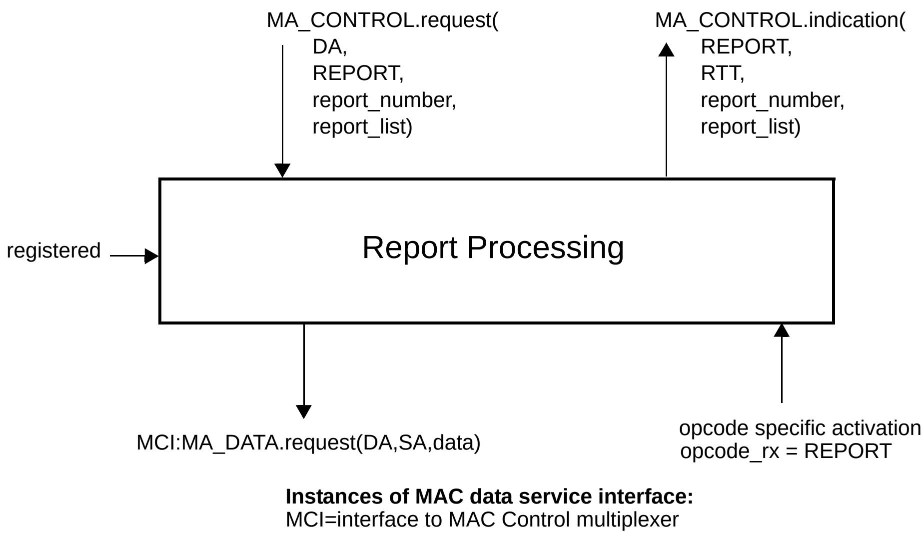


Figure 93–23—Report Processing Service Interfaces

93.3.4.1 Constants

mpcp_timeout
TYPE: 32 bit unsigned
This constant represents the maximum allowed interval of time between two MPCPDU messages. Failure to receive at least one frame within this interval is considered a fatal fault and leads to deregistration.
VALUE: 0x03B9ACA0 (1 second)

report_timeout
TYPE: 32–bit unsigned
This constant represents the maximum allowed interval of time between two REPORT messages generated by the ONU.
VALUE: 0x002FAF08 (50 milliseconds)

93.3.4.2 Variables

BEGIN
TYPE: Boolean

This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

data_rx
This variable is defined in Subclause 93.2.2.3.

data_tx
This variable is defined in Subclause 93.2.2.3.

opcode_rx
This variable is defined in Subclause 93.2.2.3.

opcode_tx
This variable is defined in Subclause 93.2.2.3.

registered
This variable is defined in Subclause 93.3.3.2.

93.3.4.3 Functions

None.

93.3.4.4 Timers

report_periodic_timer
ONUs are required to generate REPORT MPCPDUs with a periodicity of less than report_timeout value. This timer counts down time remaining before a forced generation of a REPORT message in an ONU.

mpcp_timer
This timer is defined in Subclause 93.3.3.4.

93.3.4.5 Messages

MA_DATA.request (DA, SA, m_sdu)
The service primitive is defined in @@Subclause 2.3.2@@.

MA_CONTROL.request(DA, REPORT, report_number, report_list)
This service primitive is used by a MAC Control client to request the Report Process at the ONU to transmit a queue status report. This primitive may be called at variable intervals, independently of the granting process, in order to reflect the time varying aspect of the network. This primitive uses the following parameters:
DA: multicast MAC Control address as defined in @@Annex 31B@@.
REPORT: opcode for REPORT MPCPDU as defined in @@Table 31A–1@@.
report_number: the number of queue status report sets located in report list.
The report_number value ranges from 0 to a maximum of 13.
report_list: the list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid, is a Boolean array with length of 8, ‘0’ or false indicates that the corresponding status field is not present (the length of status field is 0), while ‘1’ or true indicates that the corresponding status field is present (the length of status field is 2 octets). The index of the array is meant to reflect the same numbered priority queue in the IEEE 802.1P nomenclature. The parameter status is an array of 16–bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

MA_CONTROL.indication(REPORT, RTT, report_number, report_list)

The service primitive issued by the Report Process at the OLT to notify the MAC Control client and higher layers the queue status of the MPCP link partner. This primitive may be called multiple times, in order to reflect the time–varying aspect of the network. This primitive uses the following parameters:

REPORT: opcode for REPORT MPCPDU as defined in @@Table 31A–1@@.

RTT: this parameter holds an updated round trip time value which is recalculated following each REPORT message reception.

report_number: the number of queue status report sets located in report list. The report_number value ranges from 0 to a maximum of 13.

report_list: the list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid, is a Boolean array with length of 8, ‘0’ or false indicates that the corresponding status field is not present (the length of status field is 0), while ‘1’ or true indicates that the corresponding status field is present (the length of status field is 2 octets). The index of the array is meant to reflect the same numbered priority queue in the IEEE 802.1P nomenclature.

The parameter status is an array of 16–bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

Opcode–specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

93.3.4.6 State Diagram

The report process in the OLT shall implement the report processing state diagram as shown in Figure 93–24. The report process in the ONU shall implement the report processing state diagram as shown in Figure 93–25. Instantiation of state diagrams as described is performed for Multipoint MAC Control instances attached to unicast LLIDs only.

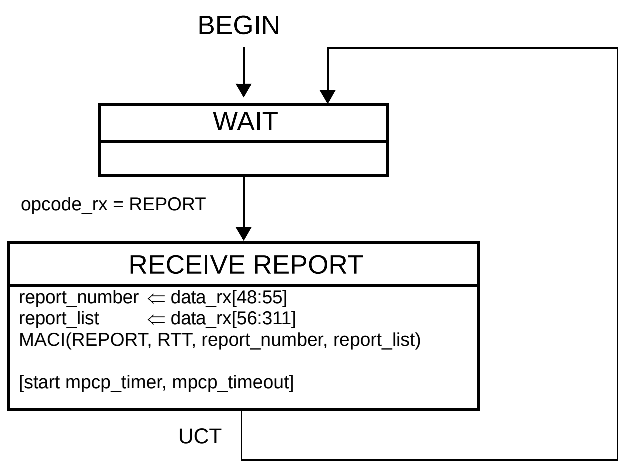
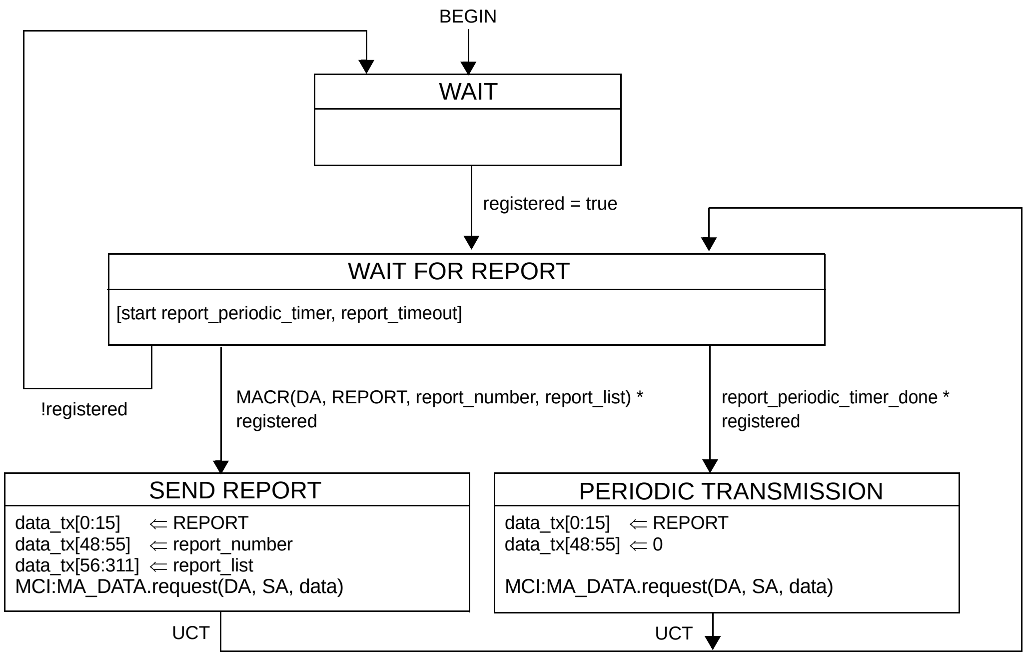


Figure 93–24—Report Processing state diagram at OLT



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 93–25—Report Processing state diagram at ONU

93.3.5 Gate Processing

A key concept pervasive in Multipoint MAC Control is the ability to arbitrate a single transmitter out of a plurality of ONUs. The OLT controls an ONU's transmission by the assigning of grants.

The transmitting window of an ONU is indicated in GATE message where start time and length are specified. An ONU will begin transmission when its localTime counter matches start_time value indicated in the GATE message. An ONU will conclude its transmission with sufficient margin to ensure that the laser is turned off before the grant length interval has elapsed.

Multiple outstanding grants may be issued to each ONU. The OLT shall not issue more than the maximum supported maximum outstanding grants as advertised by the ONU during registration (see pending grants in Subclause 93.3.6.3).

In order to maintain the watchdog timer at the ONU, grants are periodically generated. For this purpose empty GATE messages may be issued periodically.

When registered, the ONU ignores all gate messages where the discovery flag is set.

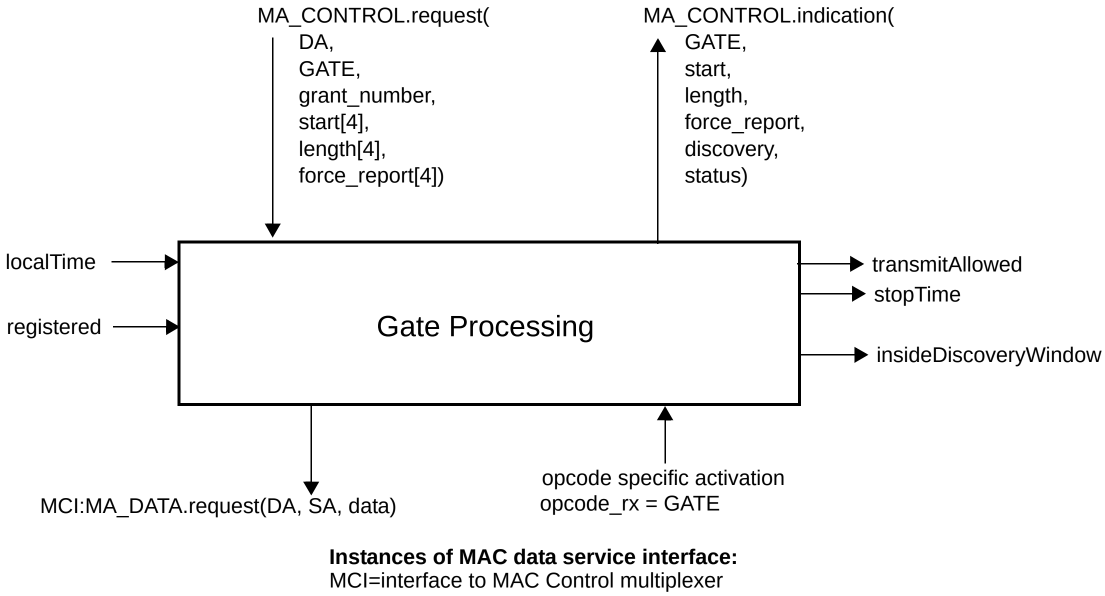


Figure 93–26—Gate Processing Service Interface

93.3.5.1 Constants

discoveryGrantLength

TYPE: 32 bit unsigned

This constant represents the duration of ONU's transmission during discovery attempt. The value of discoveryGrantLength includes MPCPDU transmission time and tailGuard as defined in Subclause 93.2.2.1. discoveryGrantLength is represented in units of time_quanta.

VALUE: 0x00000005 (672 bits)

gate_timeout

TYPE: 32–bit unsigned

This constant represents the maximum allowed interval of time between two GATE messages generated by the OLT to the same ONU.

VALUE: 0x002FAF08 (50 milliseconds)

max_future_grant_time

TYPE: 32 bit unsigned

This constant holds the time limiting the future time horizon for a valid incoming grant.

VALUE: 0x03B9ACA0 (1 second)

min_processing_time

TYPE: 32 bit unsigned

This constant is the time required for the ONU processing time.

VALUE: 0x00000400 (16.384 us)

tqSize

This constant is defined in Subcluase 93.2.2.1.

93.3.5.2 Variables

BEGIN
TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

counter
TYPE: integer
This variable is used as a loop iterator counting the number of incoming grants in a GATE message.

currentGrant
TYPE: structure {
DA 48 bit unsigned, a.k.a MAC address type
start 32 bit unsigned
length 16 bit unsigned
force_reportBoolean
discoveryBoolean}
This variable is used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed. The state is a structure field composed of multiple subfields.

data_rx
This variable is defined in Subclause 93.2.2.3.

data_tx
This variable is defined in Subclause 93.2.2.3.

effectiveLength
TYPE: 32 bit unsigned
This variable is used for temporary storage of a normalized net time value. It holds the net effective length of a grant normalized for elapsed time, and compensated for the periods required to turn the laser on and off, and waiting for receiver lock.

grantList
TYPE: list of elements having the structure define in currentGrant
This variable is used for storage of the list of pending grants. It is dynamically set by the Gate Processing functional block and is not exposed. Each time a grant is received it is added to the list. The list elements are structure fields composed of multiple subfields. The list is indexed by the start subfield in each element for quick searches.

insideDiscoveryWindow
This variable is defined in Subclause 93.3.3.2.

maxDelay
TYPE: 16 bit unsigned
This variable holds the maximum delay that can be applied by an ONU before sending the REGISTER_REQ MPCPDU. This delay is calculated such that the ONU would have sufficient time to transmit the REGISTER_REQ message and its associated overhead (FEC parity date, end–of–frame sequence, etc.) and terminate the laser before the end of the discovery grant.
nextGrant
TYPE: element having same structure as defined in currentGrant
This variable is used for local storage of a pending grant state during processing. It is dynamically

set by the Gate Processing functional block and is not exposed. The content of the variable is the next grant to become active.

nextStopTime
TYPE: 32 bit unsigned
This variable holds the value of the localTime counter corresponding to the end of the next grant.

registered
This variable is defined in Subclause 93.3.3.2.

stopTime
This variable is defined in Subclause 93.2.2.3.

syncTime
This variable is defined in Subclause 93.3.3.2.

transmitAllowed
This variable is defined in Subclause 93.2.2.3.

93.3.5.3 Functions

empty(list)
This function is use to check whether the list is empty. When there are no elements queued in the list, the function returns true. Otherwise, a value of false is returned.

confirmDiscovery(data)
This functon is used to check whether the current Discovery Window is open for the given ONU (TRUE) or not (FALSE). This function returns values as shown in Table 93–2.

Table 93–2—Operation of the confirmDiscovery(data) function

OLT Discovery Information: Discovery Window		ONU Tx capability		confirmDiscovery(data) returns
1G	10G	1G	10G	
X	1	0	1	TRUE
1	X	1	0	TRUE
0	1	1	0	FALSE
1	0	0	1	FALSE

InsertInOrder(sorted_list, inserted_element)
This function is used to queue an element inside a sorted list. The queueing order is sorted. In the condition that the list is full the element may be discarded. The length of the list is dynamic and it's maximum size equals the value advertised during registration as maximum number of pending grants.

IsBroadcast(grant)
This function is used to check whether its argument represents a broadcast grant, i.e., grant given to multiple ONUs. This is determined by the destination MAC address of the corresponding GATE message. The function returns the value true when MAC address is a global assigned MAC Control address as defined in @@Annex 31B@@, and false otherwise.

PeekHead(sorted_list)

This function is used to check the content of a sorted list. It returns the element at the head of the list without dequeuing the element.

Random(r)

This function is used to compute a random integer number uniformly distributed between 0 and r. The randomly generated number is then returned by the function.

RemoveHead(sorted_list)

This function is used to dequeue an element from the head of a sorted list. The return value of the function is the dequeued element.

93.3.5.4 Timers

gntStTmr

This timer is used to wait for the event signaling the start of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant start time.

gntWinTmr

This timer is used to wait for the event signaling the end of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant length.

gate_periodic_timer

The OLT is required to generate GATE MPCPDUs with a periodicity of less than gate_timeout value. This timer counts down time remaining before a forced generation of a GATE message in the OLT.

mpcp_timer

This timer is defined in Subclause 93.3.3.4.

rndDlyTmr

This timer is used to measure a random delay inside the discovery window. The purpose of the delay is to apriori reduce the probability of transmission overlap during the registration process, and thus lowering the expectancy of registration time in the PON.
VALUE: A random value less than the net discovery window size less the REGISTER_REQ MPCPDU frame size less the idle period and laser turn on and off delays less the preamble size less the IFG size. The timer value is set dynamically based on the parameters passed from the client.

93.3.5.5 Messages

MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in @@Subclause 2.3.2@@.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])

This service primitive is defined in Subclause 93.3.3.5.

MA_CONTROL.indication(GATE, start, length, force_report, discovery, status)

This service primitive issued by the Gate Process at the ONU to notify the MAC Control client and higher layers that a grant is pending. This primitive is invoked multiple times when a single GATE message arrives with multiple grants. It is also generated at the start and end of each grant as it becomes active. This primitive uses the following parameters:

GATE: opcode for GATE MPCPDU as defined in @@Table 31A–1@@.
start: start time of the grant. This parameter is not present when the status value is deactive.
length: length of the grant. This parameter is not present when the status value is deactive.

force_report: flags indicating whether a REPORT message should be transmitted in this grant. This parameter is not present when the status value is deactive.

discovery: This parameter holds the value true when the grant is to be used for the discovery process, and false otherwise. This parameter is not present when the status value is deactive.

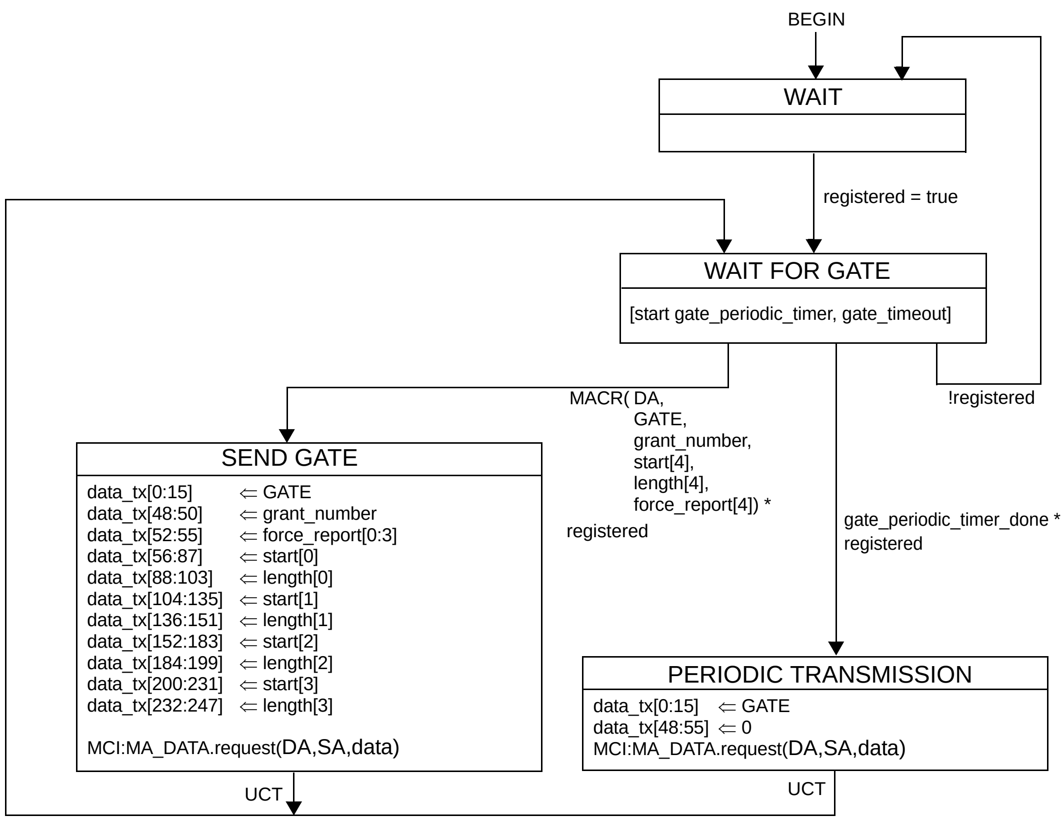
status: This parameter takes the value *arrive* on grant reception, *active* when a grant becomes active, and *deactive* at the end of a grant.

Opcode–specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

93.3.5.6 State Diagrams

The gating process in the OLT shall implement the gate processing state diagram as shown in Figure 93–27. The gating process in the ONU shall implement the gate processing state diagram as shown in Figure 93–28 and Figure 93–29. Instantiation of state diagrams as described is performed for all Multipoint MAC Control instances.



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 93–27—Gate Processing state diagram at OLT

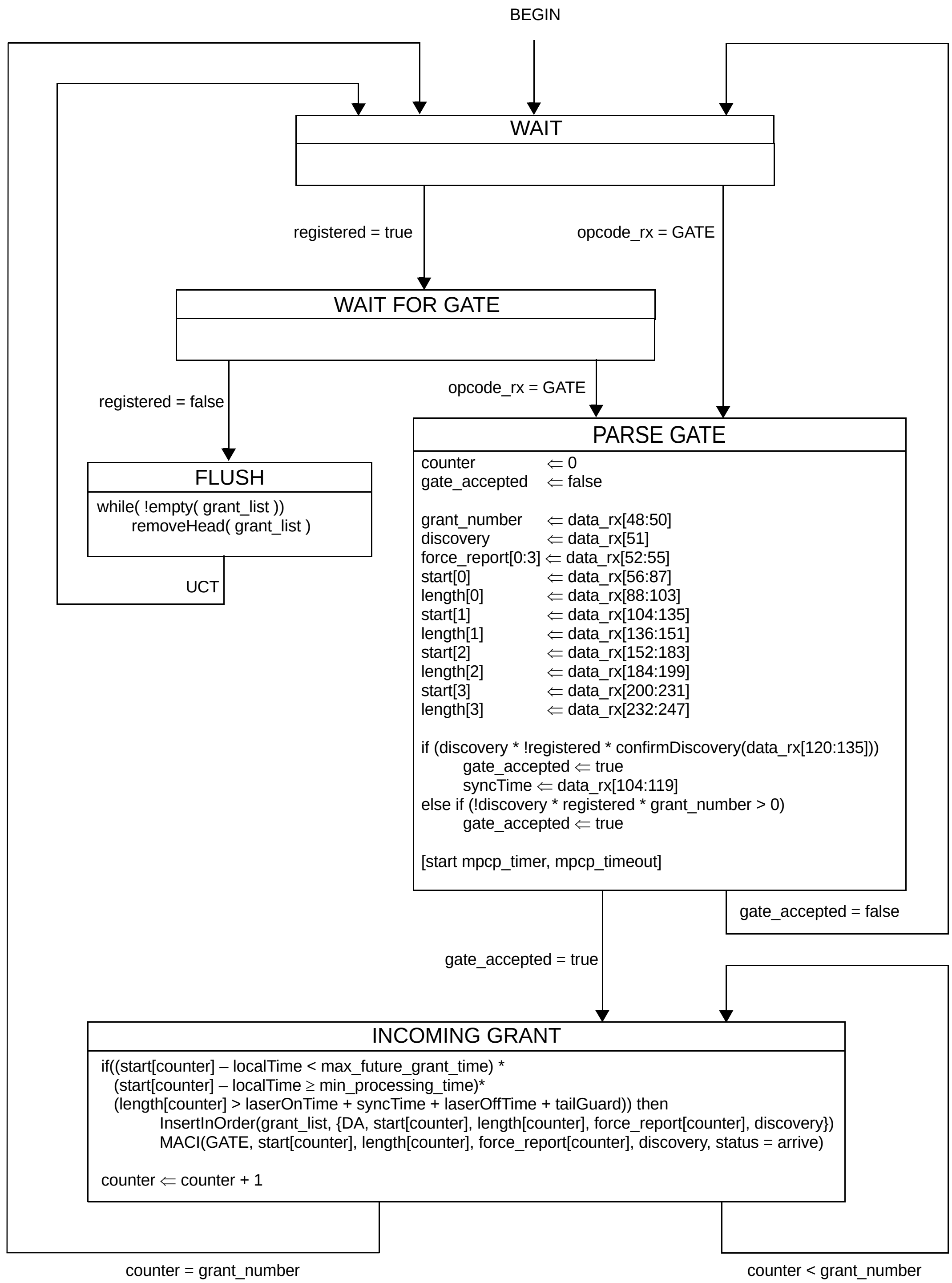


Figure 93–28—Gate Processing ONU Programing state diagram

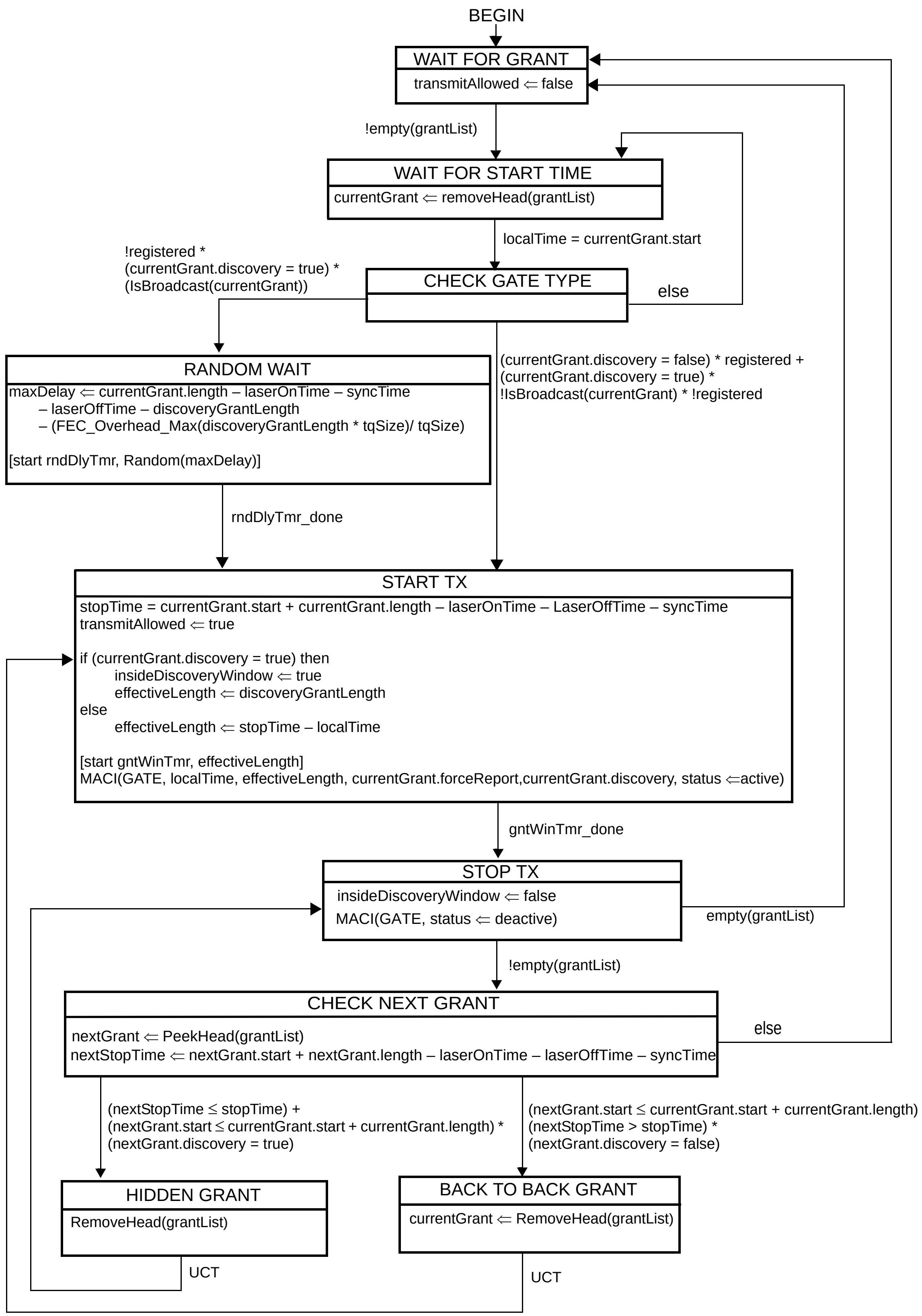


Figure 93–29—Gate Processing ONU Activation state diagram

93.3.6 MPCPDU structure and encoding

The MPCPDU structure shall be shown as in Figure 93–30, and is further defined in the following definitions:

a) Destination Address (DA). The DA in MPCPDU is the MAC Control Multicast address as specified in the annexes to @@Clause 31@@, or the individual MAC address associated with the port to which the MPCPDU is destined.
b) Source Address (SA). The SA in MPCPDU is the individual MAC address associated with the port through which the MPCPDU is transmitted. For MPCPDUs originating at the OLT end, this can be the address any of the individual MACs. These MACs may all share a single unicast address, as explained in Subclause 93.1.2.
c) Length/Type. MPCPDUs are always Type encoded, and carry the MAC_Control_Type field value as specified in @@Subclause 31.4.1.3@@.
d) Opcode. The opcode identifies the specific MPCPDU being encapsulated. Values are defined in @@Table 31A–1@@.
e) Timestamp. The timestamp field conveys the content of the localTime register at the time of transmission of the MPCPDUs. This field is 32 bits long and counts time in units of time_quanta.
f) Data/Reserved/PAD. These 40 octets are used for the payload of the MPCPDUs. When not used they would be filled with zeros on transmission, and be ignored on reception.
g) FCS. This field is the Frame Check Sequence, typically generated by the underlying MAC.

Based on the MAC instance used to generate the specific MPCPDU, the appropriate LLID shall be generated by the RS.

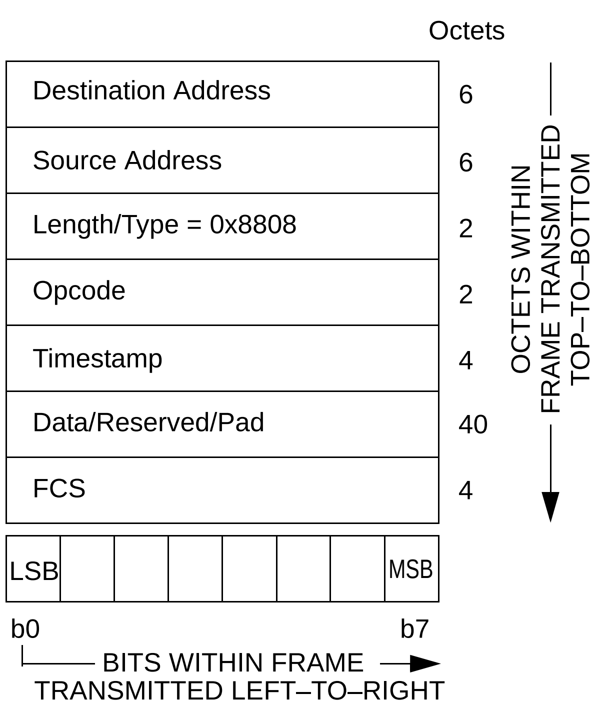


Figure 93–30—Generic MPCPDU

93.3.6.1 GATE description

The purpose of GATE message is to grant transmission windows to ONUs for both discovery messages and normal transmission. Up to four grants can be included in a single GATE message. The number of grants can also be set to zero for using the GATE message as an MPCP keep alive from OLT to the ONU.

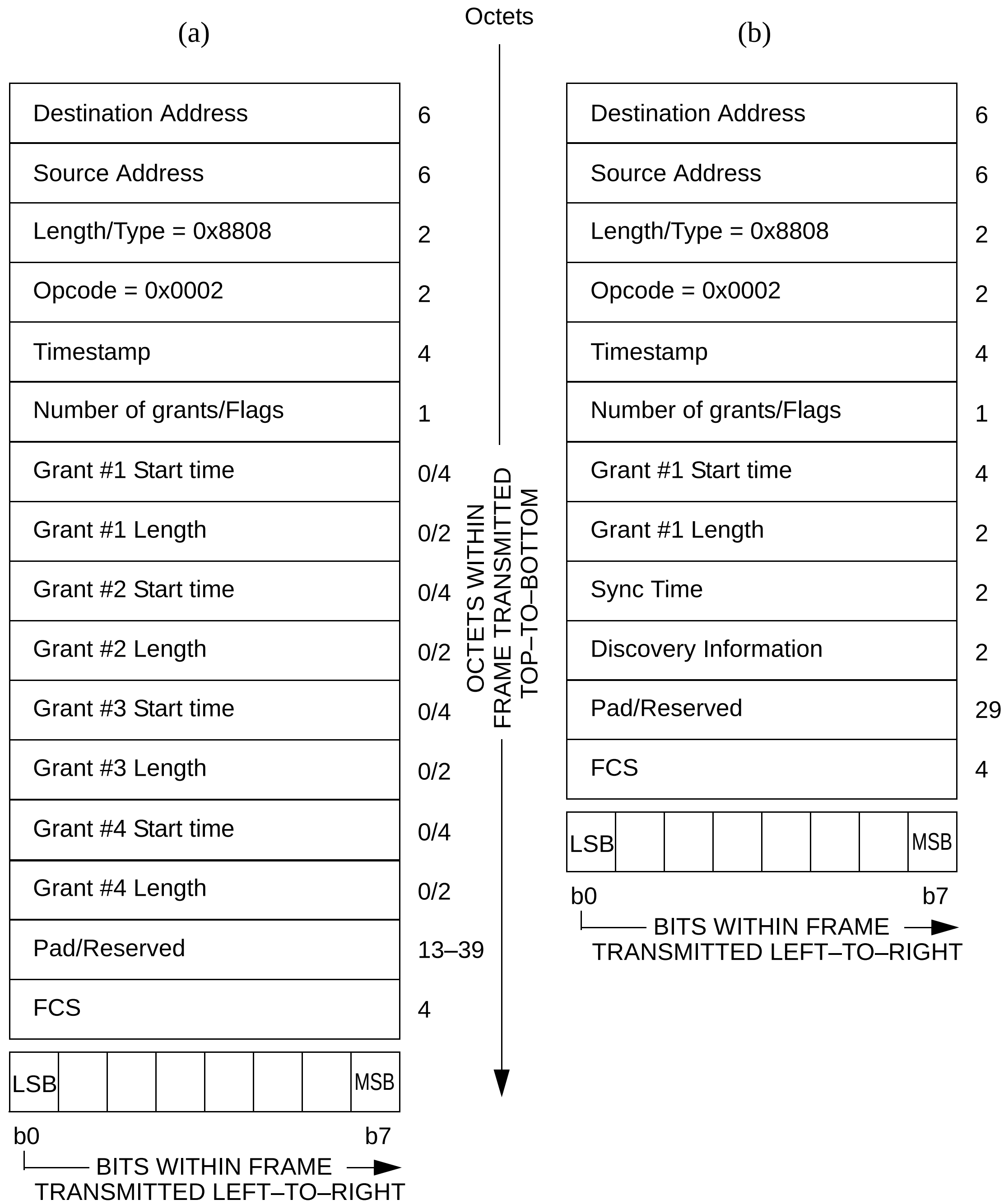


Figure 93–31—GATE MPCPDU: (a) normal GATE MPCPDU, (b) discovery GATE MPCPDU

The GATE MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the GATE MPCPDU is 0x0002.
b) Flags. This is an 8 bit flag register that holds the following flags: The Number of grants field contains the number of grants, composed of valid Length, Start Time pairs in this MPCPDU. This is a number between 0 and 4. Note: when Number of grants is set to 0, sole purpose of message is conveying of timestamp to ONU.
The Discovery flag field indicates that the signaled grants would be used for the discovery process, in which case a single grant shall be issued in the gate message.
The Force Report flag fields ask the ONU to issue a REPORT message related to the corresponding grant number at the corresponding transmission opportunity indicated in this GATE.
c) Grant #n Length. Length of the signaled grant, this is an 16 bit unsigned field. The length is counted in 1 time_quantum increments. There are 4 Grants that are possibly packed into the GATE MPCPDU. The laserOnTime, syncTime, and laserOffTime are included in and thus consume part of Grant #n Length.
d) Grant #n Start Time. Start time of the grant, this is an 32 bit unsigned field. The start time is compared to the local clock, to correlate the start of the grant. Transmitted values shall satisfy the condition Grant #n Start Time < Grant #n+1 Start Time for consecutive grants within the same GATE MPCPDU.
e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. During the synchronization time the ONU shall send a synchronization pattern of 0x55 (transmission bit sequence 1010 ...) followed by a burst delimiter and idle blocks as defined in @@Subclause 92.2.3.5@@. The value is counted in 1 time_quantum increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA and PCS. This field is present only when the gate is a discovery gate, as signaled by the Discovery flag and is not present otherwise.
f) Discovery Information. This is an 16 bit flag register. This field is present only when the gate is a discovery gate, as signaled by the Discovery flag and is not present otherwise. Table 93–3 presents the internal structure of the Discovery Information flag field.
g) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation. The size of this field depends on the used Grant #n Length/Start Time entry–pairs as well as the presence of the Sync Time and Discovery Information fields, and varies in length from 13 – 39 accordingly.

The GATE MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID, except when the discovery flag is set where the MAC Control instance is mapped to all ONUs and such frame is marked by the appropriate broadcast LLID (Subclause 93.3.2.3).

Table 93–3—GATE MPCPDU Discovery Information Fields

Bit	Flag Field	Values
0	OLT is 1G upstream capable	0 – OLT supports 1 Gb/s reception 1 – OLT does not support 1 Gb/s reception
1	OLT is 10G upstream capable	0 – OLT does not support 10 Gb/s reception 1 – OLT supports 10 Gb/s reception
2 – 3	reserved	Ignored on reception.
4	OLT is opening 1G discovery window	0 – OLT can receive 1 Gb/s data in this window 1 – OLT cannot receive 1 Gb/s data in this window
5	OLT is opening 10G discovery window	0 – OLT cannot receive 10 Gb/s data in this window 1 – OLT can receive 10 Gb/s data in this window
6 – 15	reserved	Ignored on reception.

Table 93–4—GATE MPCPDU Number of grants/Flags Fields

Bit	Flag Field	Values
0–2	Number of grants	0 – 4
3	Discovery	0 – Normal GATE 1 – Discovery GATE
4	Force Report Grant 1	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 1
5	Force Report Grant 2	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 2
6	Force Report Grant3	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 3
7	Force Report Grant 4	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 4

93.3.6.2 REPORT description

REPORT messages have several functionalities. Time stamp in each REPORT message is used for round trip (RTT) calculation. In the REPORT messages ONUs indicate the upstream bandwidth needs they request per 802.1Q priority queue. REPORT messages are also used as keep–alives from ONU to OLT. ONUs issue REPORT messages periodically in order to maintain link health at the OLT as defined in Subclause 93.3.4. In addition, the OLT may specifically request a REPORT message.

The REPORT MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REPORT MPCPDU is 0x0003.
b) Number of Queue Sets. This field specifies the number of requests in the REPORT message. A REPORT frame may hold multiple sets of Report bitmap and Queue #n as specified in the Number of Queue Sets field.
c) Report bitmap. This is an 8 bit flag register that indicates which queues are represented in this REPORT MPCPDU – see Table 93–5

Table 93–5—REPORT MPCPDU Report bitmap fields

Bit	Flag Field	Values
0	Queue 0	0 – queue 0 report is not present; 1 – queue 0 report is present
1	Queue 1	0 – queue 1 report is not present; 1 – queue 1 report is present
2	Queue 2	0 – queue 2 report is not present; 1 – queue 2 report is present
3	Queue 3	0 – queue 3 report is not present; 1 – queue 3 report is present
4	Queue 4	0 – queue 4 report is not present; 1 – queue 4 report is present
5	Queue 5	0 – queue 5 report is not present; 1 – queue 5 report is present
6	Queue 6	0 – queue 6 report is not present; 1 – queue 6 report is present

Table 93–5—REPORT MPCPDU Report bitmap fields

Bit	Flag Field	Values
7	Queue 7	0 – queue 7 report is not present; 1 – queue 7 report is present

d) Queue #n Report. This value represents the length of queue# n at time of REPORT message generation. The reported length shall be adjusted to account for the necessary inter–frame spacing. The Queue #n Report field is an unsigned 16 bit integer representing transmission request in units of time_quanta. This field is present only when the corresponding flag in the Report bitmap is set.

e) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation. The size of this field depends on the used Queue Report entries, and accordingly varies in length from 0 to 39.

The REPORT MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

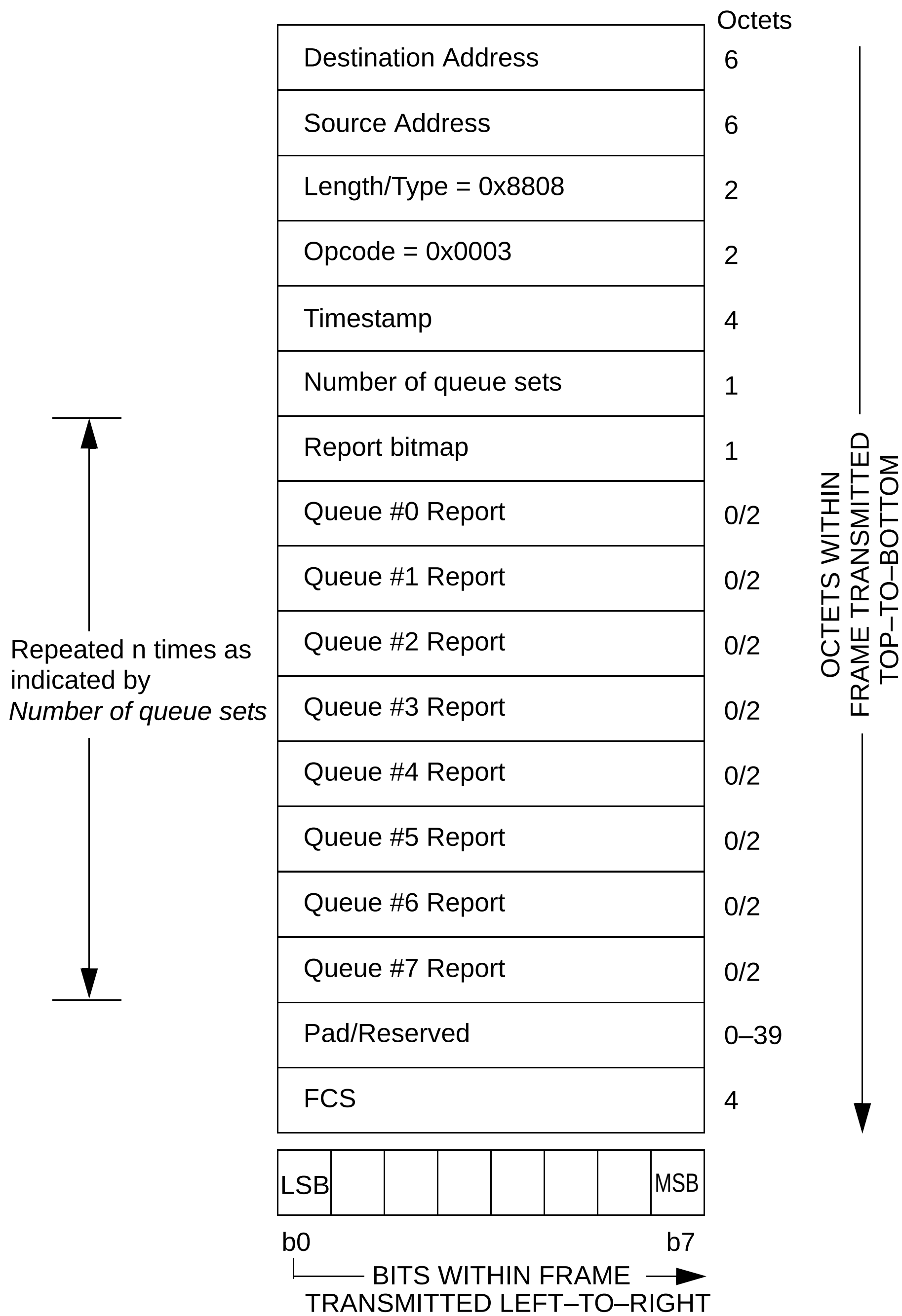


Figure 93–32—REPORT MPCPDU

93.3.6.3 REGISTER_REQ description

The REGISTER_REQ MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_REQ MPCPDU is 0x0004.
b) Flags. This is an 8 bit flag register that indicates special requirements for the registration.
c) Pending grants. This is an unsigned 8 bit value signifying the maximum number of future grants the ONU is configured to buffer. The OLT should not grant the ONU more than this maximum number of Pending grants vectors comprised of {start, length, force_report, discovery} into the future.
d) Discovery Information. This is an 16 bit flag register. Table 93–7 presents the internal structure of the Discovery Information flag field.
e) Laser On Time. This field is 1 byte long and carries the Laser On Time characteristic for the given ONU transmitter. The value is expressed in the units of time_quanta.
f) Laser Off Time. This field is 1 byte long and carries the Laser Off Time characteristic for the given ONU transmitter. The value is expressed in the units of time_quanta.
g) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation.

Table 93–6—REGISTER_REQ MPCPDU Flags fields

Value	Indication	Comment
0	reserved	Ignored on reception.
1	Register	Registration attempt for ONU.
2	reserved	Ignored on reception.
3	Deregister	This is a request to deregister the ONU. Subsequently, the MAC is deallocated and the LLID may be reused.
4–255	reserved	Ignored on reception.

Table 93–7—REGISTER_REQ MPCPDU Discovery Information Fields

Bit	Flag Field	Values
0	ONU is 1G upstream capable	0 – ONU transmitter is capable of 1 Gb/s 1 – ONU transmitter is not capable of 1 Gb/s
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2 – 3	reserved	Ignored on reception.
4	1G registration attempt	0 – 1 G registration is attempted 1 – 1 G registration is not attempted
5	10 G registration attempt	0 – 10 G registration is not attempted 1 – 10 G registration is attempted
6 – 15	reserved	Ignored on reception.

The REGISTER_REQ MPCPDU shall be generated by a MAC Control instance mapped to an undiscovered ONU, and as such shall be marked with a broadcast type of LLID (Subclause 93.3.2.3).

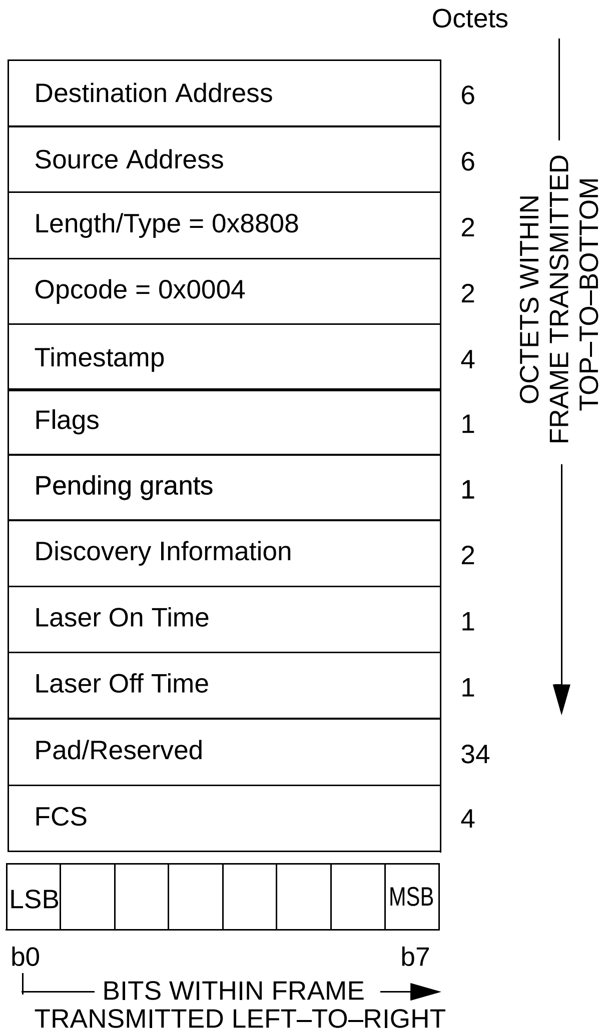


Figure 93–33—REGISTER_REQ MPCPDU

93.3.6.4 REGISTER description

The REGISTER MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) DA. The destination address used shall be an individual MAC address.
b) Opcode. The opcode for the REGISTER MPCPDU is 0x0005.
c) Assigned Port. This field holds a 16 bit unsigned value reflecting the LLID of the port assigned following registration.
d) Flags. this is an 8 bit flag register that indicates special requirements for the registration.

Table 93–8—REGISTER MPCPDU Flags field

Value	Indication	Comment
0	Reserved	Ignored on reception.
1	Reregister	The ONU is explicitly asked to re–register.

Table 93–8—REGISTER MPCPDU Flags field

Value	Indication	Comment
2	Deregister	This is a request to deallocate the port and free the LLID. Subsequently, the MAC is deallocated.
3	Ack	The requested registration is successful.
4	Nack	The requested registration attempt is denied by the higher–layer–entity.
5–255	Reserved	Ignored on reception.

e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. During the synchronization time the ONU transmits only IDLE code–pairs. The value is counted in 1 time_quantum increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA and PCS.

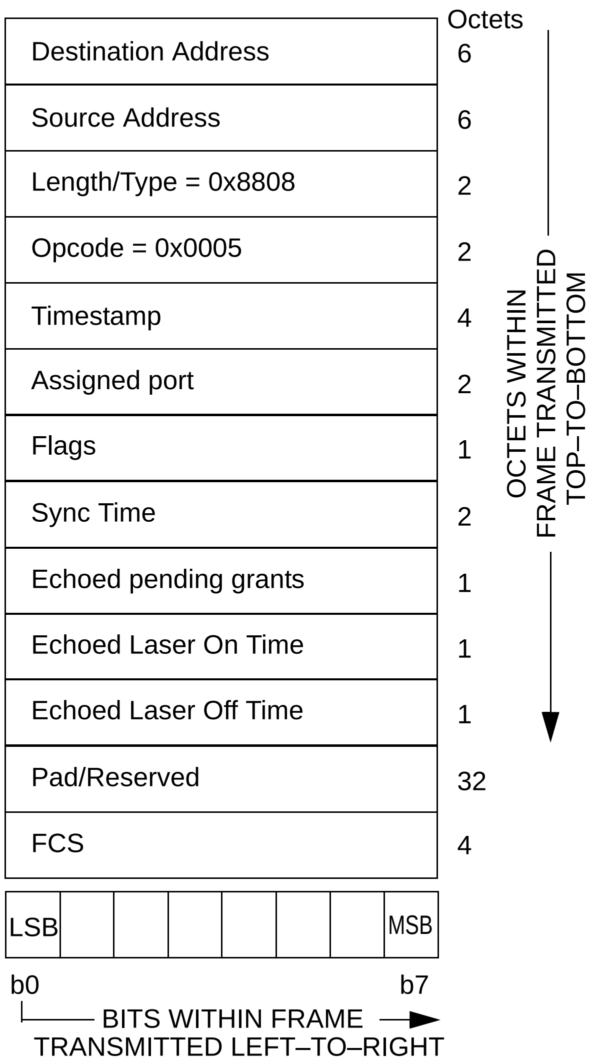


Figure 93–34—REGISTER MPCPDU

f) Echoed pending grants. This is an unsigned 8 bit value signifying the number of future grants the ONU may buffer before activating. The OLT should not grant the ONU more than this number of grants into the future.
g) Echoed Laser On Time. This is an unsigned 8 bit value signifying the Laser On Time for the given ONU transmitter. The value is expressed in the units of time_quanta. The value is delivered to the ONU for confirmation purposes only and its utilization is not prescribed in this specification.
h) Echoed Laser Off Time. This is an unsigned 8 bit value signifying the Laser Off Time for the given ONU transmitter. The value is expressed in the units of time_quanta. The value is delivered to the ONU for confirmation purposes only and its utilization is not prescribed in this specification.
i) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation.

The REGISTER MPCPDU shall be generated by a MAC Control instance mapped to all ONUs and such frame is marked by the broadcast LLID (Subclause 93.3.2.3).

93.3.6.5 REGISTER_ACK description

The REGISTER_ACK MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_ACK MPCPDU is 0x0006.
b) Flags. this is an 8 bit flag register that indicates special requirements for the registration.Echoed assigned port. This field holds a 16 bit unsigned value reflecting the LLID of the port assigned following registration.
c) Echoed Sync Time. This is an unsigned 16 bit value echoing the required synchronization time of the OLT receiver as previously advertised (Subclause 93.3.6.4).
d) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored at reception when constructing a complying MPCP protocol implementation.

Table 93–9—REGISTER_ACK MPCPDU Flags fields

Value	Indication	Comment
0	Nack	The requested registration attempt is denied by the higher–layer–entity.
1	Ack	The registration process is successfully acknowledged.
2–255	Reserved	Ignored on reception.

The REGISTER_ACK MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

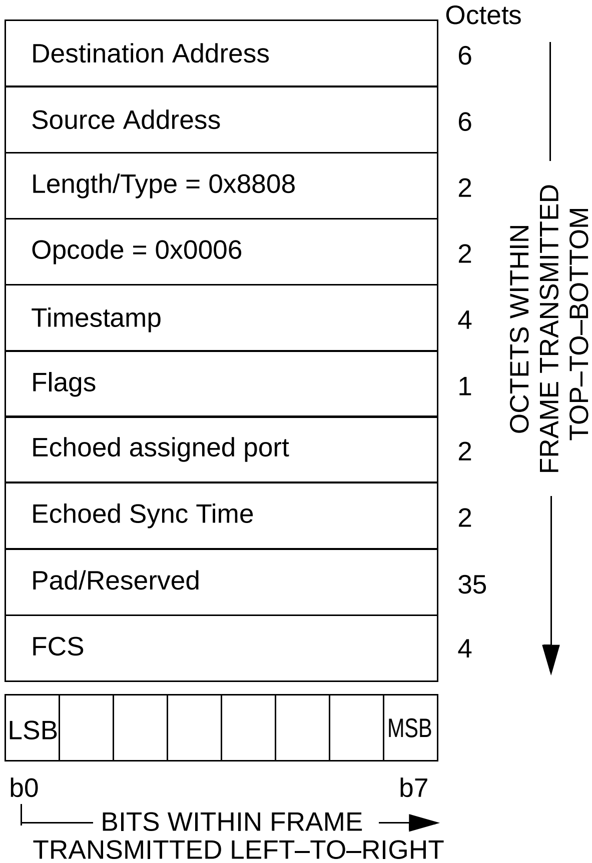


Figure 93–35—REGISTER_ACK MPCPDU

93.4 Discovery Process in dual–rate systems (informative)

The enhancements introduced to the Clause 93 discovery process for EPONs facilitate the coexistence of 10G–EPON with legacy EPON.

93.4.1 OLT speed specific discovery

The discovery GATE MPCPDU is defined in @@Clause 64@@ for 1 Gb/s operation and in Clause 93 for 10 Gb/s operation. An additional field (Discovery Information field) was added to the 10 Gb/s discovery GATE MPCPDU. This field allows the OLT to relay speed specific information regarding the discovery window to the different ONUs that may co–exist on the same PON. The OLT has the ability to transmit common discovery GATE MPCPDUs on both the 1 Gb/s transmit path and 10 Gb/s transmit path, or it can send completely separate and independent GATE messages on these different paths. For each discovery window, the OLT is capable of opening windows for individual speeds or multiple speeds.

These different combinations allow the OLT MAC Control Client to open a number of discovery windows for all of the different ONU types. Table 93–10 shows the different types of windows that are possible, along with the necessary LLID and discovery information that also needs to be present in the discovery GATE MPCPDUs. For some combinations, it is necessary for the OLT MAC Control Client to open overlapping discovery windows by sending discovery GATE MPCPDUs on both the 1 Gb/s and 10 Gb/s downstream broadcast channels.

Table 93–10—Discovery GATE MPCPDUs for all ONU types.

ONU types on the PON [DS/US transmission speed]	LLID of discovery GATE(s)	Discovery Information			
		Upstream Capable		Discovery Window	
		1G	10G	1G	10G
1/1 Gb/s	0x7FFF	1	0	1	0
10/1 Gb/s	0x7FFE	1	0	1	0
1/1 Gb/s and 10/1 Gb/s	0x7FFF, 0x7FFE[a]	1	0	1	0
10/10 Gb/s	0x7FFE	0	1	0	1
10/1 Gb/s and 10/10 Gb/s	0x7FFE	1	1	1	1
1/1 Gb/s, 10/1 Gb/s, and 10/10 Gb/s	0x7FFF, 0x7FFE[a]	1	1	1	1

[a]Two discovery GATE MPCPDUs are transmitted in the downstream broadcast channel: one with the LLID of 0x7FFF transmitted on the 1 Gb/s downstream broadcast channel and another one the LLID of 0x7FFE transmitted on the 10 Gb/s downstream broadcast channel.

Figure 93–36 shows the three primary combinations of discovery windows and the different types of REGISTER_REQ MPCPDUs that may be received during the window. Figure 93–36(a) shows reception of messages from 1 Gb/s and 10/1 Gb/s ONUs. Figure 93–36(b) shows reception of messages from 10 Gb/s ONUs. Figure 93–36(c) shows reception of messages from all types of ONUs.

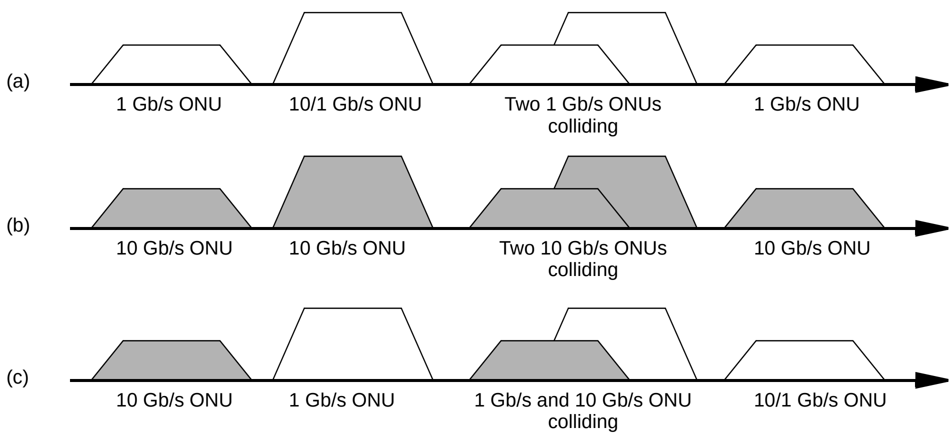


Figure 93–36—Combinations of REGISTER_REQ MPCPDUs during discovery window for 10G–EPON and EPON coexisting on the same PON.

93.4.2 ONU speed specific registration

A legacy 1 Gb/s ONU will only receive discovery GATE messages transmitted by the OLT on the 1 Gb/s broadcast channel. Operation and registration of these ONUs remains the same as previously, since no changes have been made to the existing 1 Gb/s discovery process.

A 10/1 Gb/s ONU is only capable of receiving discovery GATE MPCPDU transmitted by the OLT on the 10 Gb/s broadcast channel. These messages need to be parsed, and if a 1 Gb/s discovery window is opened, the ONU may attempt to register on the EPON.

A dual speed ONU capable of asymetric 10/1 Gb/s operation or symmetric 10/10 Gb/s operation is also only capable of receiving discovery GATE MPCPDU transmitted by the OLT on the 10 Gb/s broadcast channel. These messages need to be parsed, and the ONU makes the registration decision based on the available information. The ONU should attempt to register based during the discovery window announced as supporting the highest speed common to both the OLT and ONU. Table 93–11 shows the action the ONU should take based on the ONU transmit capabilities and the received discovery information.

Table 93–11—ONU action during discovery window

OLT Discovery Information				ONU Tx capability		ONU Action
Upstream Capable		Discovery Window				
1G	10G	1G	10G	1G	10G	
1	0	1	0	1	X	Attempt 1G registration
0	1	0	1	X	1	Attempt 10G registration
1	1	0	1	0	1	Attempt 10G registration
1	1	0	1	1	0	Wait for 1G discovery window
1	1	0	1	1	1	Attempt 10G registration
1	1	1	0	0	1	Wait for 10G discovery window
1	1	1	0	1	0	Attempt 1G registration
1	1	1	0	1	1	Wait for 10G discovery window
1	1	1	1	0	1	Attempt 10G registration
1	1	1	1	1	0	Attempt 1G registration
1	1	1	1	1	1	Attempt 10G registration

93.5 Protocol implementation conformance statement (PICS) proforma for Clause 93, Multipoint MAC Control[a]

93.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 93 Multipoint MAC Control, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

93.5.2 Identification

93.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

93.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3–2005, Clause 93, Multipoint MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3–2005.)	
Date of Statement	

[a] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

93.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	93.1	Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality	93.1	Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

93.5.4 PICS proforma tables for Multipoint MAC Control

93.5.4.1 Compatibility Considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Delay through MAC and PHY	93.3.2.4	Maximum delay variation of 16 ns (1 time_quantum)	M	Yes [ ]
CC2	OLT grant time delays	93.3.2.4	Not grant nearer than 1024 time_quanta into the future	OLT:M	Yes [ ]
CC3	ONU processing delays	93.3.2.4	Must process all messages in less than 1024 time_quanta	ONU:M	Yes [ ]
CC4	OLT grant issuance	93.3.2.4	Not grant more than one message every 1024 time_quanta	OLT:M	Yes [ ]

93.5.4.2 Multipoint MAC Control

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	OLT localTime	93.2.2.2	Track transmit clock	OLT:M	Yes [ ]
OM2	ONU localTime	93.2.2.2	Track receive clock	ONU:M	Yes [ ]
OM3	Random wait for transmitting REGISTER_REQ messages	93.3.3	Shorter than length of discovery window	ONU:M	Yes [ ]
OM4	Periodic report generation	93.3.4	Reports are generated periodically	ONU:M	Yes [ ]
OM5	Periodic granting	93.3.4	Grants are issued periodically	OLT:M	Yes [ ]
OM6	Issuing of grants	93.3.5	Not issue more than maximum supported grants	OLT:M	Yes [ ]

93.5.4.3 State Diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Multipoint Transmission Control	93.2.2.7	Meets the requirements of Figure 93–9	M	Yes [ ]
SM2	OLT Control Parser	93.2.2.7	Meets the requirements of Figure 93–10	M	Yes [ ]
SM3	ONU Control Parser	93.2.2.7	Meets the requirements of Figure 93–13	M	Yes [ ]
SM4	OLT Control Multiplexer	93.2.2.7	Meets the requirements of Figure 93–14	OLT:M	Yes [ ]
SM5	ONU Control Multiplexer	93.2.2.7	Meets the requirements of Figure 93–15	OLT:M	Yes [ ]
SM6	Discovery Processing OLT Window Setup	93.3.3.6	Meets the requirements of Figure 93–18	OLT:M	Yes [ ]
SM7	Discovery Processing OLT Process Requests	93.3.3.6	Meets the requirements of Figure 93–19	OLT:M	Yes [ ]
SM8	Discovery Processing OLT Register	93.3.3.6	Meets the requirements of Figure 93–20	ONU:M	Yes [ ]
SM9	Discovery Processing OLT Final Registration	93.3.3.6	Meets the requirements of Figure 93–21	OLT:M	Yes [ ]
SM10	Discovery Processing ONU Registration	93.3.3.6	Meets the requirements of Figure 93–22	ONU:M	Yes [ ]
SM11	Report Processing at OLT	93.3.4.6	Meets the requirements of Figure 93–24	OLT:M	Yes [ ]
SM12	Report Processing at ONU	93.3.4.6	Meets the requirements of Figure 93–25	ONU:M	Yes [ ]
SM13	Gate Processing at OLT	93.3.5.6	Meets the requirements of Figure 93–27	OLT:M	Yes [ ]
SM14	Gate Processing at ONU	93.3.5.6	Meets the requirements of Figure 93–28	ONU:M	Yes [ ]
SM15	Gate Processing ONU Activation	93.3.5.6	Meets the requirements of Figure 93–29	ONU:M	Yes [ ]

93.5.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	MPCPDU structure	93.3.6	As in Figure 93–30	M	Yes [ ]
MP2	LLID for MPCPDU	93.3.6	RS generates LLID for MPCPDU	M	Yes [ ]
MP3	Grants during discovery	93.3.6.1	Single grant in GATE message during discovery	OLT:M	Yes [ ]
MP4	Grant start time	93.3.6.1	Grants within one GATE MPCPDU are sorted by their Start time values	OLT:M	Yes [ ]
MP5	TX during synchronization	93.3.6.1	Transmit IDLE code groups	ONU:M	Yes [ ]
MP6	GATE generation	93.3.6.1	GATE generated for active ONU except during discovery	OLT:M	Yes [ ]
MP7	GATE LLID	93.3.6.1	Unicast LLID except for discovery	OLT:M	Yes [ ]
MP8	REPORT issuing	93.3.6.2	Issues REPORT periodically	ONU:M	Yes [ ]
MP9	REPORT generation	93.3.6.2	Generated by active ONU	ONU:M	Yes [ ]
MP10	REPORT LLID	93.3.6.2	REPORT has unicast LLID	ONU:M	Yes [ ]
MP11	REGISTER_REQ generation	93.3.6.3	Generated by undiscovered ONU	ONU:M	Yes [ ]
MP12	REGISTER_REQ LLID	93.3.6.3	Use broadcast LLID	ONU:M	Yes [ ]
MP13	REGISTER DA address	93.3.6.4	Use individual MAC address	OLT:M	Yes [ ]
MP14	REGISTER generation	93.3.6.4	Generated for all ONUs	OLT:M	Yes [ ]
MP15	REGISTER_ACK generation	93.3.6.5	Generated by active ONU	ONU:M	Yes [ ]
MP16	REGISTER_ACK LLID	93.3.6.5	Use unicast LLID	ONU:M	Yes [ ]