OPTICAL INTERNETWORKING FORUM

Implementation Agreement for Integrated Polarization Multiplexed Quadrature Modulated Transmitters

IA # OIF-PMQ-TX-01.2

May 15, 2015

Implementation Agreement created and approved
by the Optical Internetworking Forum
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TITLE: **Implementation Agreement for Integrated Polarization Multiplexed Quadrature Modulated Transmitters.**

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ABSTRACT: This Implementation Agreement specifies key aspects of integrated polarization multiplexed quadrature modulated optical transmitters operating at rates up to 32 GBd for applications such as 100G PM-QPSK DWDM transmission. This is not a multi-source agreement (MSA) but it is expected that it will serve as a foundation for future MSAs.

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4 Document Revision History

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DATE: **May 15th, 2015**

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OIF-PMQ-TX-01.0	March 12, 2010	Created from oif2009.186.05	M. Bouda
OIF-PMQ-TX-01.1	August 27, 2013	Based on oif2013.046.05 Changes to Sections 7, 11 and 16 - Updates to Type 3 Envelope - Addition of Type 4 Envelope - Addition of 4-GPPO interface Changes to Appendix B (Informative) - Potential locations of mounting holes Addition of Appendix C (Informative) - SMT landing pad dimension	M. Bouda
OIF-PMQ-TX-01.2	May 15, 2015	Based on oif2014.099.05 - Reduction of SMT options to FPC only - FPC option included in document body - Added FPC mechanical specifications	M. Bouda

5 Introduction

This document details an Implementation Agreement (IA) for an optical integrated Polarization Multiplexed (PM) quadrature modulated transmitter for applications with nominal symbol rates of up 32 GBaud. While specifically addressing 100G PM-QPSK applications with FEC, this Implementation Agreement strives to remain modulation format and data rate agnostic whenever practical to maximize applicability to other future applications. This IA is expected to serve as a foundation for future MSAs.

6 Functionality

This Implementation Agreement specifies in detail a single opto-electronic module with the functionality contained in the yellow area enclosed by the bold line in Figure 1. This module will be referred to as Polarization Multiplexed-Quadrature Modulator or PM-Q Modulator.

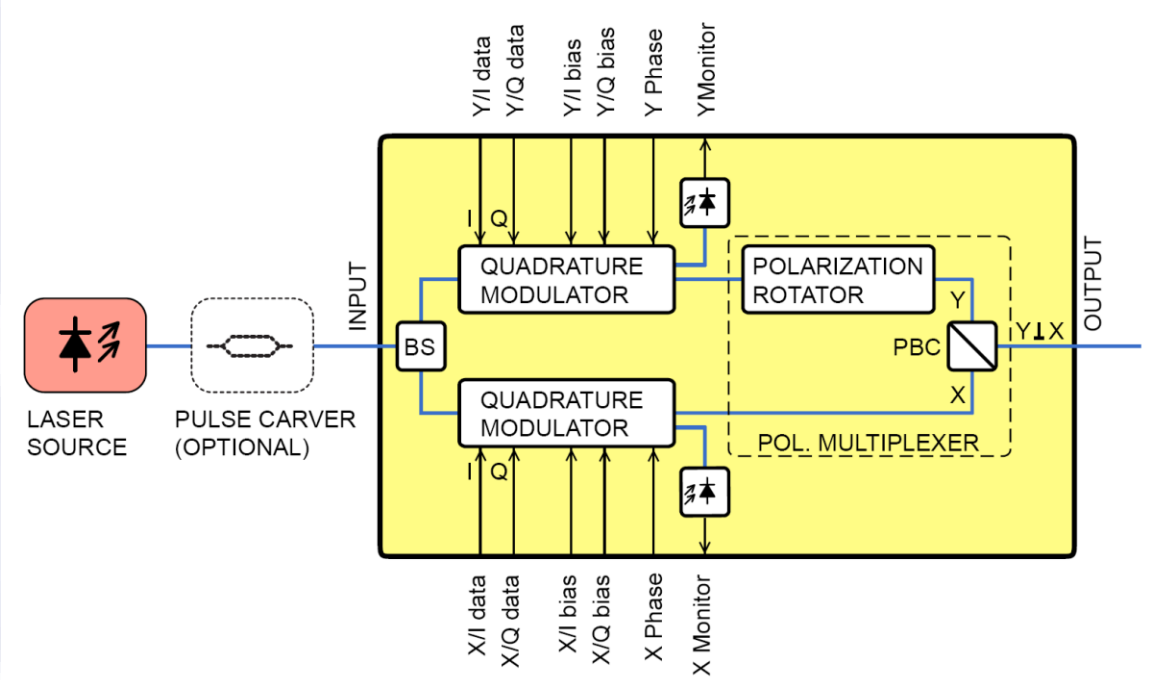

Figure 1 Functional diagram of a polarization multiplexed quadrature modulated integrated transmitter with a detailed functional diagram of the data modulator.

The optical power from an input fiber is divided into two parts and each part is independently modulated by a quadrature modulator. The resulting two modulated signals are combined with their polarizations orthogonal to each other, and output through an optical output fiber. The power in each of the two polarizations is independently monitored with photodiodes.

The quadrature modulators typically comprise two nested Mach-Zehnder modulators with bias control, a 90º phase shifter in the outer modulators with phase control, and an output power monitoring output. Any implementation or technology choices may be used to realize the same basic functionality.

As indicated in Figure 1, the PM-Q Modulator includes the following basic functional components:

- One optical input
- One optical power splitter
- Two independent quadrature modulators
- Two independent monitoring photodiodes
- One polarization multiplexer
- One optical output

The PM-Q Modulator module specified in this Implementation Agreement does not include drivers or any control electronics.

The following independent interfaces are specified for the PM-Q modulator:

- One optical input fiber
- One optical output fiber
- Four high-speed data interfaces
- Four modulator bias control interfaces
- Two phase control interfaces
- Two power monitoring interfaces

The two polarized components at the output are referred to as “X” and “Y”, and the arms in which information is modulated onto the polarization component are correspondingly referred to as X and Y arms. Each quadrature modulator is driven by an “I” and a “Q” data signal. The four high-speed data interfaces are referred to as X/I, X/Q, Y/I and Y/Q data interfaces. Nominal phase shifts in the quadrature modulators between I and Q shall be the same in X and Y arms.

Each of the four data modulators needs to be biased with a suitable DC voltage. This IA specifies biasing pins supporting both single-ended as well as push-pull biasing. The naming of the bias pins is consistent with the naming of the high-speed data interfaces. The I and Q phase offset is controlled via phase control pins also supporting both single-ended as well as push-pull control. The phase offset between I and Q in X and Y arms is controlled by phase control interfaces X Phase and Y Phase respectively.

7 Electrical Interfaces

7.1 Mechanical Specification of Low-Speed Interface and Interface Locations

The mechanical specification of an 18-pin low-speed interface is shown in Figure 2. The low-speed pins are grouped in groups of 6 pins. The type of the low-speed pins, their length and their distance from the bottom plane of the modulator package are not specified.

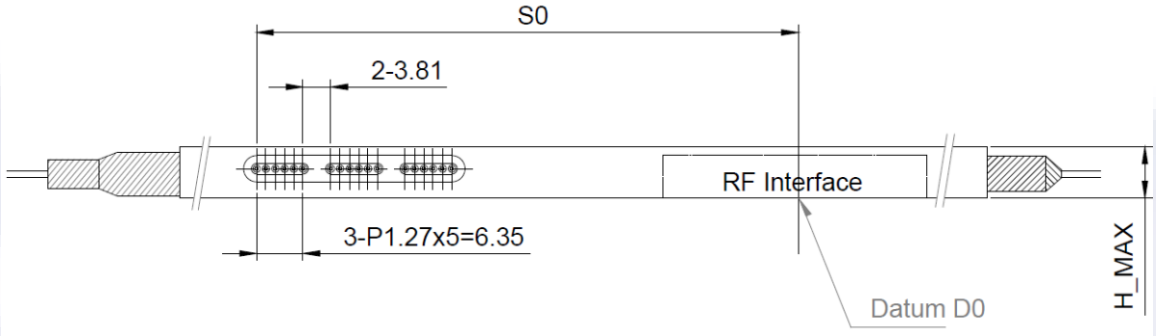

Figure 2 Specification of low-speed interface, and location of low- and high-speed interfaces relative to a Datum.

Figure 2 further defines the positions of both low-speed and high-speed interfaces relative to a Datum D0. Datum D0 is centered between the center lines of the high-speed connectors. The spacing between DC and RF interfaces is defined by parameter S0.

The applicable high-speed interface configuration and the values of H_MAX and S0 are specified in Table 7.

7.2 Mechanical Specification of High-Speed Interface Options

The high-speed data interfaces of the PM-Q Modulator module shall be coaxial GPPO-compatible or Flexible Printed Circuit (FPC), depending on modulator envelope type as specified in Table 7.

7.2.1 GPPO-Compatible High-Speed Interface Options

Figure 3 and Figure 4 define the 2+2 GPPO and 4 GPPO high-speed interface configurations.

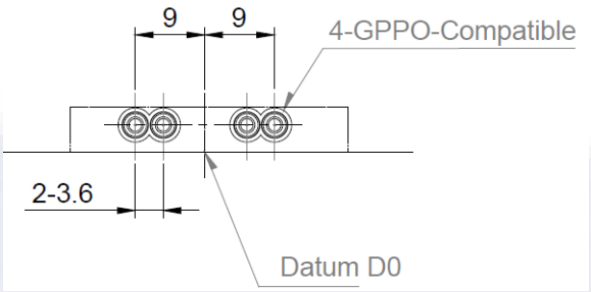

Figure 3 Mechanical specification of a "2+2 GPPO" high-speed interface.

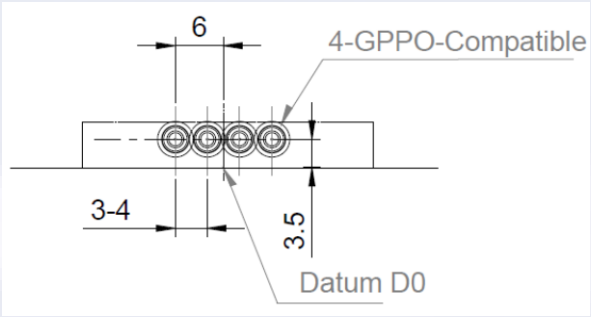

Figure 4 Mechanical specification of a "4 GPPO" high-speed interface.

7.2.2 FPC High-Speed Interface Option

Figure 5 and the relevant parameter values in Table 1 define the FPC High-Speed Interface configuration.

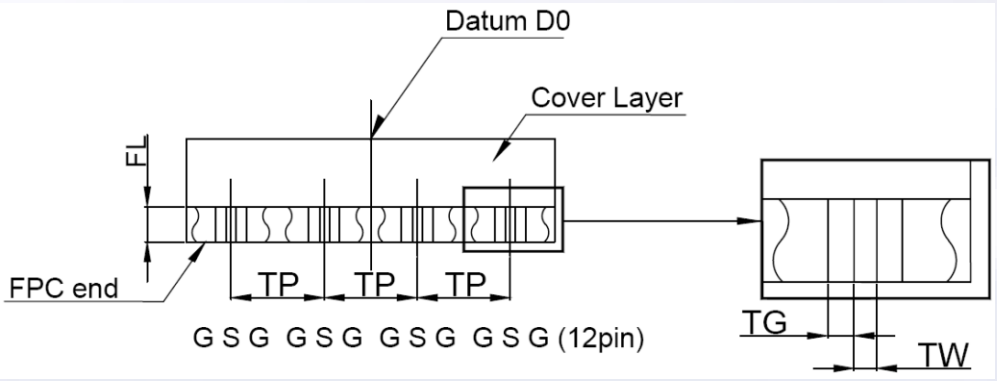

Figure 5 Mechanical specification of FPC high-speed interface.

In case the module is used inside a transponder package and is placed close to a transponder package wall as shown in Figure 6, the extent of the FPC landing pad is defined relative to Datum D1. Datum D1 is defined as the point of intersection between the center line of the High Speed Interface, the surface of the host PCB, and the inner wall surface of the transponder package.

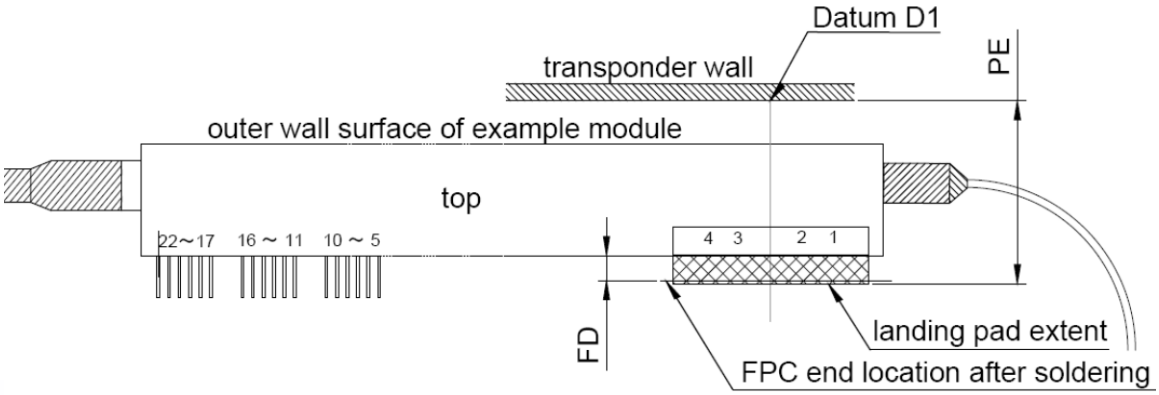

Figure 6 Landing pad extent and module wall to FPC-end distance.

Table 1 Mechanical specification of FPC high-speed interface.

Parameter	Symbol	Unit	Min.	Typ.	Max.
Signal trace pitch	TP	mm		4	
Signal trace width	TW	µm	300	350	400
Signal-Ground gap width	TG	µm	450	500	550
Landing pad extent on host PCB	PE	mm			14.5
Module wall to FPC-end distance options	FD	mm	3.5 1.5	3.8 1.8	4.1 2.1
FPC solder length options	FL	mm		1.5 0.9	

7.3 Electrical Interface Pin Assignments

The pin numbering starts with the first high-speed data interface connector furthest from the low-speed pins and the pin number increases towards the opposite side.

A first electrical interface grouping, ordering and function are listed in Table 2. An alternative allowed electrical interface ordering is provided in Table 3. The alternative ordering in Table 3 interleaves corresponding X and Y polarization quadrature bias pins to minimize the electrical crosstalk between the I and Q modulator biases. The separation between the monitor photodiode cathodes is also maximized with this alternative ordering for crosstalk reasons.

Table 2 Electrical interface pin-out and function with multiple options for biasing and phase control.

Pin	Symbol		Description
1	Data_X/I		X-polarization in-phase data input
2	Data_X/Q		X-polarization quadrature data input
3	Data_Y/I		Y-polarization in-phase data input
4	Data_Y/Q		Y-polarization quadrature data input
5	Bias_Y/Q(p)	Bias_Y/Q	Y/Q modulator (positive) bias
6	Bias_Y/Q(n)	GND or NC	Y/Q modulator neg. bias (push-pull) or GND or NC (single-ended)
7	Bias_Y/I(p)	Bias_Y/I	Y/I modulator (positive) bias
8	Bias_Y/I(n)	GND or NC	Y/I modulator neg. bias (push-pull) or GND or NC (single-ended)
9	Bias_X/Q(p)	Bias_X/Q	X/Q modulator (positive) bias
10	Bias_X/Q(n)	GND or NC	X/Q modulator neg. bias (push-pull) or GND or NC (single-ended)
11	Bias_X/I(p)	Bias_X/I	X/I modulator (positive) bias
12	Bias_X/I(n)	GND or NC	X/I modulator neg. bias (push-pull) or GND or NC (single-ended)
13	Phase_Y(p)	Phase_Y	Y pol. phase (positive)
14	Phase_Y(n)	GND or NC	Y pol. phase negative (push-pull) or GND or NC (single-ended)
15	Phase_X(p)	Phase_X	X pol. phase (positive)
16	Phase_X(n)	GND or NC	X pol. phase negative (push-pull) or GND or NC (single-ended)
17	NC or Bias_Subst [1)]		Not Connected or substrate bias [1)]
18	Y_A		Y-polarization photodiode Anode
19	Y_C		Y-polarization photodiode Cathode
20	GND		Ground
21	X_C		X-polarization photodiode Cathode
22	X_A		X-polarization photodiode Anode

1) Pin 17 may be used for substrate bias if needed. Otherwise the pin shall be Not Connected.

Table 3 Alternative electrical interface pin-out and function with multiple options for biasing and phase control.

Pin	Symbol		Description
1	Data_X/I		X-polarization in-phase data input
2	Data_X/Q		X-polarization quadrature data input
3	Data_Y/I		Y-polarization in-phase data input
4	Data_Y/Q		Y-polarization quadrature data input
5	Bias_Y/Q(p)	Bias_Y/Q	Y/Q modulator (positive) bias
6	Bias_Y/Q(n)	GND or NC	Y/Q modulator neg. bias (push-pull) or GND or NC (single-ended)
7	Bias_X/Q(p)	Bias_X/Q	X/Q modulator (positive) bias
8	Bias_X/Q(n)	GND or NC	X/Q modulator neg. bias (push-pull) or GND or NC (single-ended)
9	Bias_Y/I(p)	Bias_Y/I	Y/I modulator (positive) bias
10	Bias_Y/I(n)	GND or NC	Y/I modulator neg. bias (push-pull) or GND or NC (single-ended)
11	Bias_X/I(p)	Bias_X/I	X/I modulator (positive) bias
12	Bias_X/I(n)	GND or NC	X/I modulator neg. bias (push-pull) or GND or NC (single-ended)
13	Phase_Y(p)	Phase_Y	Y pol. phase (positive)
14	Phase_Y(n)	GND or NC	Y pol. phase negative (push-pull) or GND or NC (single-ended)
15	Phase_X(p)	Phase_X	X pol. phase (positive)
16	Phase_X(n)	GND or NC	X pol. phase negative (push-pull) or GND or NC (single-ended)
17	NC or Bias_Subst [1)]		Not Connected or substrate bias [1)]
18	Y_C		Y-polarization photodiode Cathode
19	Y_A		Y-polarization photodiode Anode
20	GND		Ground
21	X_A		X-polarization photodiode Anode
22	X_C		X-polarization photodiode Cathode

1) Pin 17 may be used for substrate bias if needed. Otherwise the pin shall be Not Connected.

7.4 Electrical Properties of Low-Speed Electrical Interface

The electrical properties related to the power monitor diodes are specified in Table 4. The opto-electronic properties of the optical modulator including the high-speed data interfaces are specified in Section 8.

Table 4 Low-speed interface electrical properties.

Parameter	Unit	Min.	Typ.	Max.	Remarks
Monitor PD Responsivity	mA/W	1)		1)	
Monitoring PD O/E Bandwidth	GHz	1			
1) Application Specific - because of the range of applications for this component, a specific value cannot be provided.					

8 Opto-Electronic Properties

Electrical specification of the high-speed interface and opto-electronic properties are given in Table 5 at the end of life over the operating temperature and frequency ranges.

Table 5 Electrical and opto-electronic properties.

Parameter	Unit	Min.	Typ.	Max.	Remarks
S21 E/O Bandwidth (3dB)	GHz	23			3% smoothed, reference frequency at 1.5 GHz or 2 GHz
S11 Electrical Return Loss f ≤ 25 GHz 25 < f ≤ 32 GHz	dB	 10 8			
Vpi_PRBS	V			3.5	Specified at PRBS31 at 32 GBd
Vpi_LF (*1)	V			3.4	Measured at 1.5 GHz or 2 GHz
RF Impedance	Ohm		50		
I/Q skew (*2)	ps			4	For each polarization component
Total skew (*3)	ps			10	
I/Q skew variation	ps			2	
Total skew variation	ps			5	
1) A module vendor shall provide data showing correlation between Vpi_LF and Vpi_PRBS, and specify a Vpi_LF that guarantees a Vpi_PRBS satisfying the requirements in this table. 2) I/Q Skew is the skew between channel pairs X/I and X/Q, and Y/I and Y/Q. 3) Total skew is the maximum skew between any of the four physical channels X/I, X/Q, Y/I and Y/Q.					

Skew is defined as the maximum signal propagation time difference between physical signal channels, between electrical input and optical output interfaces. Skew includes any skew variation due to aging, temperature and any other effects.

9 Optical Properties

Optical properties of the optical modulator are listed in Table 6 at the end of life over the operating temperature and frequency ranges. Tighter parent and child MZI extinction ratio specifications may be required for certain applications such as PM-16QAM modulation (extended performance).

Table 6 Optical properties.

Parameter	Unit	Min.	Typ.	Max.	Remarks
Operating Frequency C-Band L-Band	THz	 191.35 186.0		 196.2 191.5	At least one range shall be supported in one device
Input power	dBm			18	Peak power
Insertion loss	dB	1)		14	All modulators at peak transmission, for each polarization
Insertion loss difference between X and Y				1)	
Optical return loss	dB	30			Input and output
Parent MZI ER Basic Performance Extended Performance	dB	 20 22			
Child MZI ER Basic Performance Extended Performance	dB	 20 25			
Polarization ER	dB	20			

1) Application Specific - because of the range of applications for this component, a specific value cannot be provided.

In case of polarization maintaining fiber, the optical connector key shall be aligned to the slow axis of the polarization maintaining fiber. The input fiber shall be polarization maintaining. Optical and opto-electronic specifications assume that a polarized input signal is launched into the slow axis of the input fiber.

The output fiber shall be either SMF or PMF.

10 Environmental Conditions

The typically expected operating temperature range is -5ºC to +75ºC. For the purpose of uniform calculation of the Failures In Time (FIT) rate, a fielded temperature of 55ºC shall be used.

11 Mechanical Properties

The dimensions of mechanical envelopes depend on the application. Envelope parameters are defined in Figure 7 and Figure 8. A reference point or datum is used to reference the extent of the envelopes, as well as the location of all electrical interfaces.

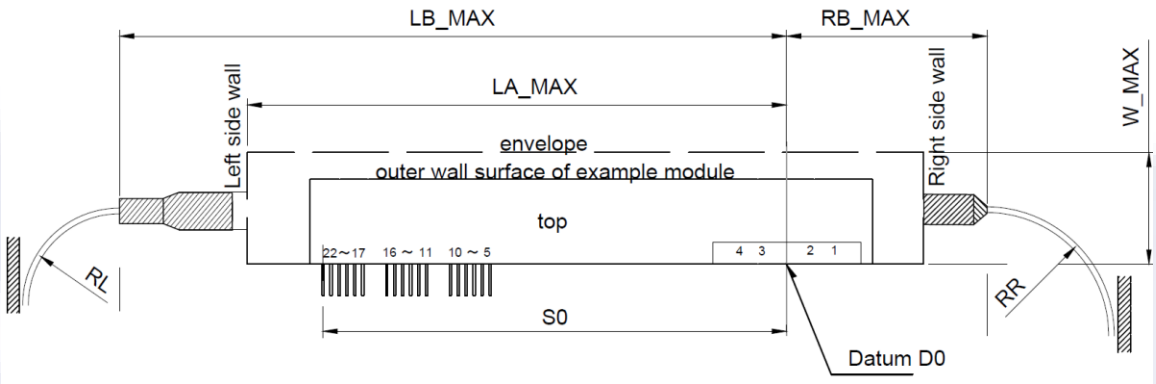

Figure 7 Location of Datum and dimensions related to Envelope Types 1, 2, and 3 (top view).

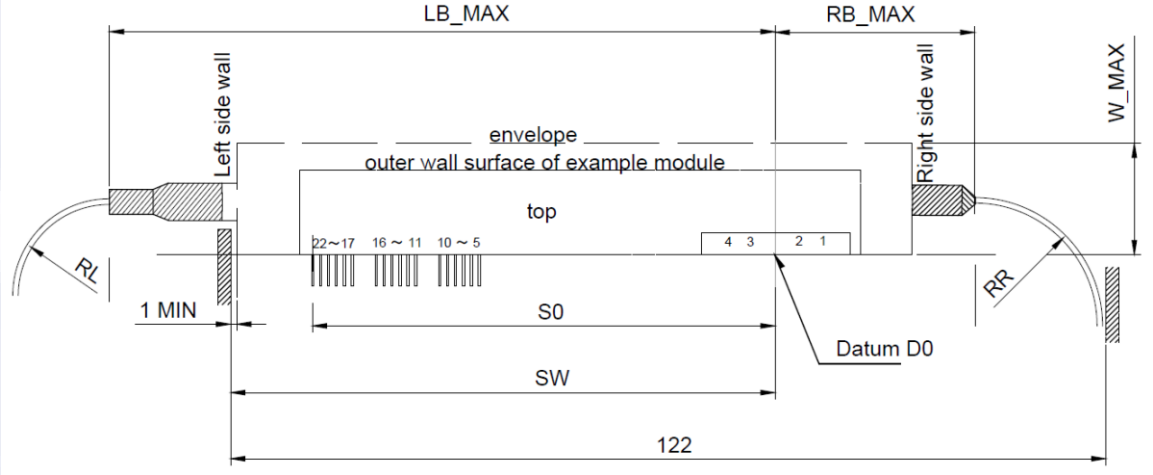

Figure 8 Location of Datum and dimensions related to Envelope Type 4 (top view).

Bend radii and boot lengths are not explicitly specified to avoid restricting the choice of implementation or technology.

Table 7 specifies four Envelope Types. Features and dimensions of Envelope Types 1 and 2 are derived from mechanical constraints of a 5”x7” transponder module application. Features and dimensions of Envelope Types 3 and 4 are derived from mechanical constraints of a 4”x5” transponder module application.

Table 7 Envelope Type features and dimensional parameters in mm.

Parameter	Type 1	Type 2	Type 3	Type 4
High-speed interface	2+2 GPPO		4 GPPO or FPC	
Input fiber side wall	right		right	
Output fiber side wall	left	right or left	right or left	right or left
Mounting hole side	bottom		bottom	
S0	74.06		48.83	61.2
SW	-	-	-	67.2
RB_MAX	36.0	51.1	36.0	39.8
LA_MAX		88.5	57.0	-
LB_MAX	-	-	-	85.2
for RR=20mm	98.8	-	89.3	-
for RR=15mm	103.8	-	94.3	-
W_MAX	13.5	20.0	20.0	13.5
H_MAX	7		7	

Mounting holes shall be of type M2.

Appendix A: Glossary

AC	Alternating Current
BS	Beam Splitter
BW	Band Width
DC	Direct Current
E/O	Electro-Optical
ER	Extinction Ratio
FEC	Forward Error Correction
FIT	Failures In Time
ffs	for further study
GND	Ground
IA	Implementation Agreement
MSA	Multi-Source Agreement
MZI	Mach-Zehnder Interferometer
NC	Not Connected
PBC	Polarization Beam Combiner
PD	Photo Diode
PMF	Polarization Maintaining Fiber
PM-Q	Polarization Multiplexed Quadrature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SMF	Single Mode Fiber

Appendix B: Examples of Additional Mechanical Details

This Appendix is informational and intended to avoid incompatible placement of alternate mounting holes and to provide other informative information that may be useful.

Mounting hole placement options are suggested in the area between the low-speed and high-speed electrical interfaces, along the side wall with the electrical interfaces. Other holes will exist. At least one additional mounting hole shall be located at the side opposite the electrical interfaces.

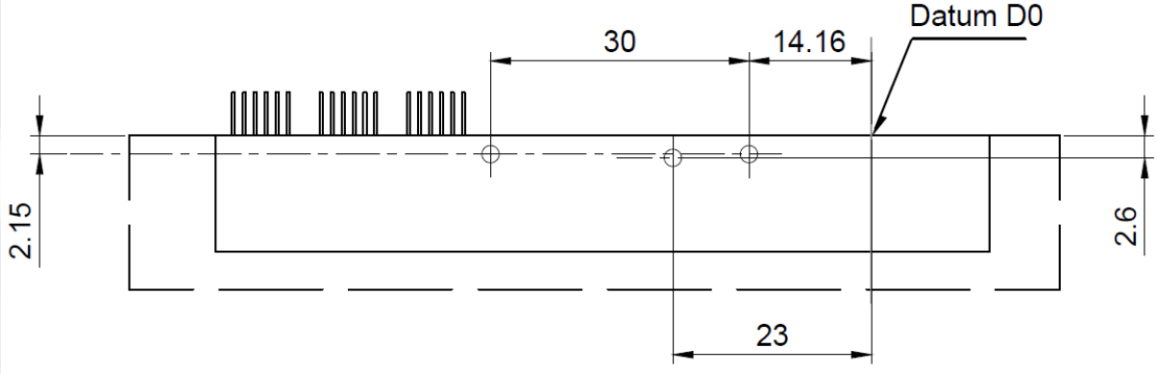

Figure 9 A subset of locations of potentially existing mounting holes for Types 1 and 2 (bottom view).

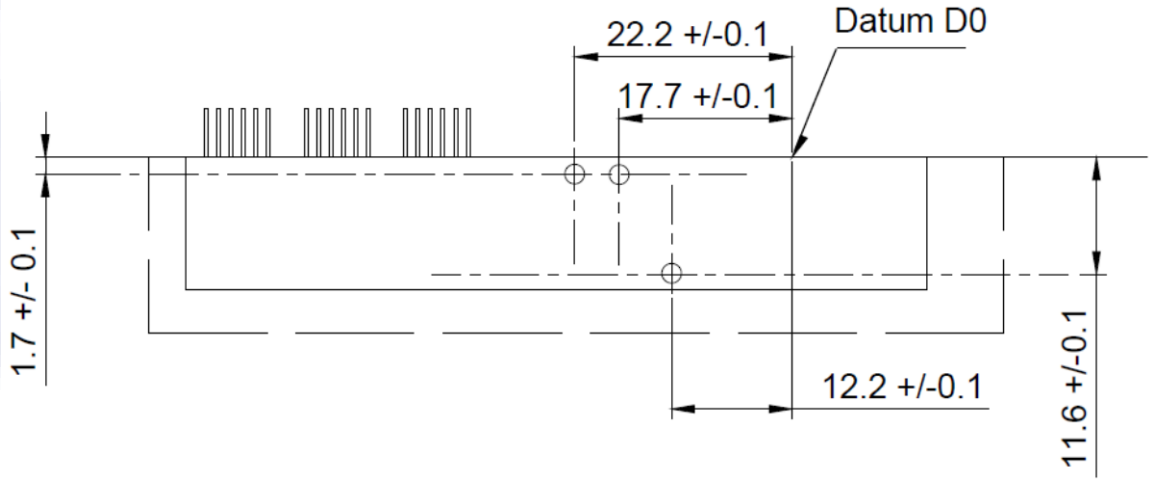

Figure 10 Potentially existing mounting holes for Types 3 and 4 (bottom view).

Boot lengths may vary from 21.2mm to 10.3mm depending on implementation.

Appendix C: Example of reference PCB interface design

This Appendix pertains to applications involving a modulator with FPC-type high-speed interface. The Printed Circuit Board (PCB) design example in Figure 11 is informational.

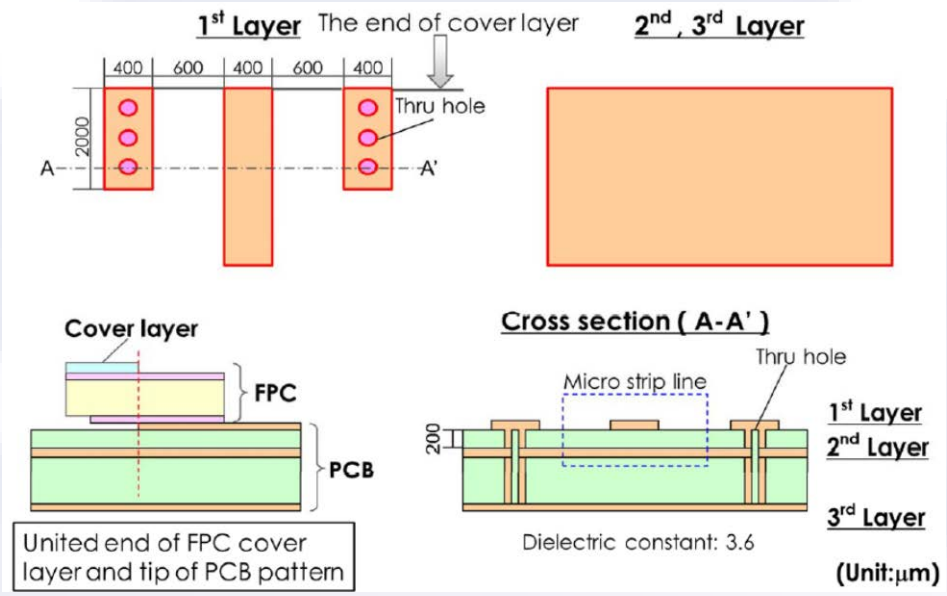

Figure 11 PCB interface design example.

Appendix D: Companies belonging to OIF when document was approved

Acacia Communications	Fujikura	NeoPhotonics
ADVA Optical Networking	Fujitsu	NTT Corporation
Alcatel-Lucent	Furukawa Electric Japan	O-Net Communications (HK) Ltd
Altera	Google	Oclaro
AMCC	Hewlett Packard	Orange
Amphenol Corp.	Hitachi	PETRA
Analog Devices	Huawei Technologies	Picometrix
Anritsu	IBM Corporation	PMC Sierra
Applied Communication Sciences	Infinera	QLogic Corporation
Avago Technologies Inc.	Inphi	Qorvo
Broadcom	Intel	Ranovus
Brocade	Ixia	Rockley Photonics
BRPhotonics	JDSU	Samtec Inc.
BTI Systems	Juniper Networks	Semtech
China Telecom	Kaiam	Socionext Inc.
Ciena Corporation	Kandou	Spirent Communications
Cisco Systems	KDDI R&D Laboratories	Sumitomo Electric Industries
ClariPhy Communications	Keysight Technologies, Inc.	Sumitomo Osaka Cement
Coriant R&G GmbH	LeCroy	TE Connectivity
CPqD	Luxtera	Tektronix
Deutsche Telekom	M/A-COM Technology Solutions	TELUS Communications, Inc.
Dove Networking Solutions	Mellanox Technologies	TeraXion
EMC Corporation	Microsemi Inc.	Texas Instruments
Emcore	Microsoft Corporation	Time Warner Cable
Ericsson	Mitsubishi Electric Corporation	US Conec
ETRI	Molex	Verizon
FCI USA LLC	MoSys, Inc.	Xilinx
Fiberhome Technologies Group	MultiPhy Ltd	Yamaichi Electronics Ltd.
Finisar Corporation	NEC	ZTE Corporation