2020中国互连技术与产业大会

基于硅光子的下一代共封装光电一体化设计

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12/15/2020

intel®

Outline

- **Co-Packaged Silicon Photonics**
- **3-D Integrated 112Gb/s MRM Transmitter**
  - Nonlinear PAM-4 equalization
  - Integrated thermal control
- **112Gb/s CMOS TIA for Co-Packaged Optics**
- **Fully-Integrated Silicon Photonics Transceiver System**
- **Conclusions**

World of Data

Source: Keysight

AWS CLOUD

49 Availability Zones within 18 geographic Regions

Plans for 12 more Availability Zones and 4 more Regions

IaaS/PaaS

MICROSOFT AZURE

Available in 36 regions

Plans for 6 additional regions.

IaaS/PaaS/SaaS

IBM CLOUD

60 Data Centers in 19 countries

IaaS/PaaS

FACEBOOK

7 Mega Centers

Plans to expand 3 of the existing and add 4 new Mega Data centers

SaaS

GOOGLE CLOUD

13 regions and 49 zones

Plans for 5 additional regions and 14 zones

IaaS/PaaS/SaaS

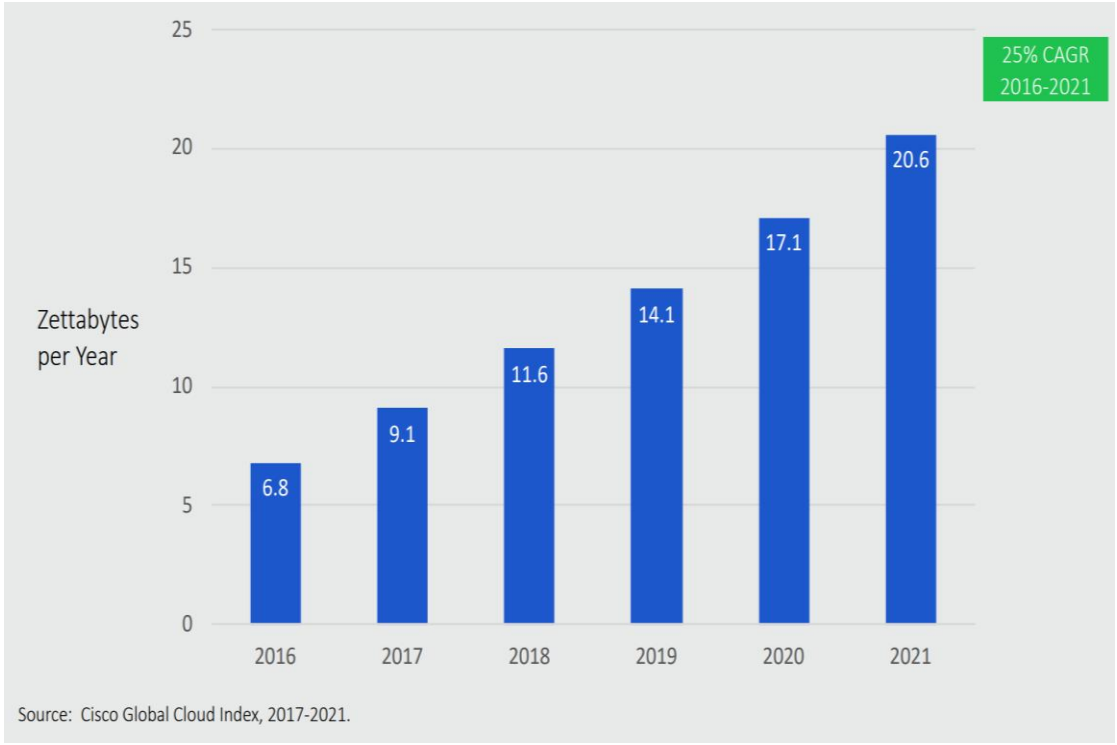
ALIBABA

7 regions and 33 zones

Plans for 4 additional regions

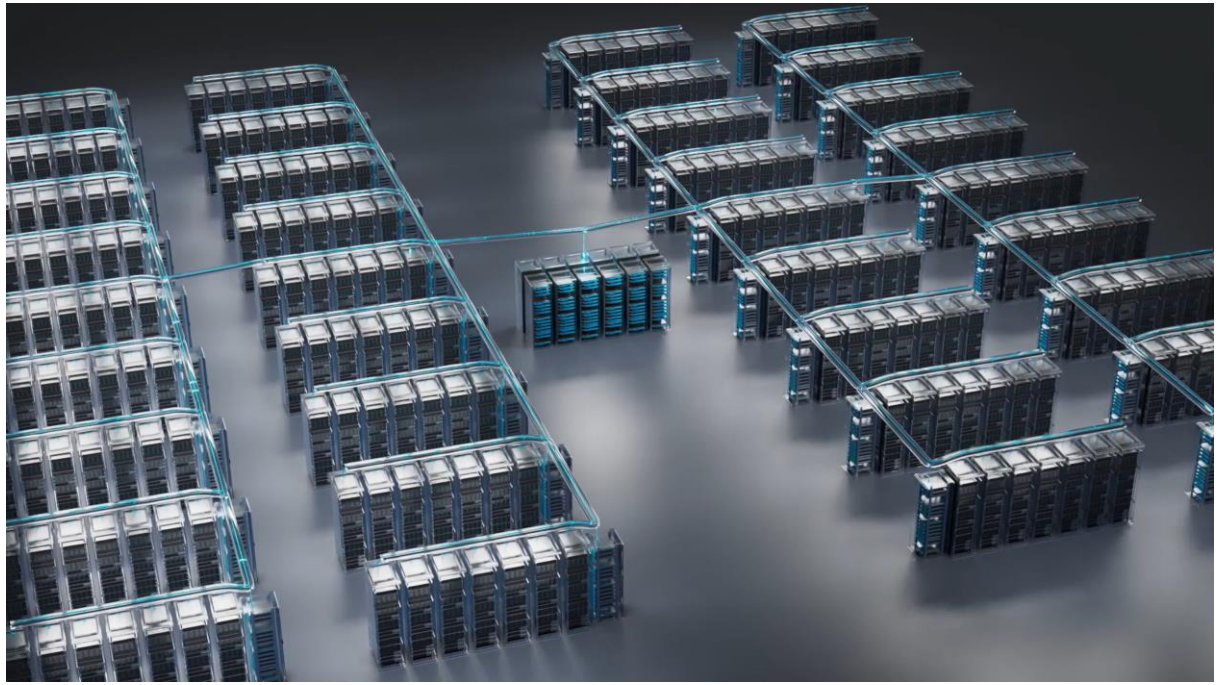
IaaS/PaaS

Source: Cisco



- Global data traffic continue to soar in the era of AI & Cloud.
- Annual global data center IP traffic will reach 20ZB by 2021.

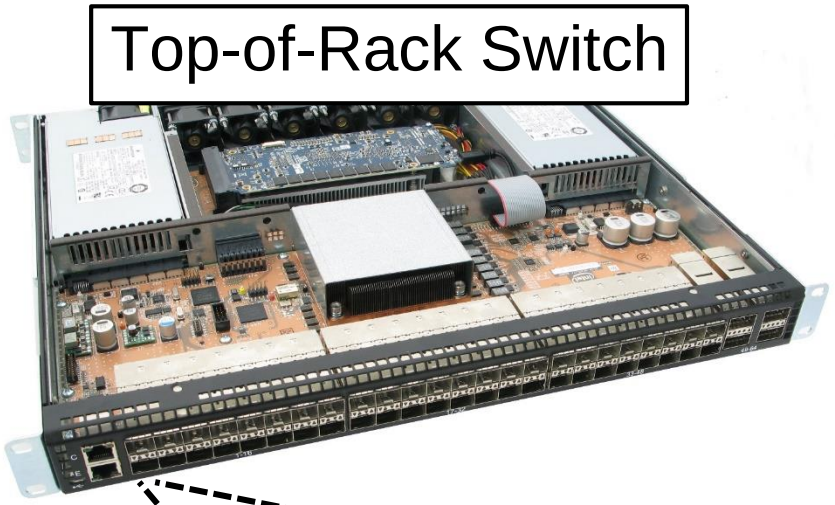
Data Center Interconnect Infrastructure

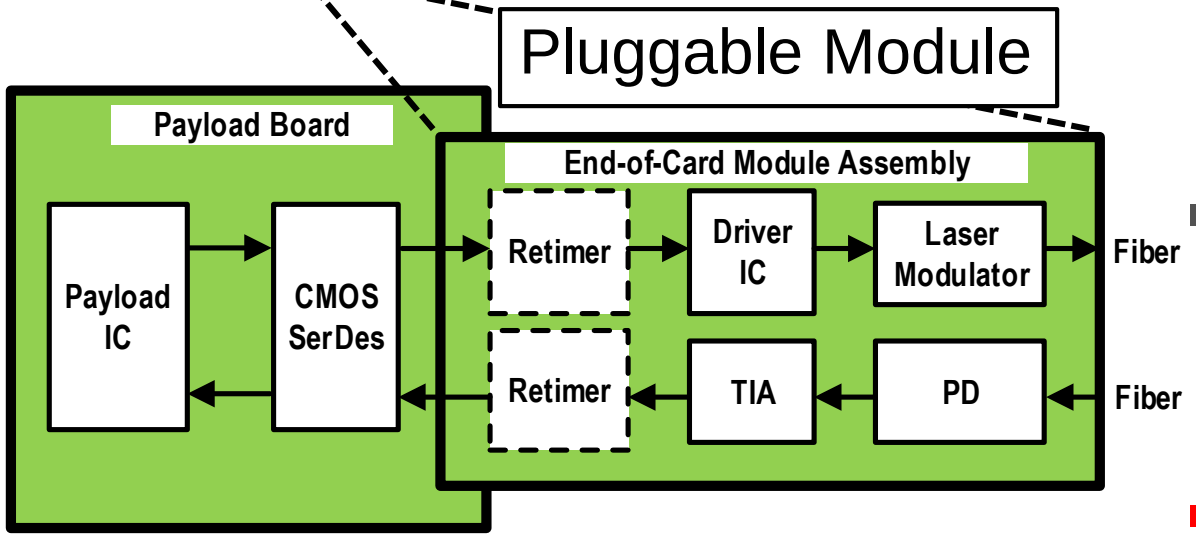


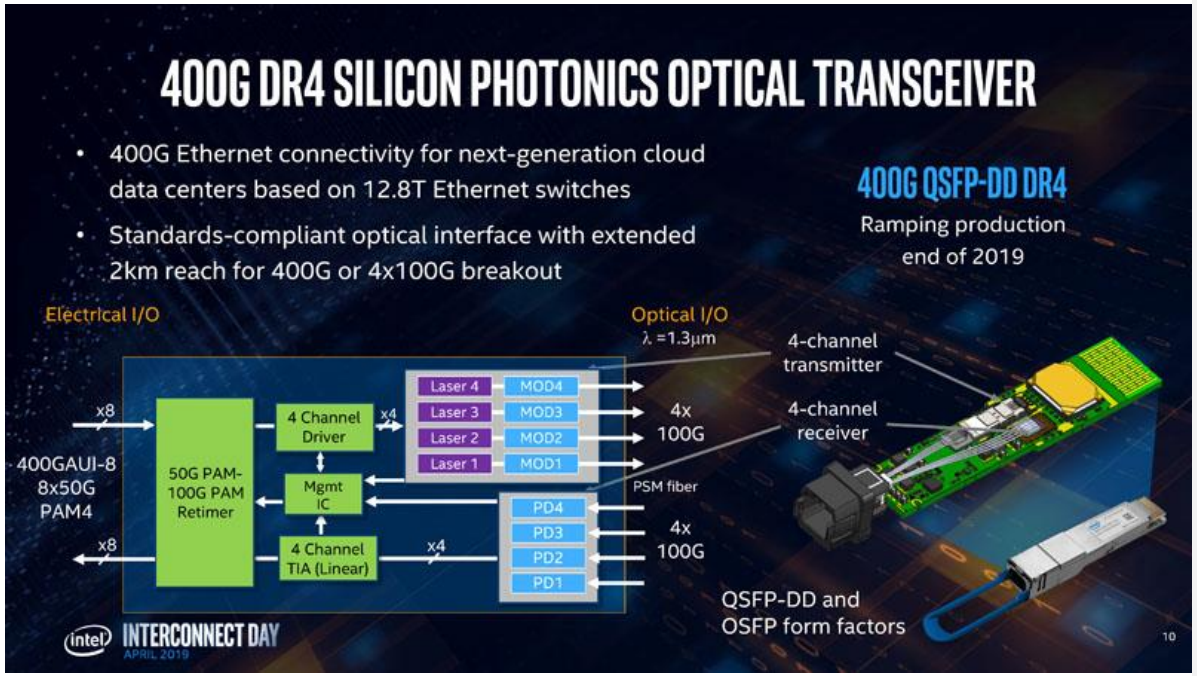
Intel's Pluggable Optical Module Products

- Optics dominate modern data center interconnect infrastructure from meters to tens of kilometers.
- Pluggable optical modules are commonly used to allow for user-friendly I/O management.

Pluggable 400GbE Solution (Today)



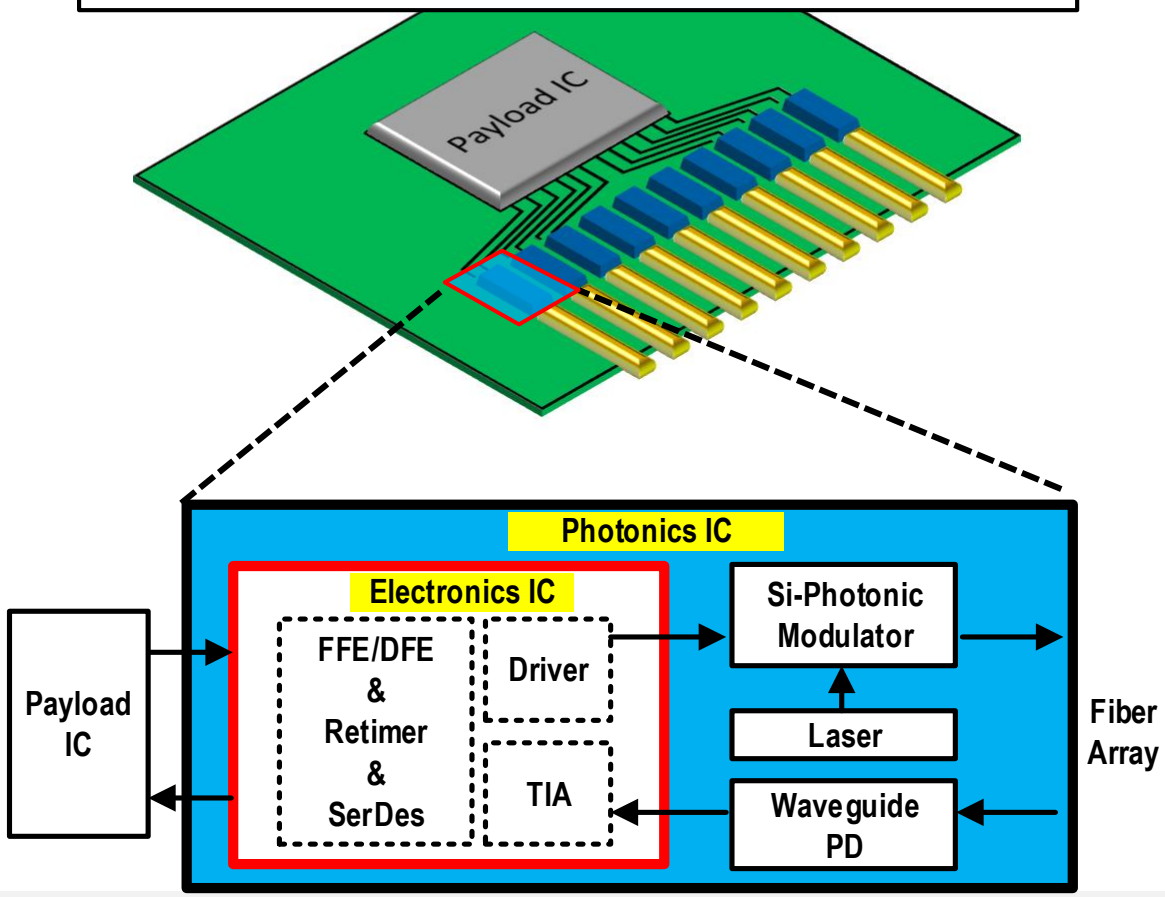




- Pluggable module increases cost, limits I/O density and performance scaling beyond 400G.
- 20pJ/bit now, need to go <5pJ/bit.

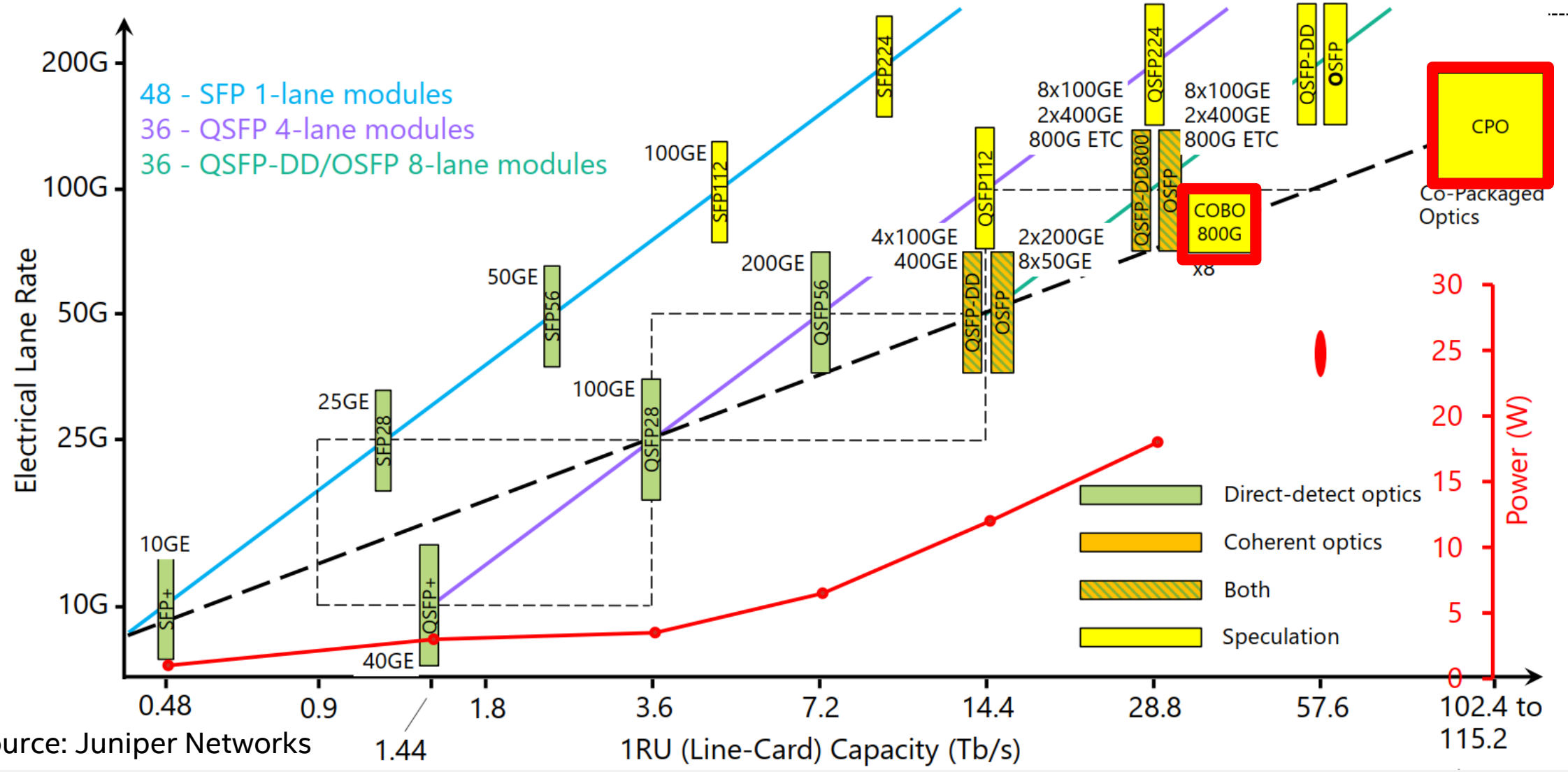
Co-Packaged Si-Photonic Transceiver

Payload Board with Co-packaged Si-Photonic Transceivers



- Bring optics closer to switch IC.
  - Ultra-short channel (XSR) eliminates expensive and power-hungry SerDes IC for lossy host-to-module interconnect.
- Co-packaged silicon photonics can deliver breakthrough improvement in cost and I/O density.
- Key: Integrated Silicon Photonics PIC + CMOS EIC engine.

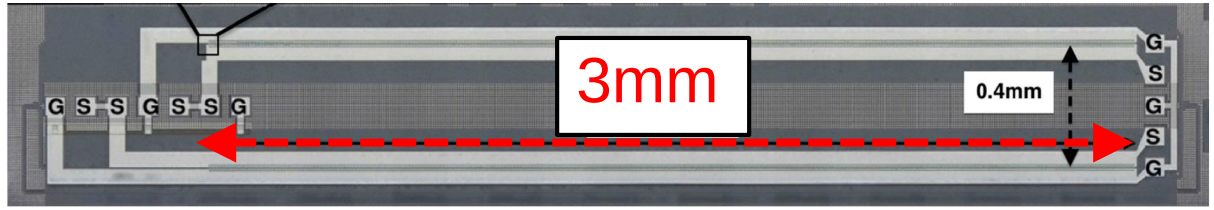
Roadmap From Pluggable to CPO



Source: Juniper Networks

Si-Photonic Microring Modulator

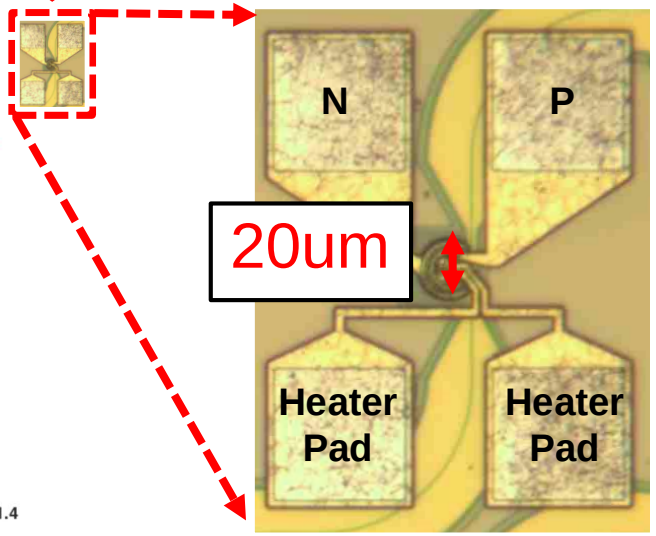
Mach-Zehnder Modulator



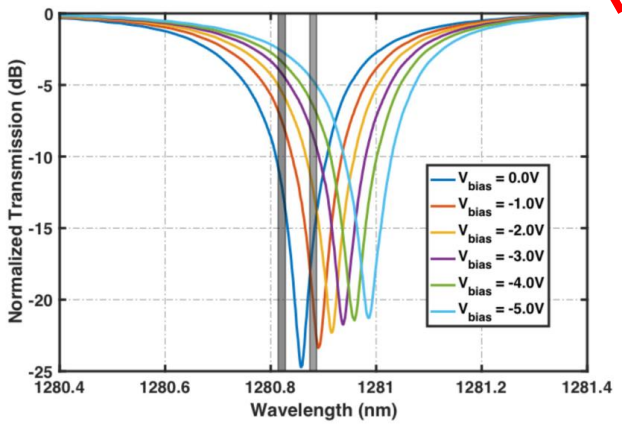
[R. Ding, Optcomm2014]

150X Size Reduction

10um MRM



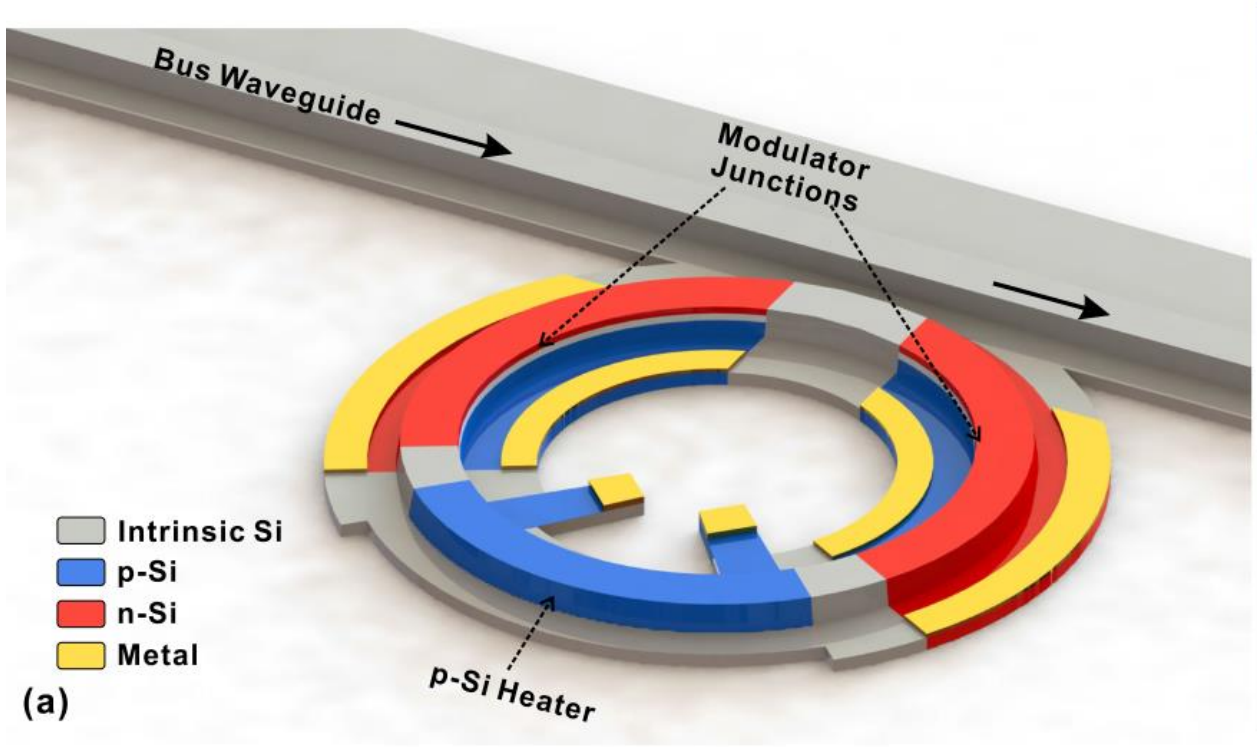
MRM Spectrum

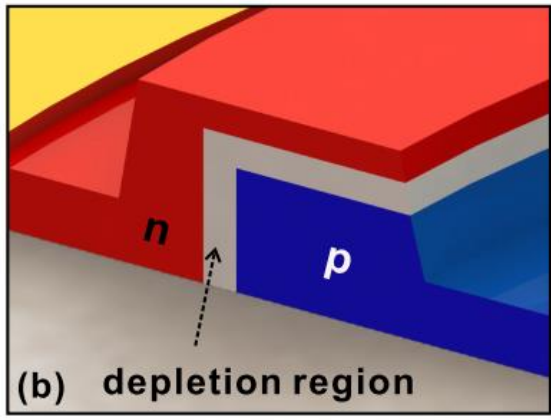


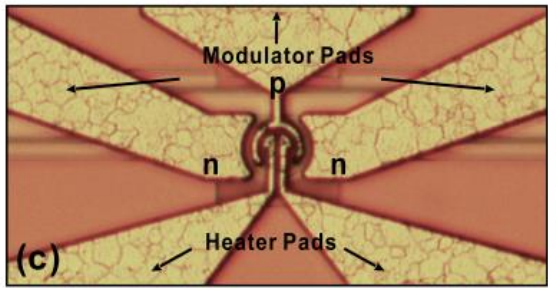
- **Key advantages:**
  - Ultra-compact (100X to 1000X smaller than MZM).
  - High EO bandwidth (>50GHz).
  - Scalable to DWDM design.
- **Challenges for PAM-4 link:**
  - High-swing driver for depletion-mode MRM.
  - Optical nonlinearities.
  - Sensitive to PVT variation.

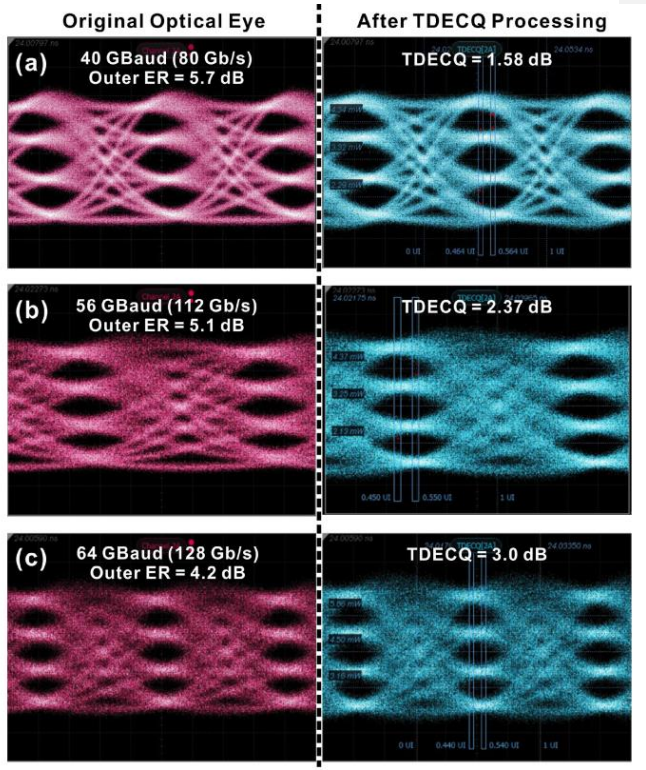
128Gb/s Silicon Microring Modulator

[J. Sun, JLT2018]









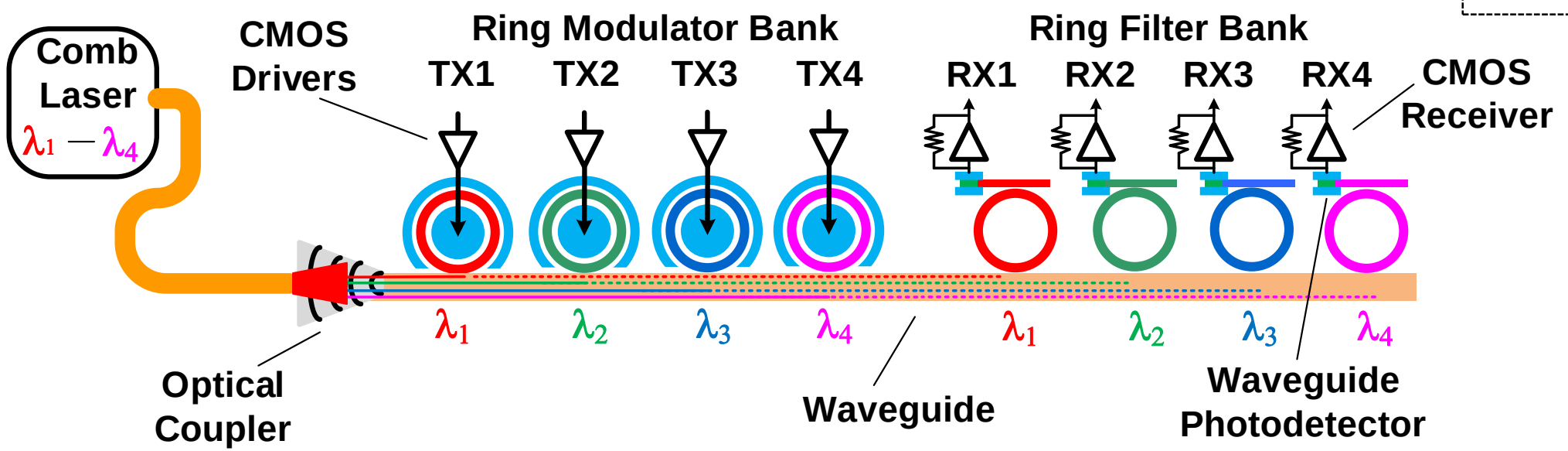
- World 1st demonstrated MRM with up to 128Gb/s modulation.
- Vπ·L = 0.52V·cm, heater efficiency = 19.5mW/π.
- >140GHz RC BW (40fF junction capacitance), 50GHz EO 3dB BW.

MRM-based Co-Packaged Switch by Intel

https://newsroom.intel.com/news/intel-demonstrates-industry-first-co-packaged-optics-ethernet-switch/

- World 1st demonstrated 12.8Tb/s ethernet switch with MRM-based 400G DR4 compliant co-packaged optical links.

Microring-based Si-Photonic DWDM Link



- DWDM link utilizes MRM array as modulators and filters.
- Bandwidth scales with the degree of WDM.
- Ideally little or no interference between channels.
- Example: a 16-λ MRM-based DWDM link with 100GHz Channel Spacing, 100Gb/s PAM-4 per-MRM = 1.6Tb/s/fiber!

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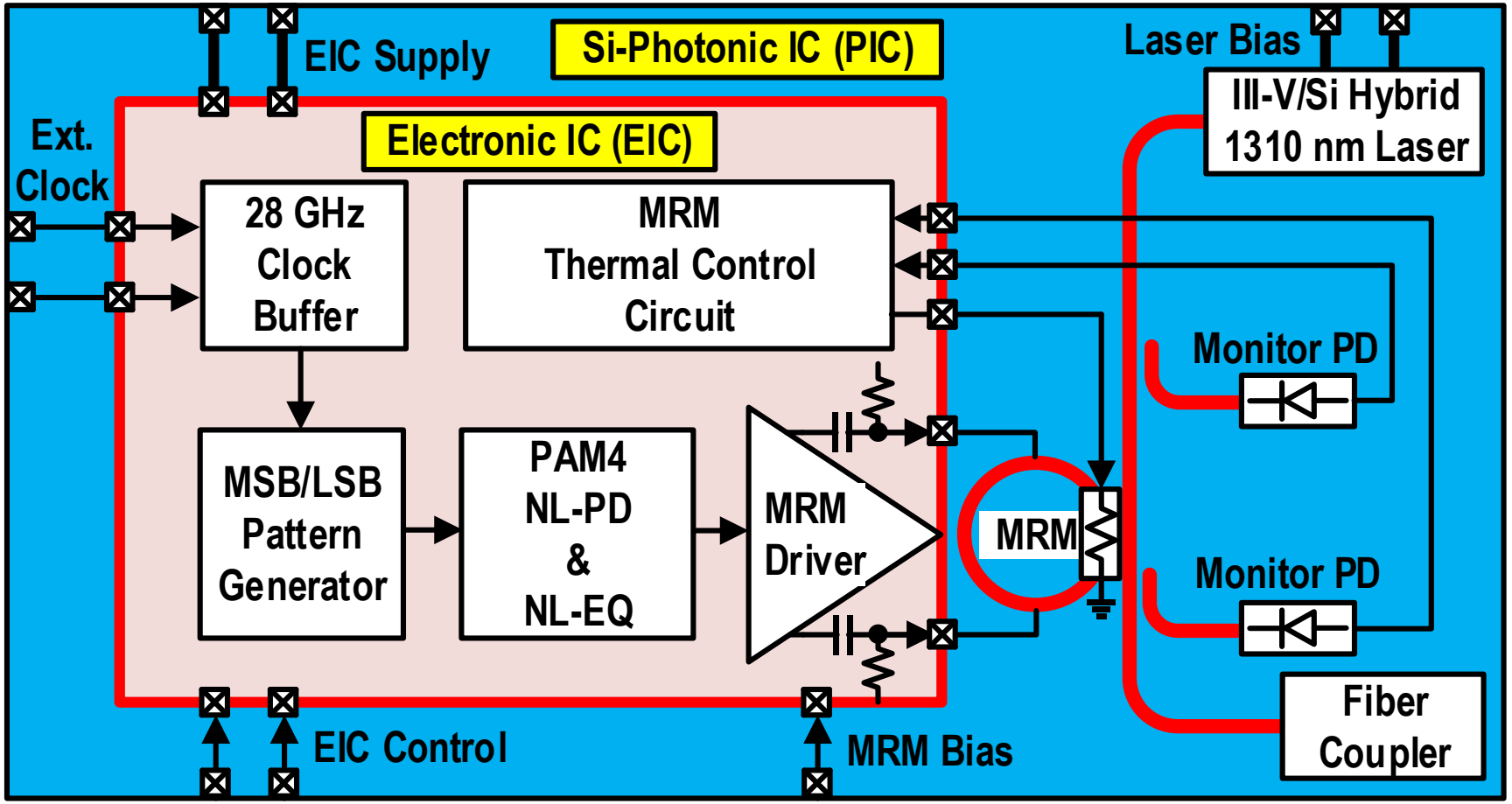
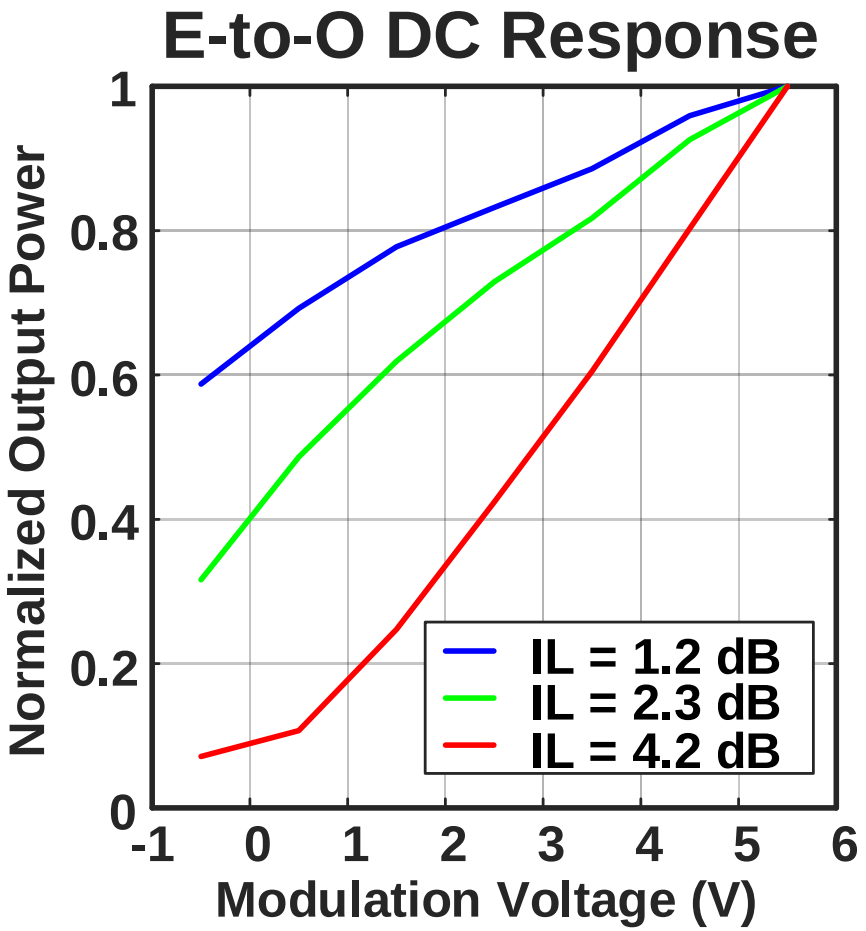
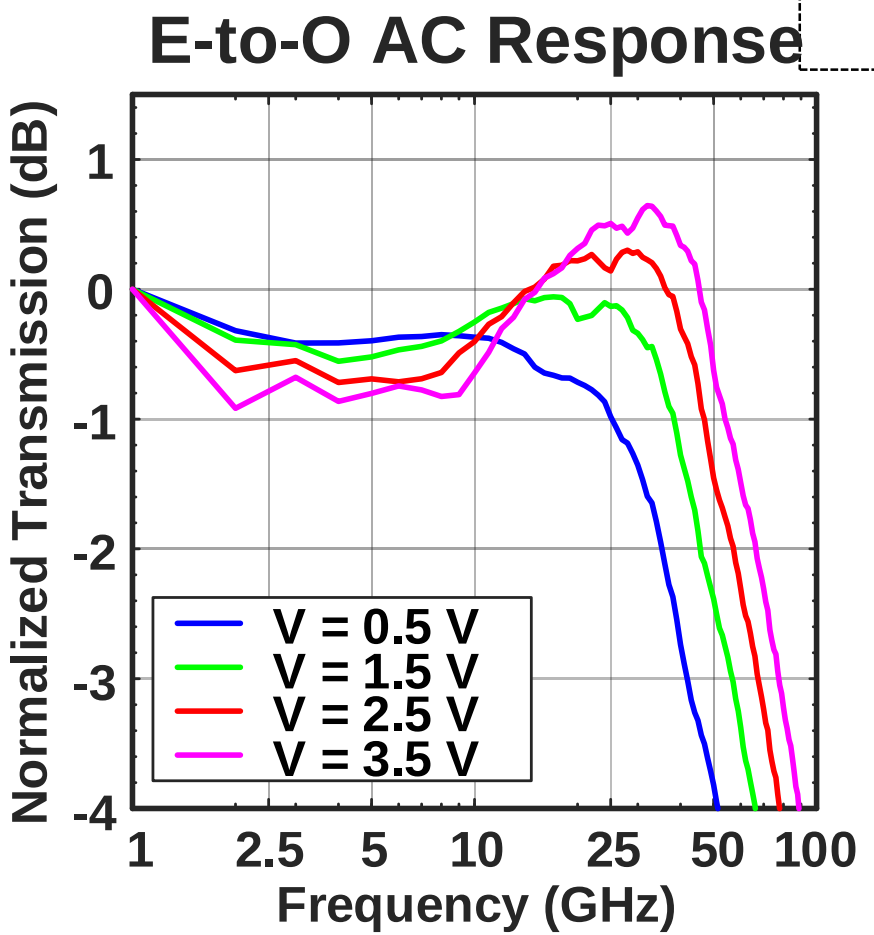
3D-Integrated Si-Photonic Transmitter



- AC-coupled differential MRM driver with 3Vpp output swing.
- Integrated heater and PD for MRM wavelength control.

MRM Nonlinearities

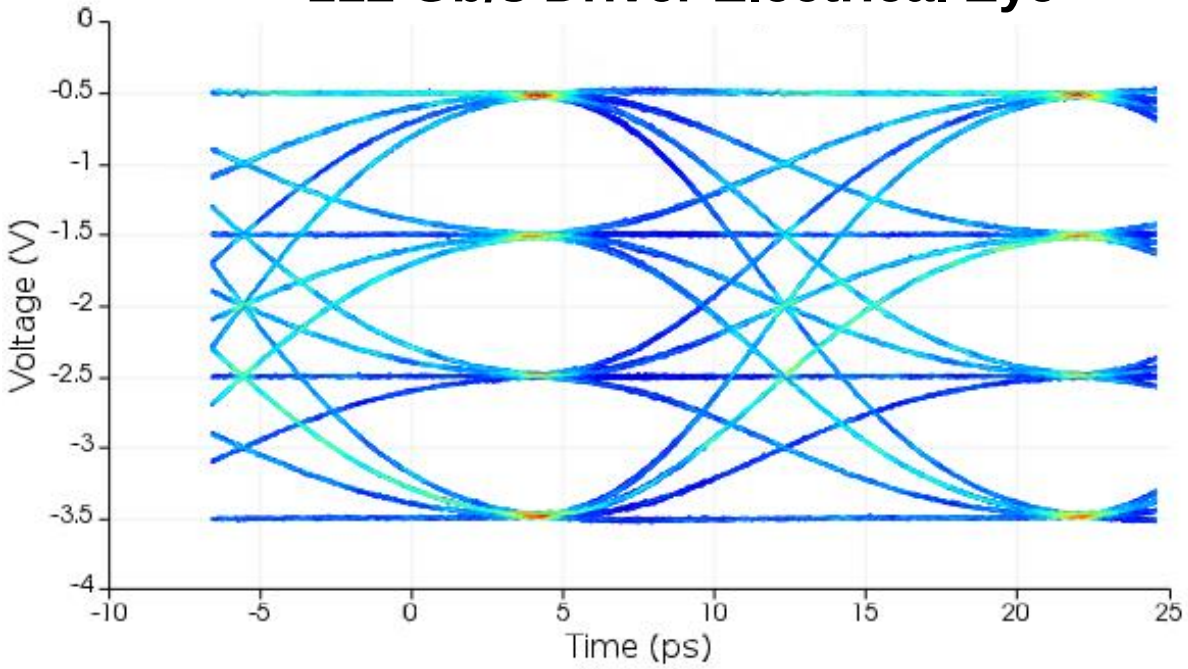




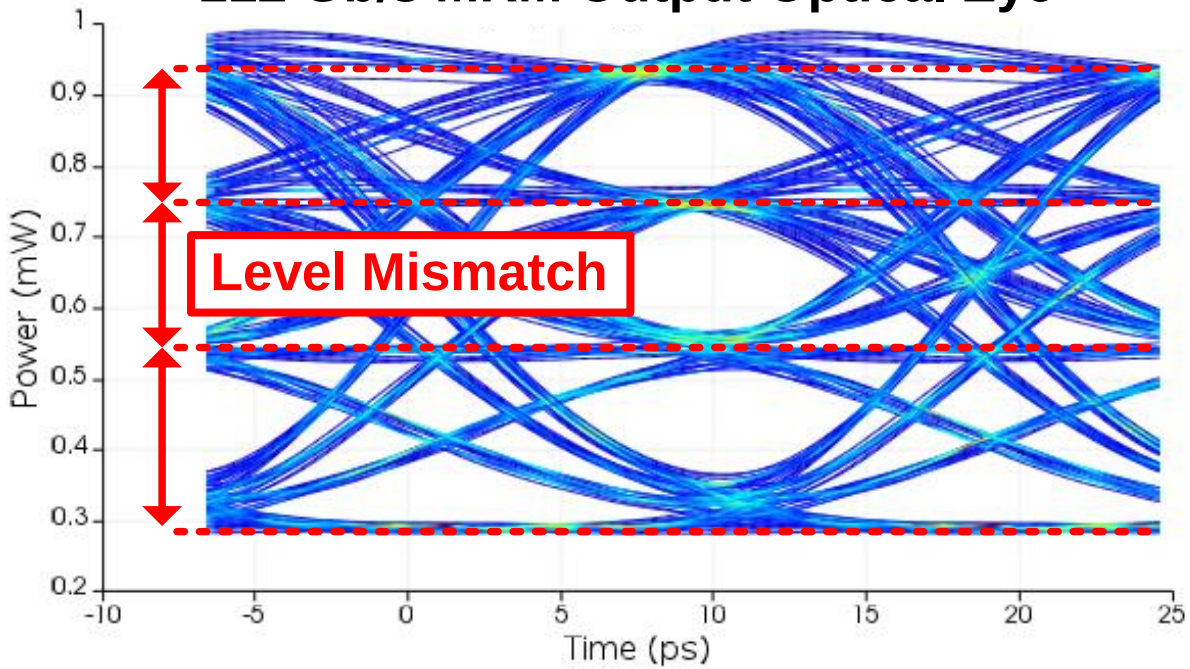
- Nonlinear DC response → Static nonlinearity.
- Voltage-dependent AC response → Dynamic nonlinearity.

Effect of Static Nonlinearity

112 Gb/s Driver Electrical Eye



112 Gb/s MRM Output Optical Eye

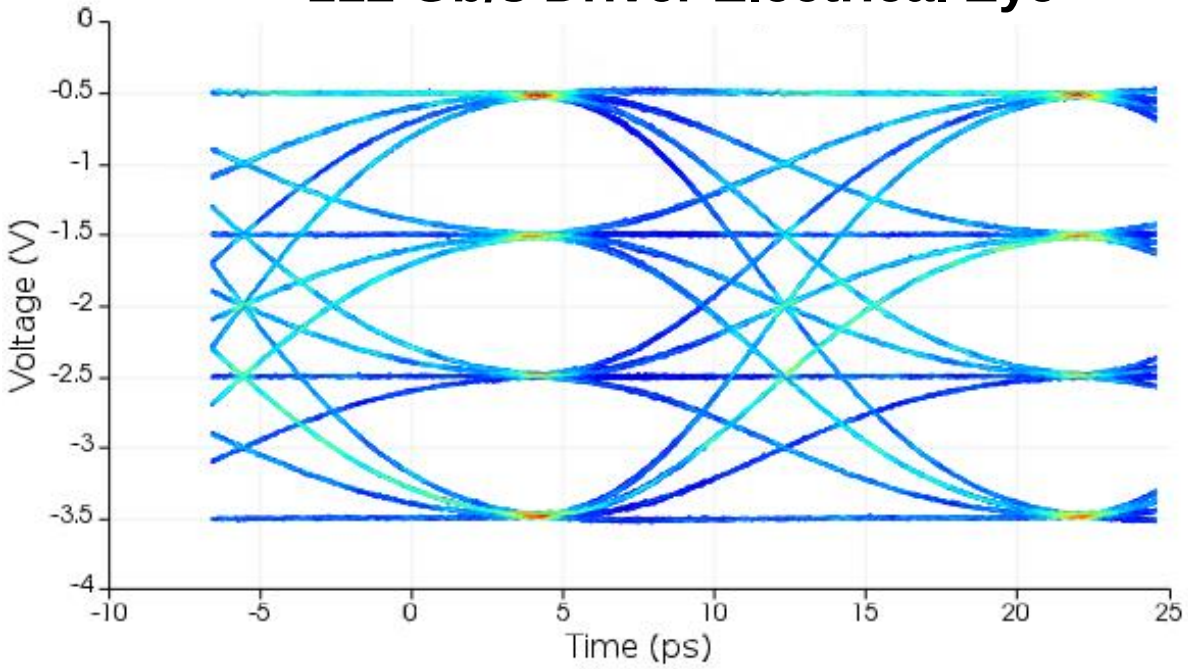


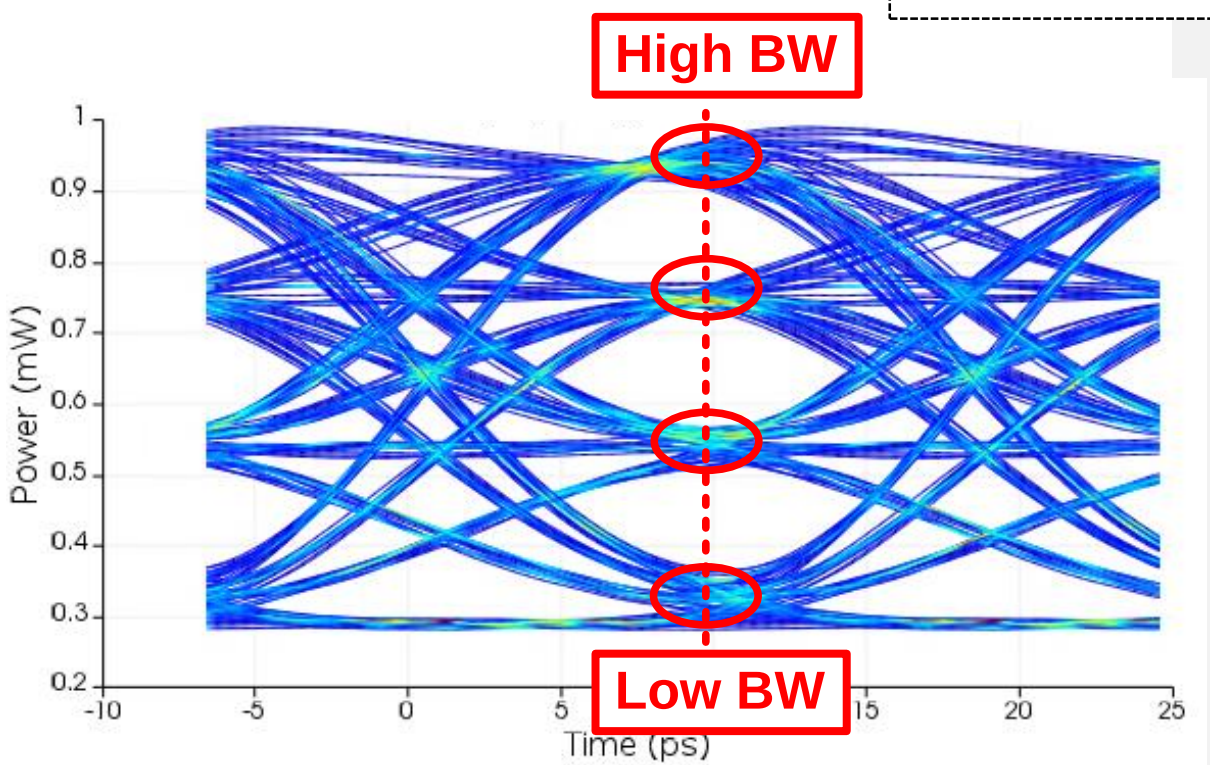
*RLM is Ratio of Level Mismatch.

- Asymmetric optical levels → RLM penalty.

Effect of Dynamic Nonlinearity

112 Gb/s Driver Electrical Eye

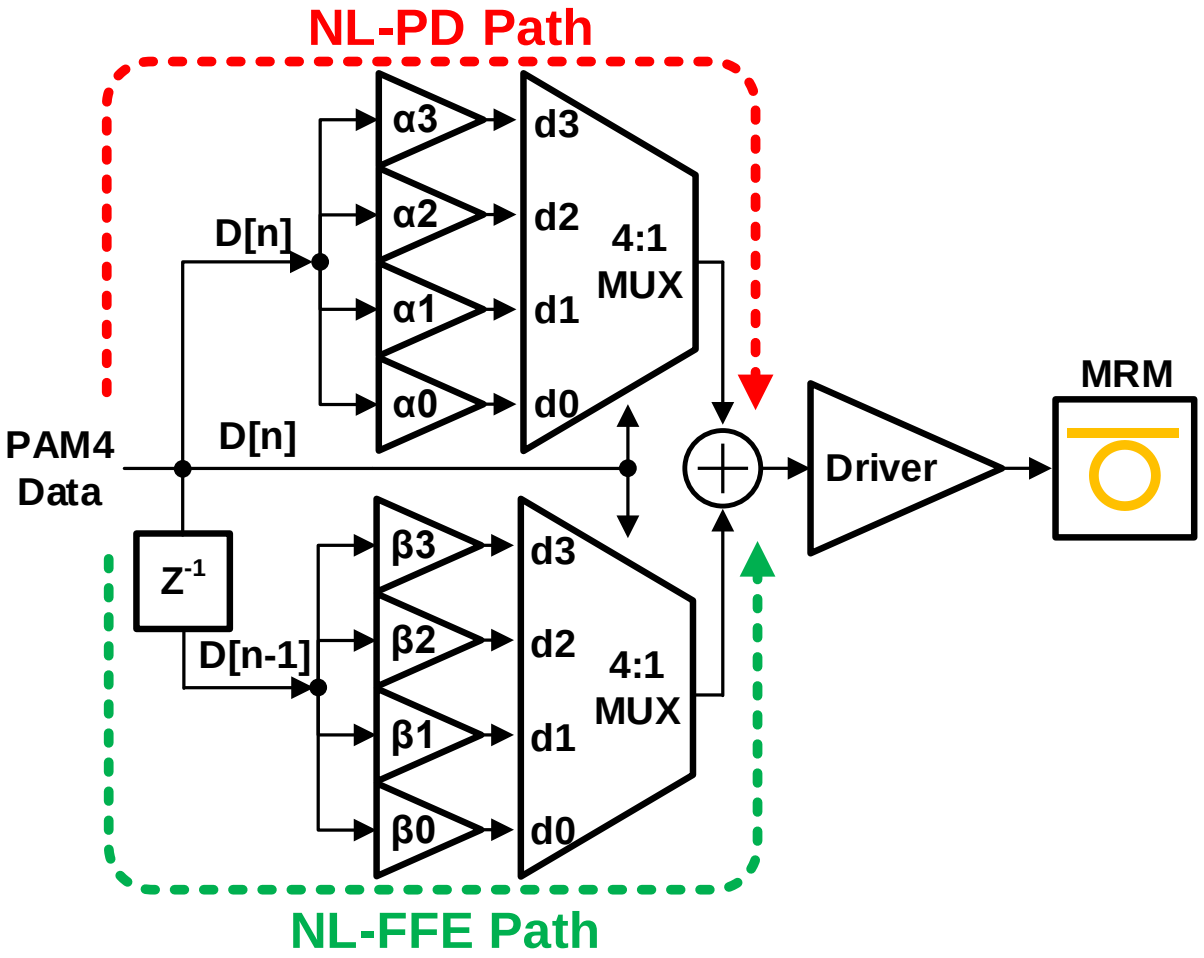




*TDECQ is Transmitter Dispersion Eye Closure (Quaternary).

- Asymmetric optical levels → RLM penalty.
- Level-dependent ISI → TDECQ and BER penalty.

Dual-Path PAM-4 Nonlinear Equalizer



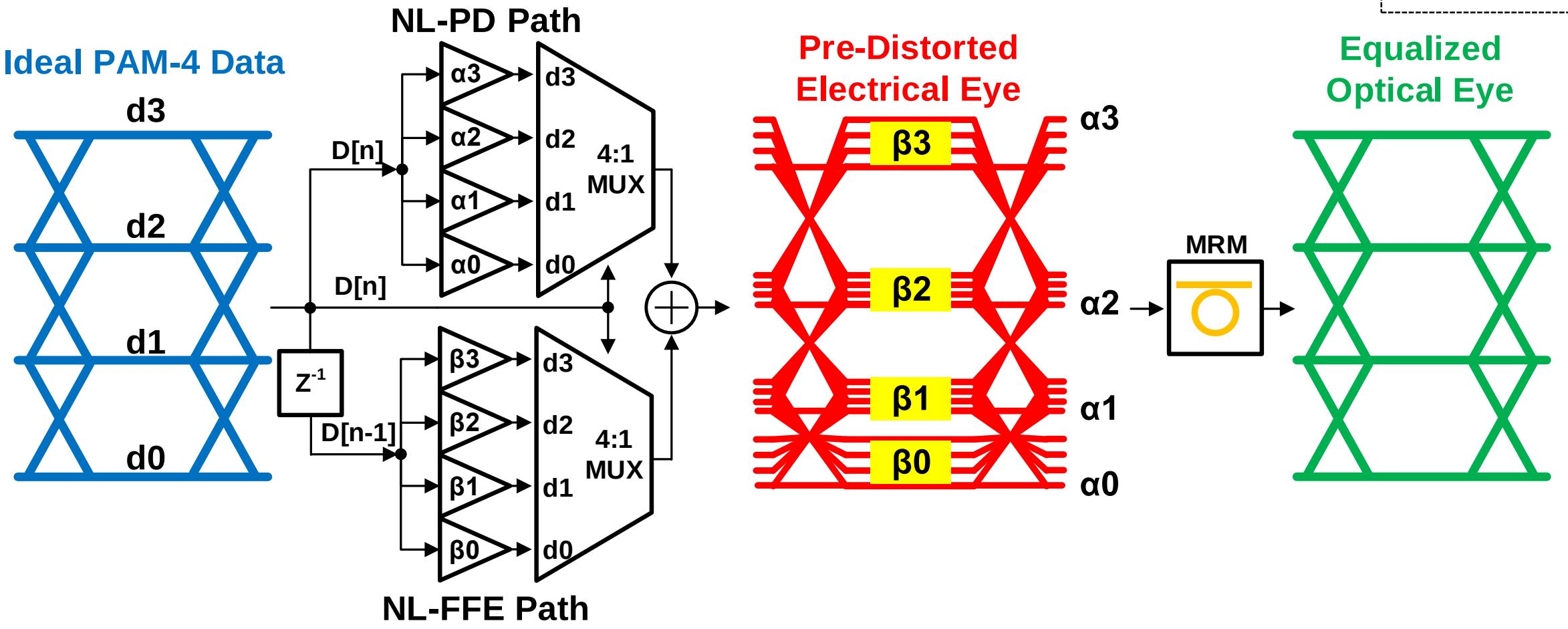
- Dual-path equalizer to compensate for MRM nonlinearities.
- Nonlinear pre-distortion path:

→ Level-dependent gain.

- Nonlinear FFE path:

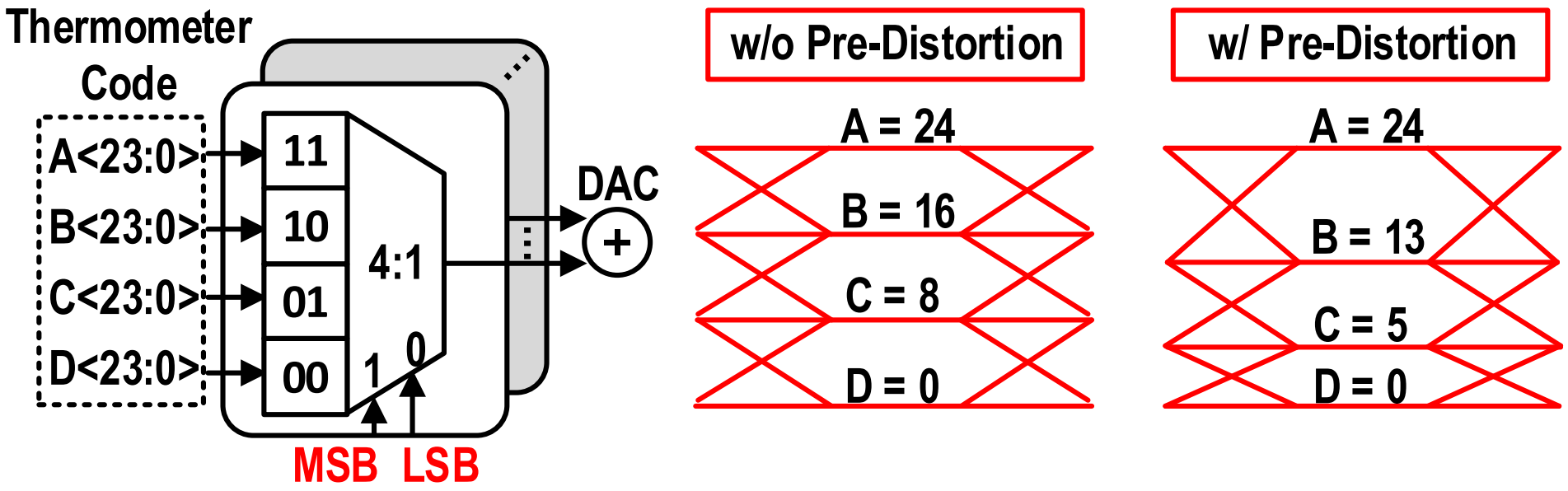
→ Level-dependent FFE coefficient.

Dual-Path PAM-4 Nonlinear Equalizer



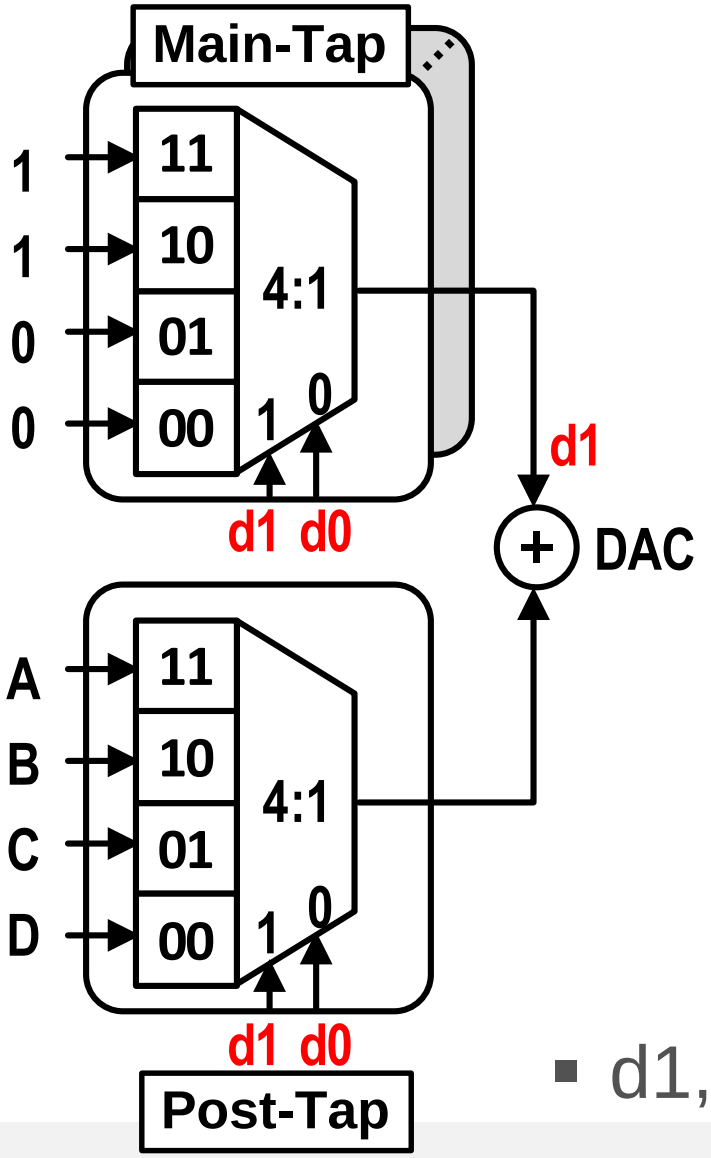
$$Dout\,[n] = D\,[n] * \alpha\,(D\,[n]) + D\,[n-1] * \beta\,(D\,[n])$$

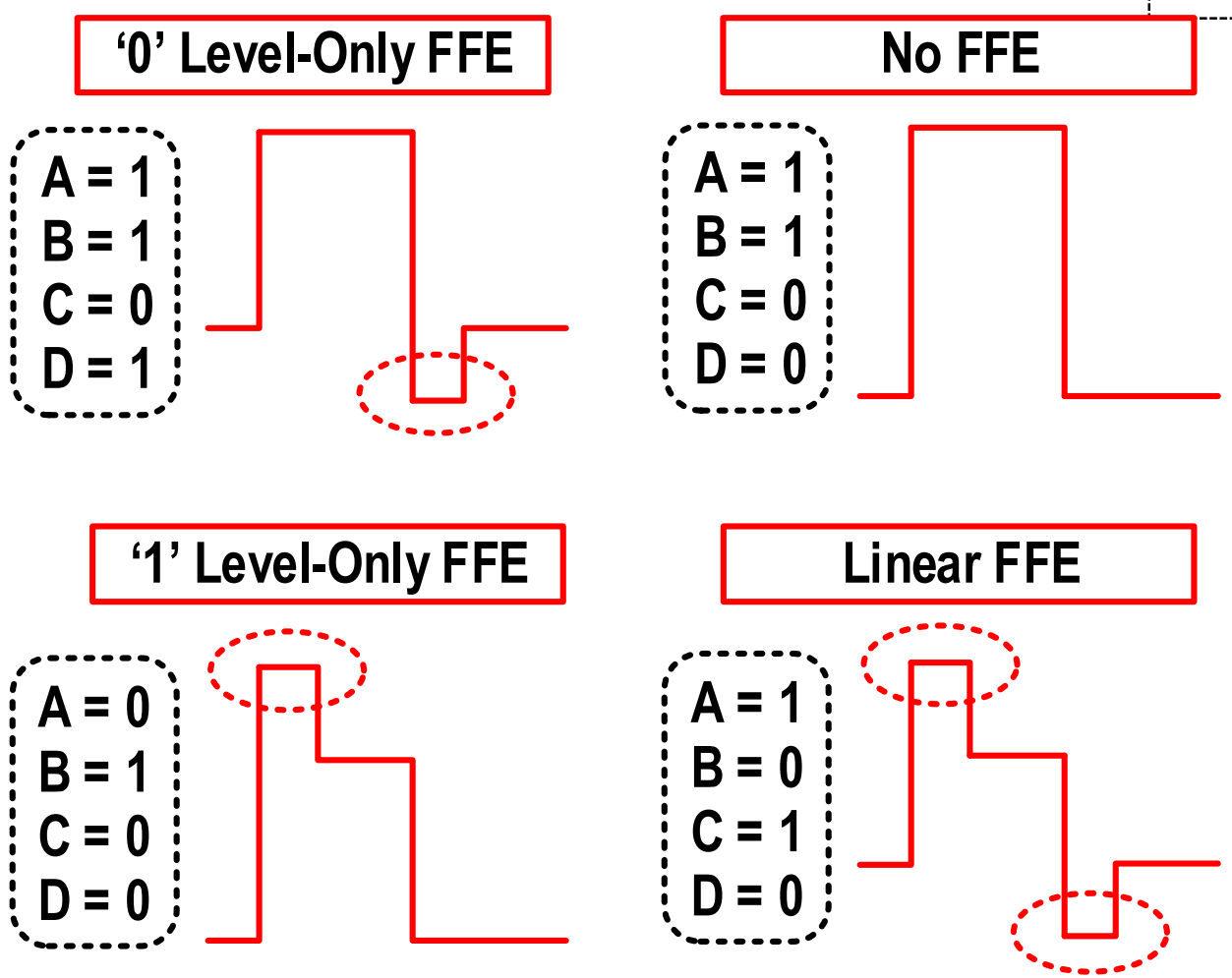
LUT-based PAM-4 Nonlinear Pre-Distortion



- Compatible with CMOS serializer and DAC driver.
- 4-bit LUT array addressed by MSB/LSB data directly.
- PAM-4 levels can be mapped to the table values of LUT array.

LUT-based Nonlinear FFE (NRZ)





- d1, d0 represents data stream with 1UI delay.

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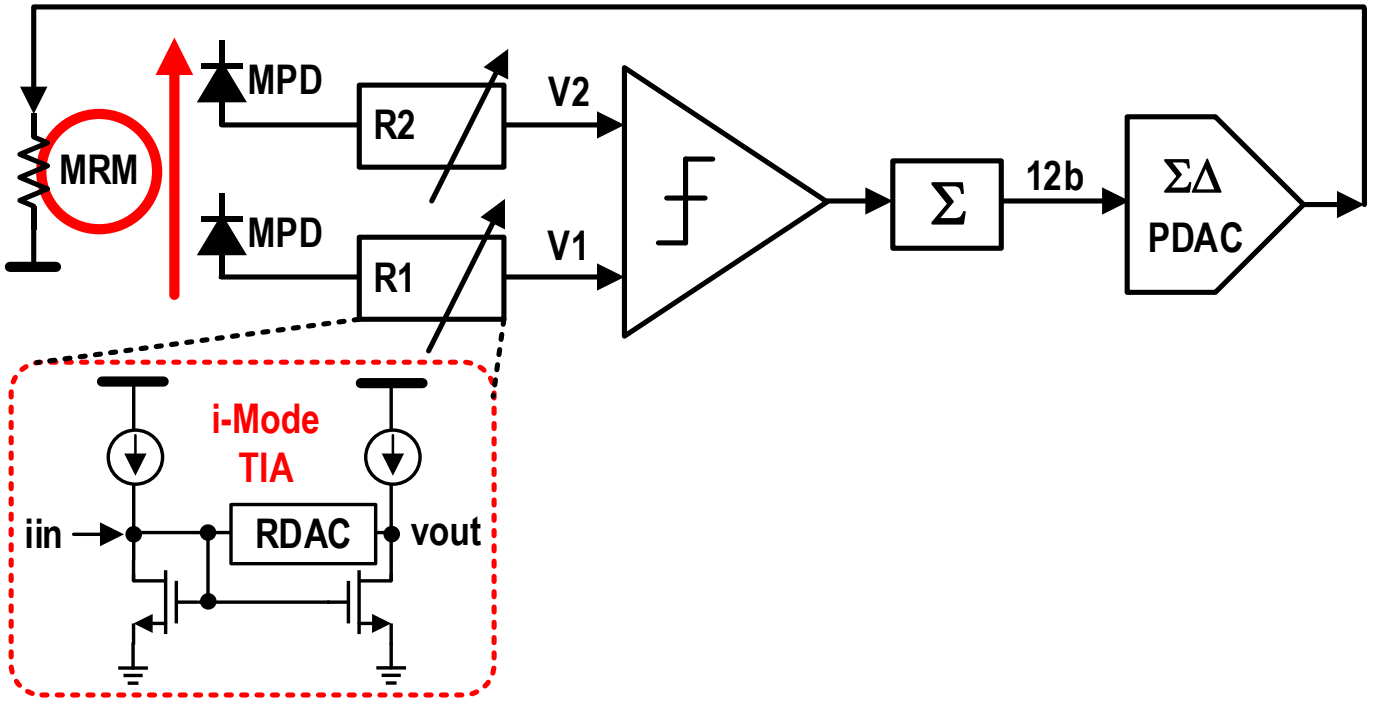
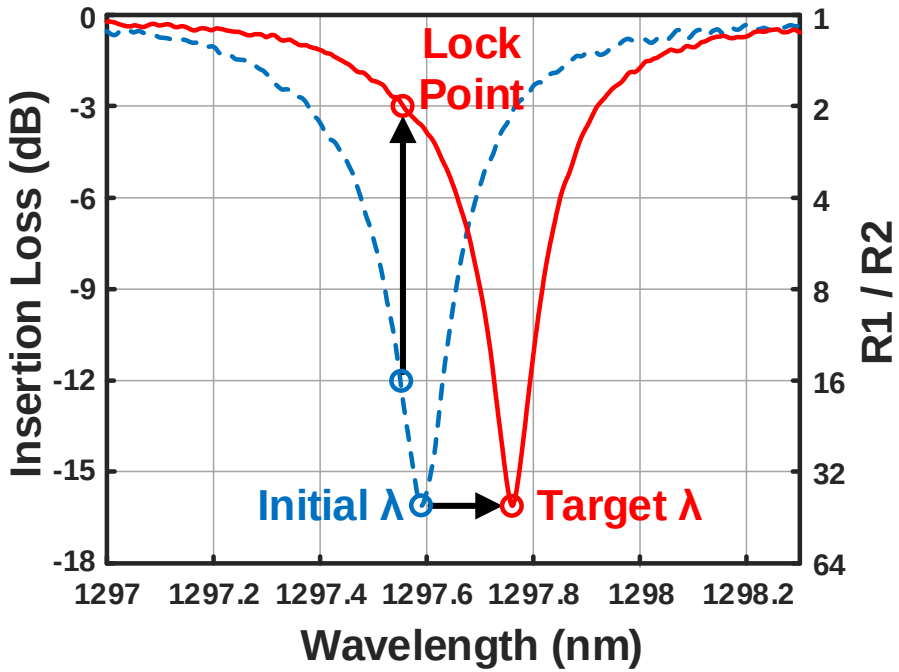
- Co-Packaged Silicon Photonics
- **3-D Integrated 112Gb/s MRM Transmitter**
  - Nonlinear PAM-4 equalization
  - **Integrated thermal control**
- 112Gb/s CMOS TIA for Co-Packaged Optics
- 112Gb/s Silicon Photonics Link Demo
- Conclusions

Integrated Thermal Control Loop

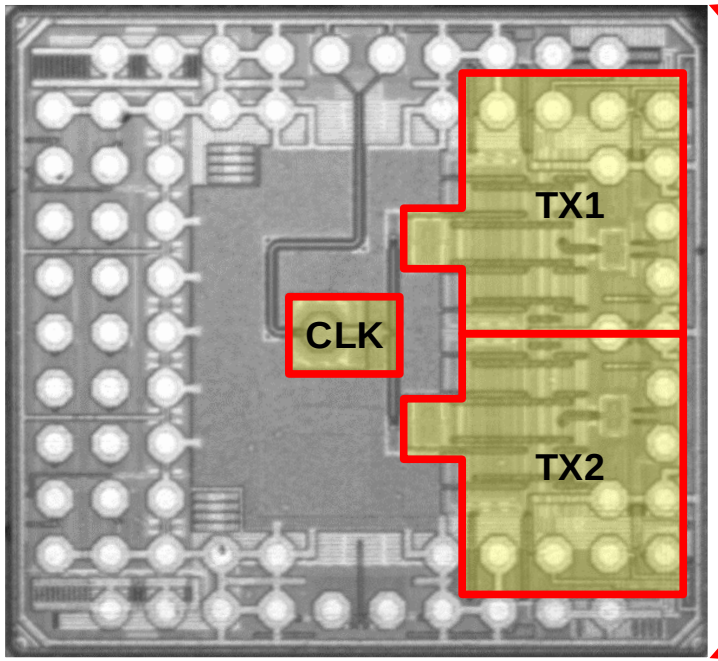




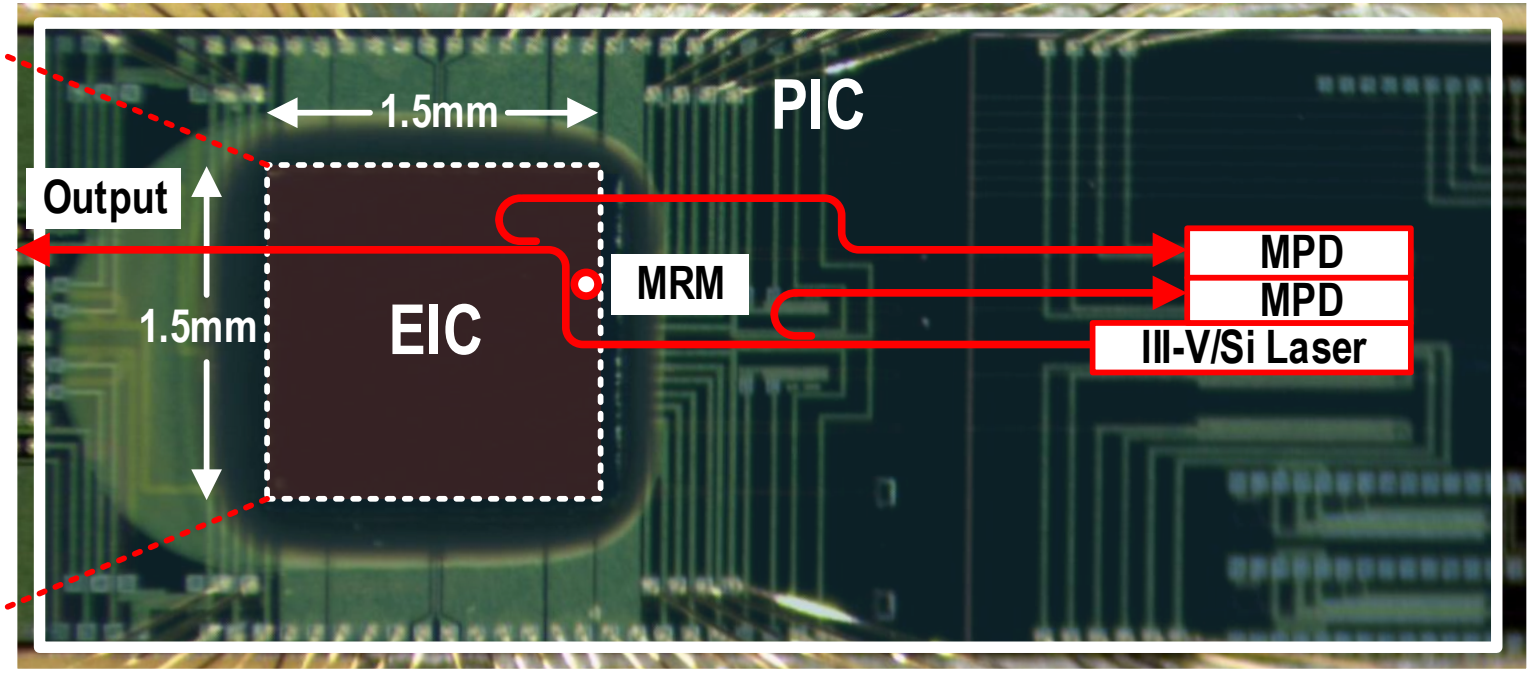
- Low-power Bang-Bang control loop with dual sensor TIA.
- Locking based on MRM insertion loss (IL target is set by R1/R2).
- Decouples absolute laser power fluctuation.

EIC and PIC Floorplan

EIC Die-Photo

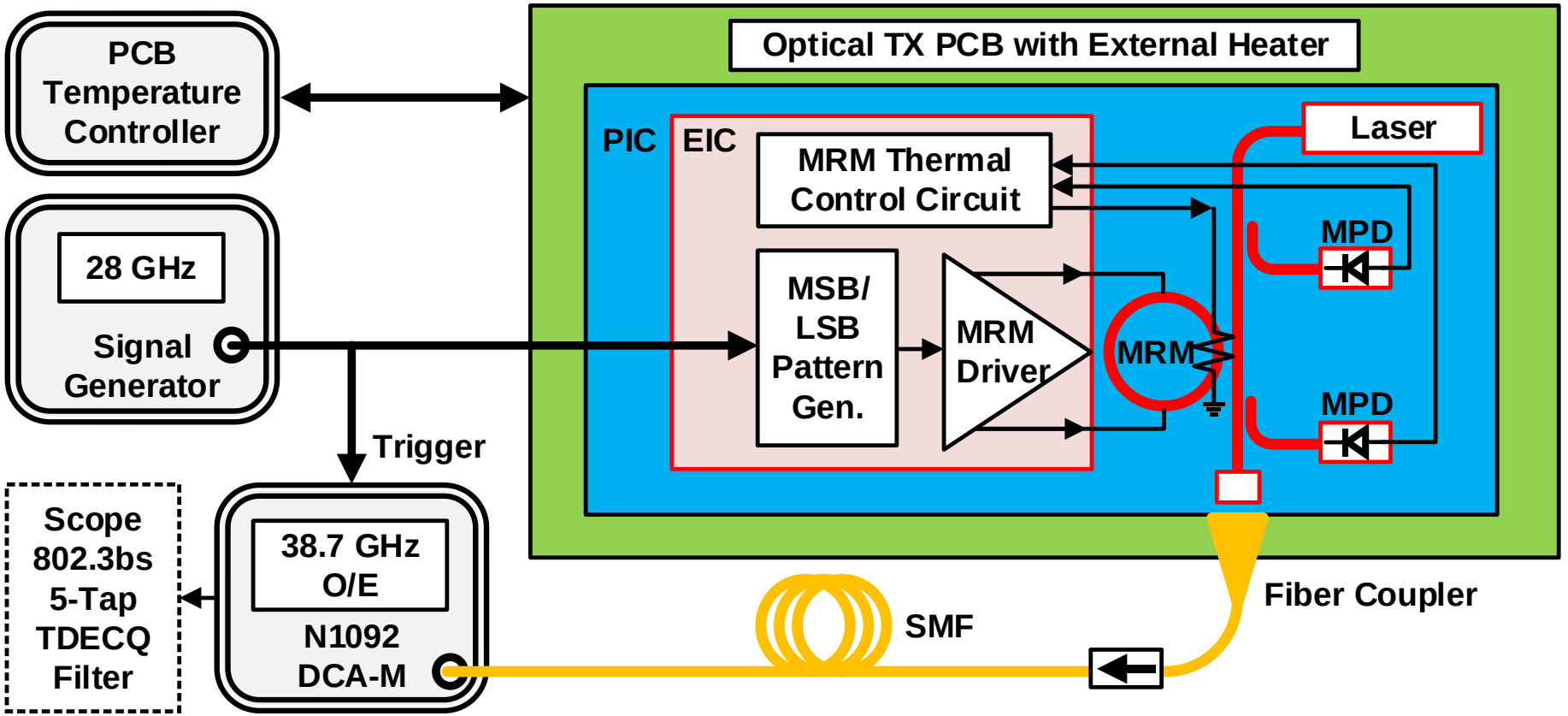


3D-Integrated EIC+PIC using Cu-Pillar Packaging



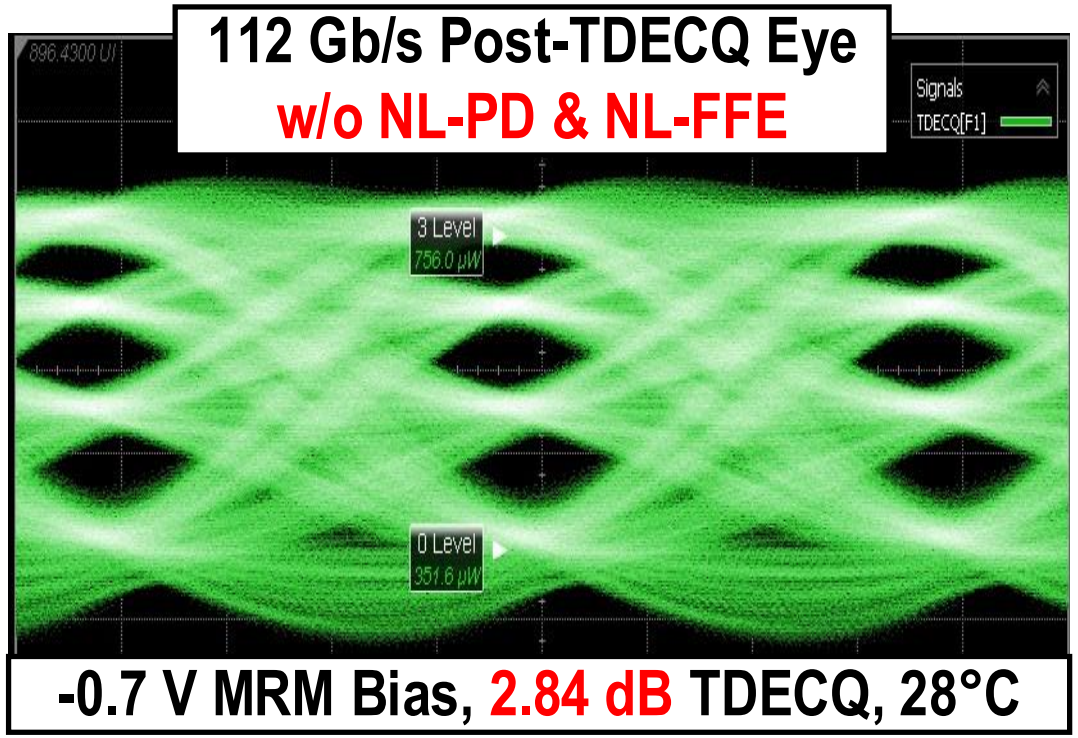
- EIC was fabricated using 28nm CMOS process.
- Transmitter active area is ~0.4mm^2.

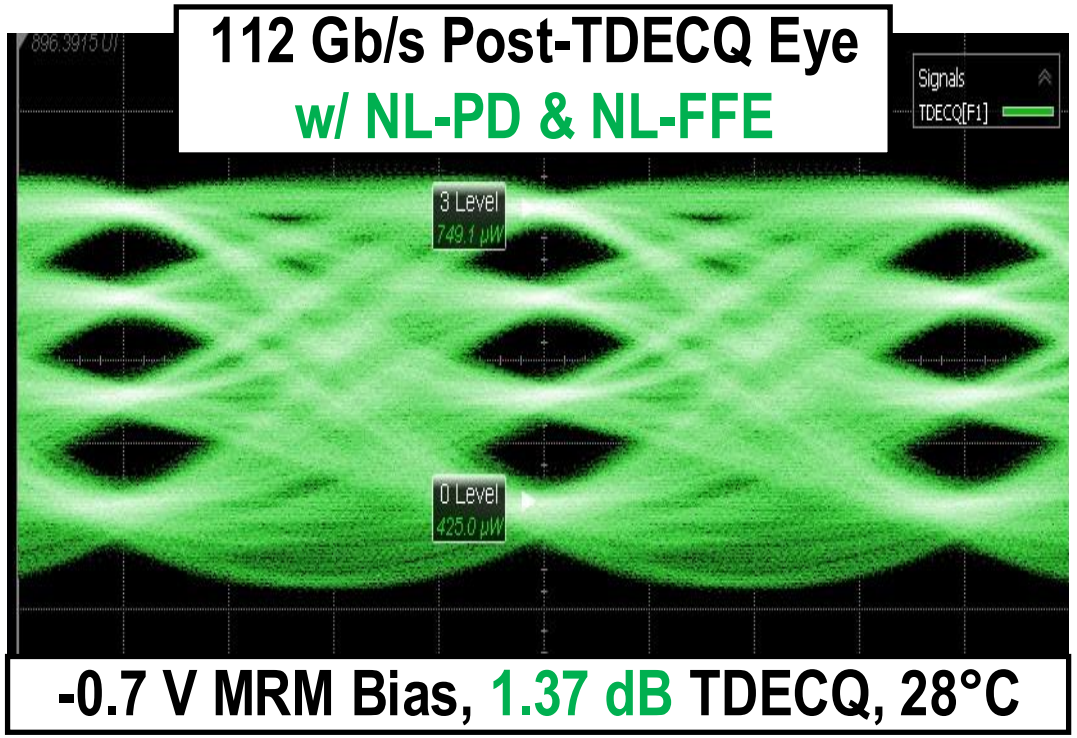
Optical Measurement Setup



- Chip-on-board assembly with external temperature controller.
- TX output directly-detected by a 38.7GHz optical oscilloscope.

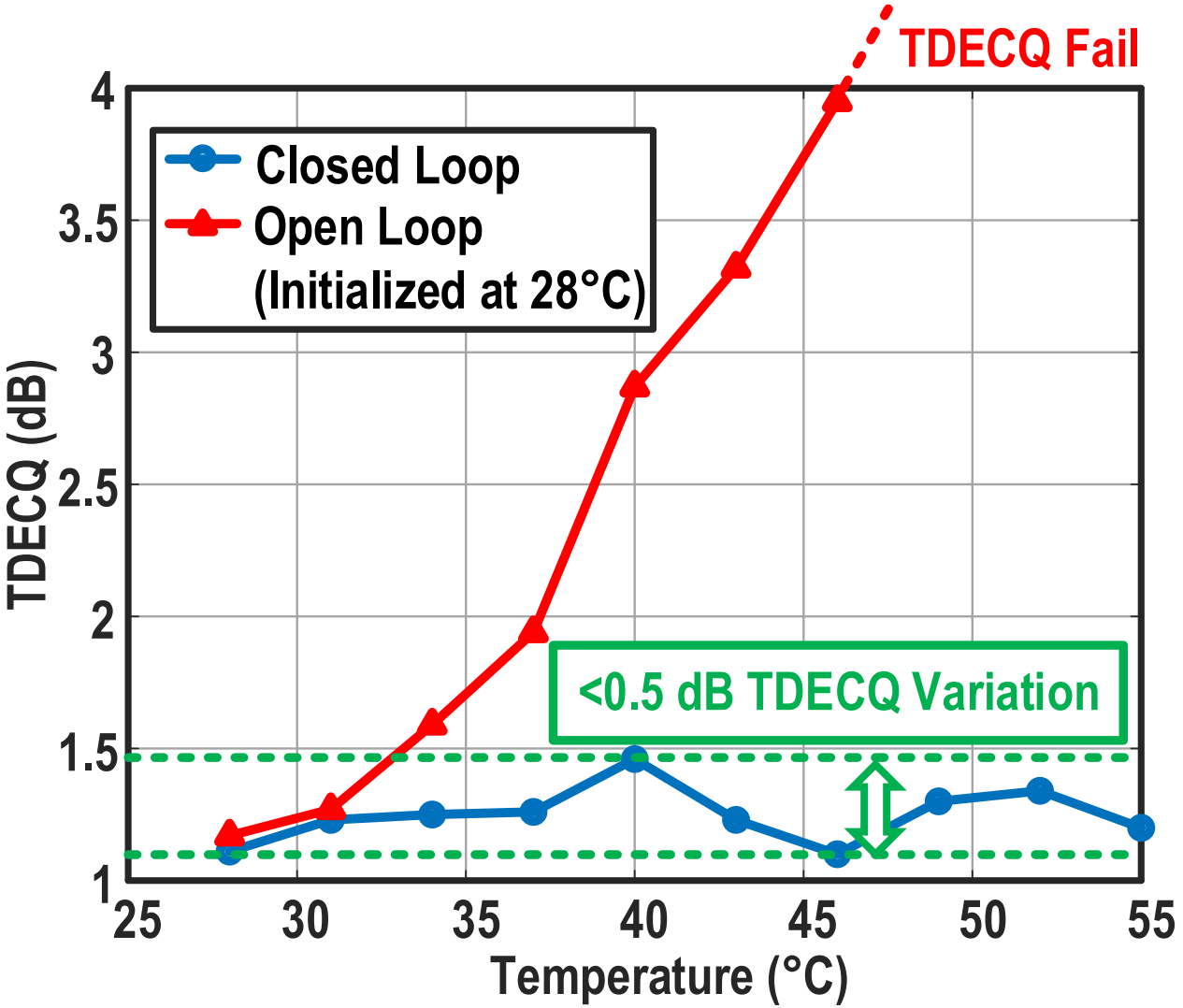
Effect of Nonlinear PAM-4 Equalization

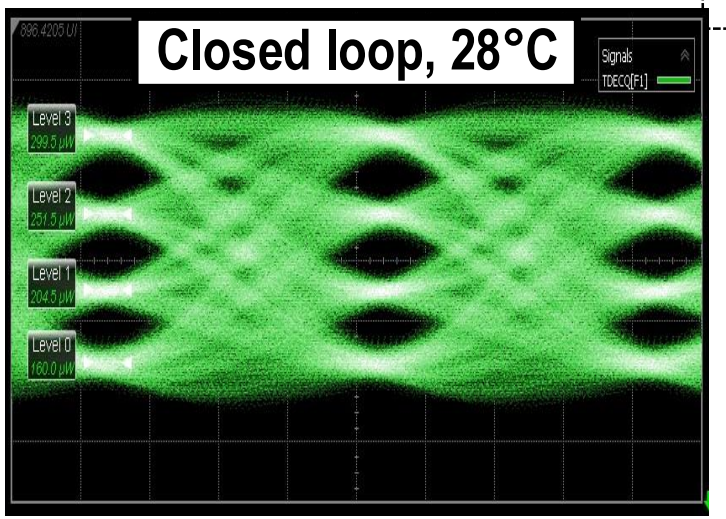


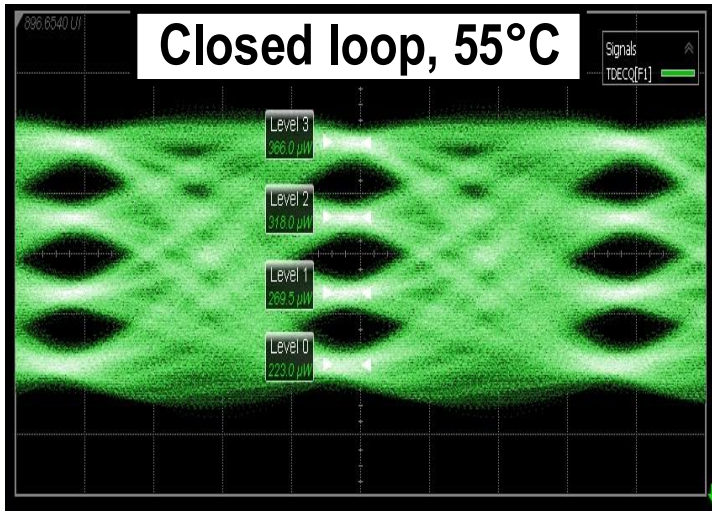


- ~1.5dB TDECQ improvement by NL-PD and NL-FFE.

Thermal Control Test (Closed Loop)







Comparison with 3D-Integrated MZM-TX

	G. Denoyer JLT 2015	E. Temporiti ISSCC 2016	C. Li BCICTS 2018	This Work
Modulator	TW-MZM	TW-MZM	Segmented-MZM	MRM
Device Size	3.36mm	3mm	7mm	20um
On-Chip Laser	No	No	No	Yes
EIC Process	130nm BiCMOS	55nm BiCMOS	16nm CMOS	28nm CMOS
Signaling	NRZ	NRZ	PAM-4	PAM-4
Data Rate	56Gb/s	56Gb/s	56Gb/s	112Gb/s
Driver Swing	$4V_{pp}$	$1.6V_{pp}$	$1.8V_{pp}$	$3V_{pp}$
On-Chip Pattern Gen. + Serializer	Yes	No	Yes	Yes
EIC Power	593mW	300mW	708mW	*676mW
EIC-only Energy-Efficiency	10.6pJ/bit	5.35pJ/bit	12.6pJ/bit	6pJ/bit

*Excluding 160mW on-chip laser power.

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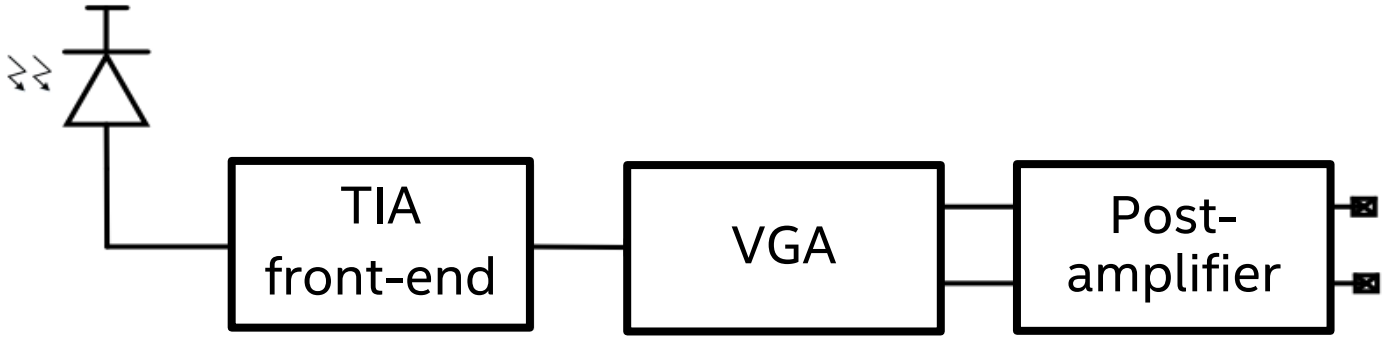
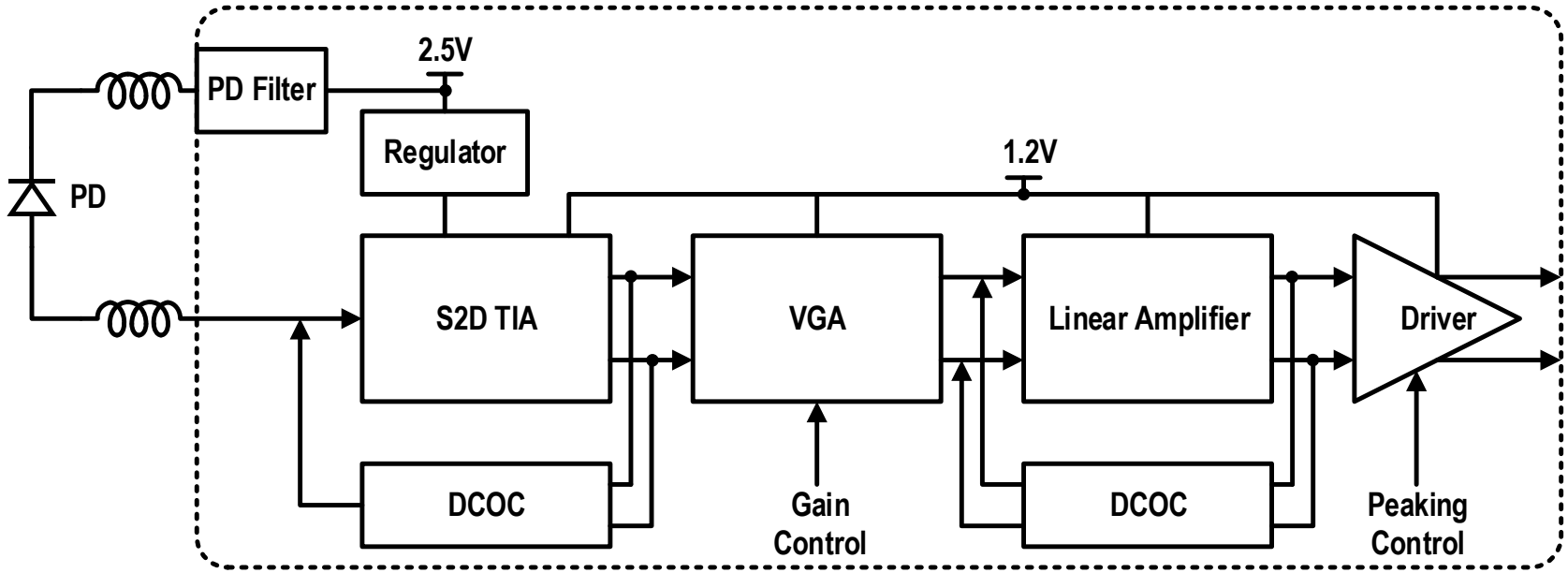
CMOS TIAs: Challenges & Design Target



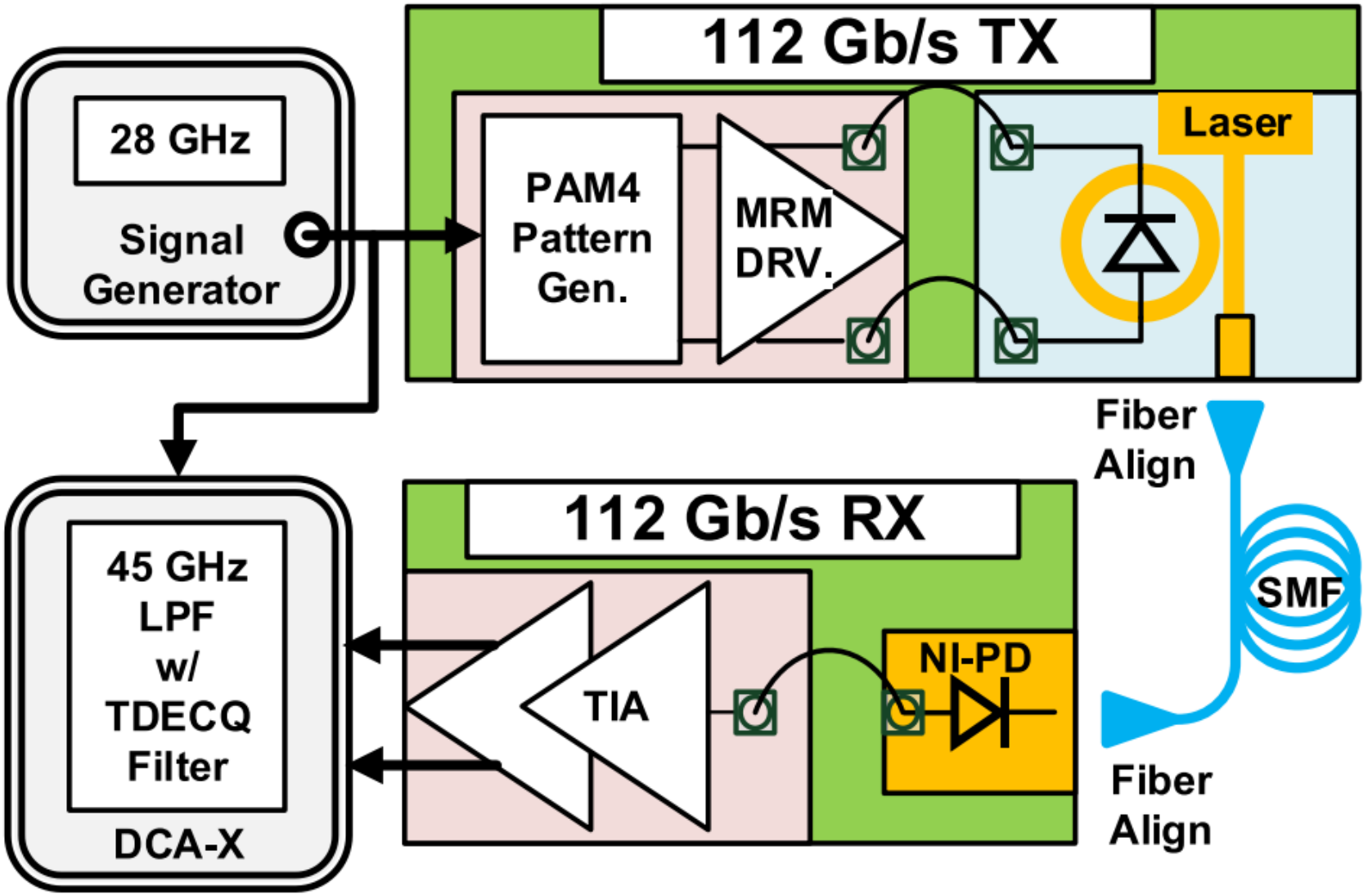
- Current 50+Gbaud TIAs are almost exclusively BiCMOS design.
- Challenge for CMOS TIAs:
  - Smaller per-stage gain => More stages.
  - More stages => lower BW, higher noise, higher distortion.
- Design goal: 28nm CMOS TIA to support 400G Ethernet standards.
  - Data rates up to 112Gb/s PAM-4 with 35GHz photodiode.
  - Input referred noise < 5μA-rms.

112Gb/s CMOS Linear TIA Architecture



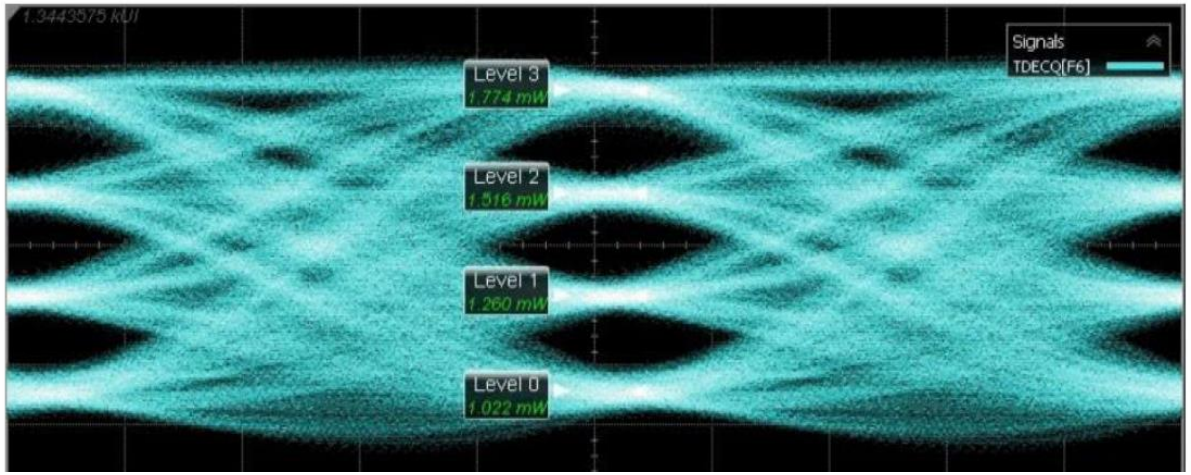
- 3 primary blocks: TIA front-end, VGA, post-amplifier.
- 2 power supplies:
  - 2.5V supply for PD bias and TIA core regulator.
  - 1.2V supply for post-amplifier to optimize power.
- Analog controls to tune gain and peaking.

112Gb/s Optical Link Test Setup



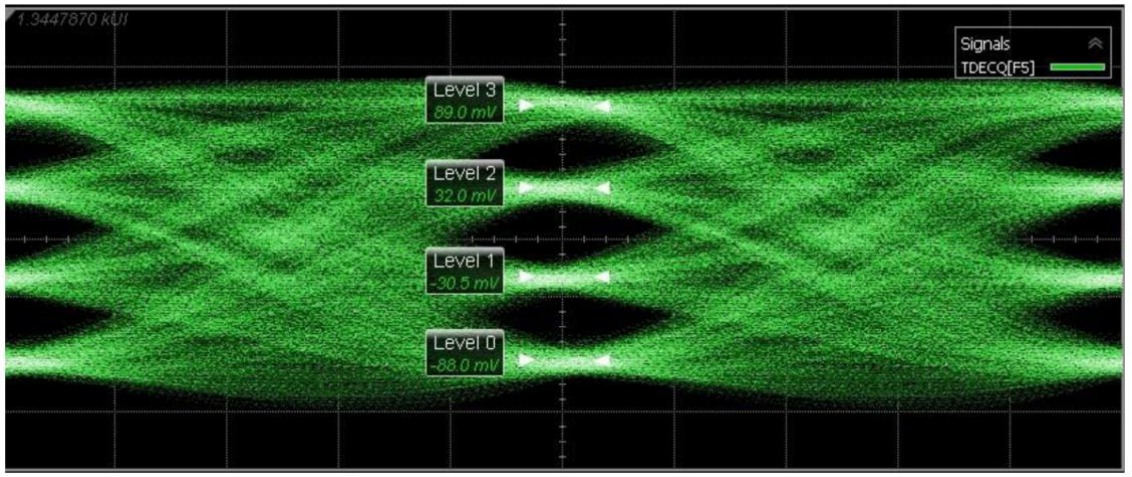
112Gb/s PAM-4 Optical Link Measurement

112Gb/s PAM-4 TX Optical Eye
from Optical Oscilloscope



TDECQ = 0.5dB

112Gb/s PAM-4 RX Electrical Eye
from TIA Output



TDECQ = 0.86dB

- Only 0.36dB TDECQ penalty measured from the full-link demo compared with TX-only reference measurement.

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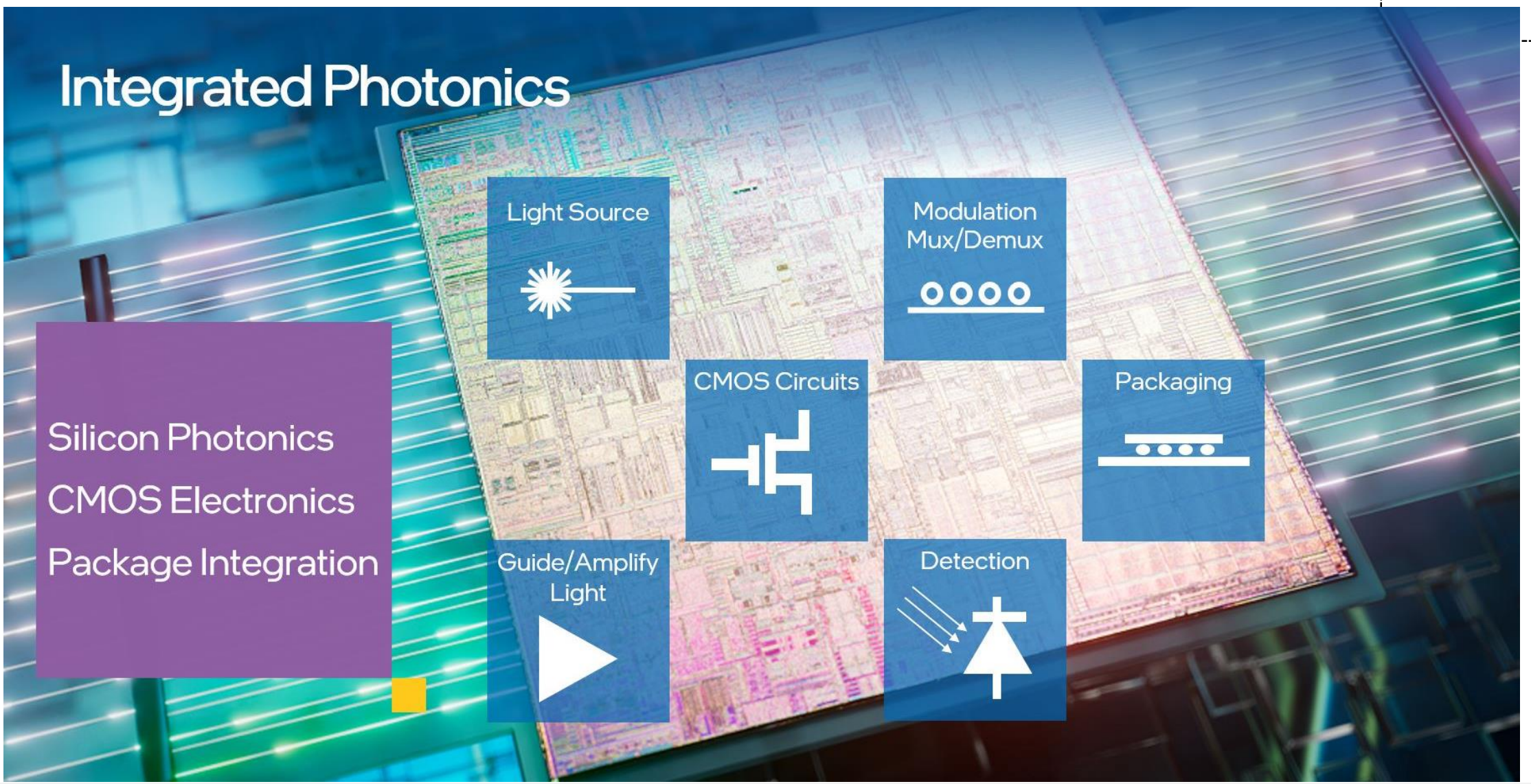
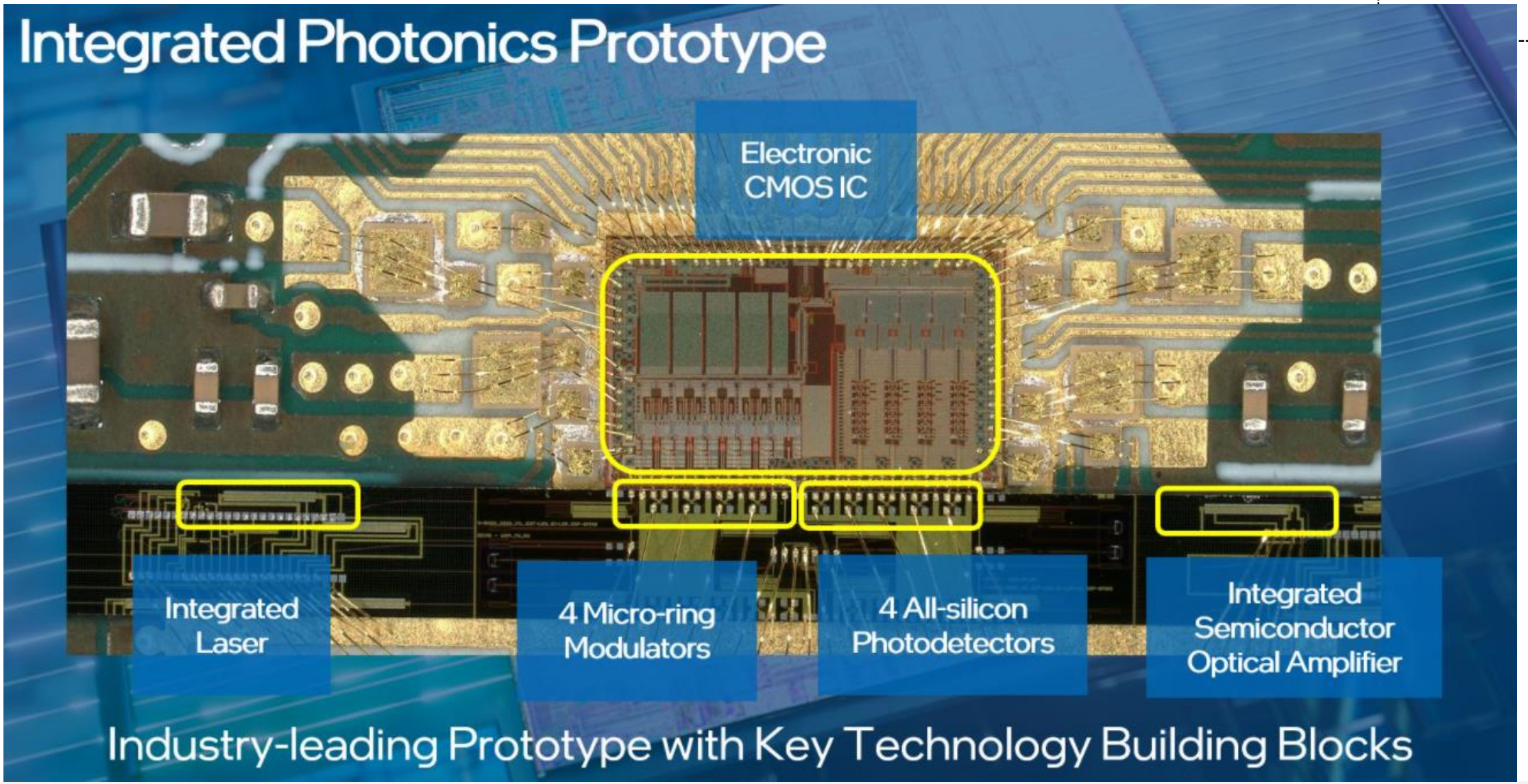
- Conclusions

Integrated Photonics



Putting Everything Together



Outline

- Co-Packaged Silicon Photonics
- 3-D Integrated 112Gb/s MRM Transmitter
  - Nonlinear PAM-4 equalization
  - Integrated thermal control
- 112Gb/s CMOS TIA for Co-Packaged Optics
- Fully-Integrated Silicon Photonics Transceiver System
- **Conclusions**

Conclusions

- **Co-Packaged Optics is essential for future data centers.**
- **First 3D-integrated 112Gb/s PAM-4 MRM-based transmitter with integrated laser.**
  - **0.88dB** TDECQ by enabling driver nonlinear PAM-4 equalization.
  - **<1.5dB** TDECQ over 27°C with closed-loop thermal control.
  - **Highest** data rate reported over comparable solutions.
- **First 112Gb/s MRM-based optical link with low-power PAM-4 CMOS linear TIA.**
  - **Highest CMOS TIA BW** reported. **>40GHz** S21 BW, **60GHz** ZT BW.
  - **0.96pJ/bit** energy efficiency.
- **Demonstrated a compelling path to pursue fully-integrated photonics solution for future Terabit optical links.**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