High-Speed Multilevel Coded Modulation and Soft Performance Monitoring in Optical Communications

Tsuyoshi Yoshida[1], Isamu Kudo[1], Kenji Ishii[1], Hideo Yoshida[1], Hidenori Shimizu[1], Susumu Hirano[1], Yoshiaki Konishi[1], Magnus Karlsson[2], and Erik Agrell[2]

[1] *Information Technology R&D Center, Mitsubishi Electric Corporation, Kamakura, Japan*

[2] *Fiber-Optic Communications Research Center, Chalmers University of Technology, Gothenburg, Sweden*

Yoshida.Tsuyoshi@ah.MitsubishiElectric.co.jp

Abstract: We implemented and evaluated probabilistically-shaped multilevel coded modulation and soft-information based performance monitoring at throughputs from 200 Gb/s to 1.2 Tb/s for multi-haul fiber-optic communications. Error-free operations were observed in 5- to 128-ary modulation formats. © 2024 The Author(s)

1. Introduction

The importance of information and communications infrastructure is evolving with emerging data-driven applications such as generative artificial intelligence. On the other hand, the power consumption of the infrastructure can be a big issue in the near future. Since optical communications are handling huge amounts of data traffic, their energy efficiency must be continuously improved. Reducing the number of physical optical transceivers and the power consumption in each physical optical transceiver can be key enablers. The first enabler means to increase the maximum throughput per optical wavelength channel by increasing the maximum baudrate and the modulation order, which highly depends on the advancement of analog opto-electronic devices performance [1]. The second enabler can be divided into two aspects, where one is low-power operation; choosing the highest spectral efficiency with a bare minimum system margin [2], realized by highly granular spectral efficiency and live performance monitoring. The other is the low-power implementation for supporting various spectral efficiencies. Here, we address those two aspects in the second key using coding, performance monitoring, and their high-speed implementation and evaluation.

A highly granular spectral efficiency is realized by digital signal processing (DSP) aided coherent communications [3] with coded modulation, including forward error correction (FEC) [4–6] and probabilistic constellation shaping (PCS) [7,8] as implemented in [9]. The combination of multilevel coding (MLC) and multi-stage decoding is beneficial to support various modulation orders at low power consumption [10–16] by protecting some bits with high-performance soft-decision (SD) FEC [6] and all bits with low-power hard-decision (HD) FEC [5].

In this work, we implemented multilevel coded modulation [14,15] with the energy-efficient and highly granular PCS method described in [17] and the low-complexity live performance monitoring based on the histogram of the SD-FEC decoder input used in [18], useful for maintaining the system margin. The rest of the paper summarizes the high-speed implementation and the experimental evaluation of the coded modulation and performance monitoring.

2. Implemented coded modulation and performance monitoring

We implemented coded modulation for multi-haul fiber-optic communications at throughputs of 200 Gb/s or higher with various modulation formats having constellation sizes from 4 to 256. Fig. 1 shows the block diagrams for (a) the encoder and (b) the decoder, respectively.

At the encoder, the PCS encoder based on hierarchical distribution matching [17] converts source bits into shaped bit labels representing channel-input multi-dimensional quadrature amplitude modulation (QAM) symbols with PCS, where a portion of the sign bits is reserved for FEC redundant bits generated later. The FEC encoder regards a block of bits from the PCS encoder as information bits and encodes them depending on the assignment of bit level to set-partitioned pulse amplitude modulation (PAM) symbols. We employed two types of MLC schemes [14,15], where all information bits are protected by low-power HD-FEC and the information bits, placed at the least significant bit (LSB) level, that select constellation subsets are protected by strong SD-FEC. The frame structures of the MLC schemes for (a) high- and (b) low-order QAM are shown in Fig. 2. The redundant bits are assigned to sign bits, placed at the most significant bit (MSB) level, of PAM symbols in the case of Fig. 2(a) [14], while those are carried by other symbols in the case of Fig. 2(b), termed sparse-dense MLC [15]. The generated bits from the FEC encoder are converted to symbols used for channel input.

At the decoder, channel-output symbols are demapped to bits with reliability for the SD-FEC decoding and bit candidates for the HD-FEC decoding. The bits before HD-FEC decoding are recovered based on the set-partitioned bits from the SD-FEC decoder. Then, the HD-FEC decoder recovers the FEC information bits, and the PCS decoder recovers the source bits. Note that the FEC coding employs set partitioning for the multistage decoding while the

symbol mapping rule should be designed to reduce the Hamming distance between nearest neighboring points for better performance before the FEC decoding. Thus, we introduced binary reflected labelling for PAM symbols carrying the SD-FEC redundant bits. This binary reflection can be realized by the exclusive OR operation (XOR) shown in Figs. 1(a) and 1(b).

The performance in these MLC systems can mostly be defined by the SD-FEC decoder input. As in conventional systems, the SD-FEC decoder is equipped with a bit-flipping counter for estimating the BER at the SD-FEC decoder input (i.e., logarithmic ratio of *a posteriori* probabilities, L-values). We also implemented a histogram monitor (H-mon. in Fig. 1(b)) of reliability information, i.e., quantized absolute amplitudes of the SD-FEC decoder input. Based on the histogram, the soft information metric of asymmetric information is estimated. The detailed process can be found in [18]. The estimated BER and the estimated soft information can be converted to hard and soft Q-factors ($\Delta\hat{Q}_{\mathrm{hard}}$ and $\Delta\hat{Q}_{\mathrm{soft}}$), respectively [19].

In the case of 800 Gb/s MLC 64-QAM at the FEC threshold, the percentages of the power consumption in the MLC circuitry were 43%, 6%, 24%, and 18% for the SD-FEC decoder, HD-FEC decoder, symbol demapping, and PCS encoder/decoder, respectively. The others were less than 9% together and 5% in each block, including the HD-FEC encoder, XOR, HD, SD-FEC encoder, and interleaver/deinterleaver (not explicitly shown in Fig. 1 (a)).

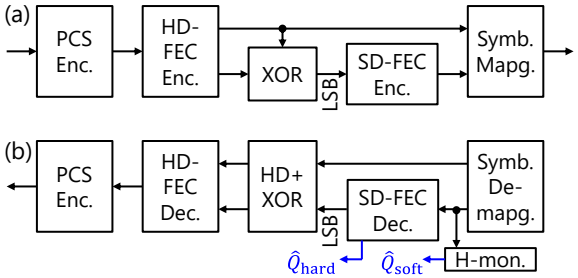

Fig. 1. Block diagrams of implemented MLC circuitry: (a) encoder and (b) decoder.

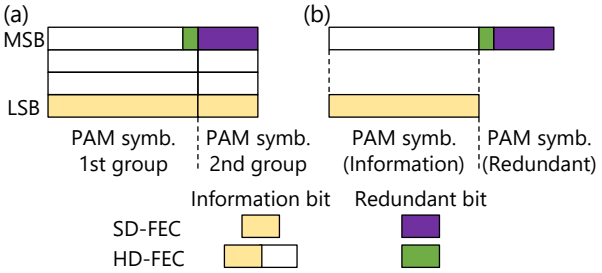

Fig. 2. Frame structures of the MLC schemes for (a) high-order QAM and (b) low-order QAM with sparse-dense coding.

3. Experiments

The implemented circuitry shown in the previous section was experimentally evaluated in this section. Figs. 3 and 4 show the experimental setup and the measurement results, respectively. The generated pseudo-random binary sequence (PRBS) was fed to the MLC encoder, followed by the transmitter (Tx)-side equalizer to obtain the pre-equalized sampled signals on the test chip. Through the transmission-line side interface, sampled signals at the receiver (Rx) were equalized and decoded by the MLC decoder to count the erroneous bits of the recovered PRBS.

We first performed digital noise-loading tests to examine the MLC performance and the estimation characteristics of the soft performance monitoring for efficient evaluation in various cases, reducing the influence of the variable characteristics of fiber-optic channels. Fig. 4(a) shows the experimental measurement results in the digital noise-loading tests. The inset shows relative Q-factors (ΔQ) as a function of relative signal-to-noise ratio (ΔSNR). The ΔQ is $\hat{Q}_{\mathrm{hard}}/\gamma_{\mathrm{Q}}$ or $\hat{Q}_{\mathrm{soft}}/\gamma_{\mathrm{Q}}$, where γ_{Q} denotes the Q-factor corresponding to the FEC threshold (here we define it as a value of 0.4 dB higher than the floor level of $\hat{Q}_{\mathrm{hard}}$). The ΔSNR is given by SNR/γ_{SNR}, where γ_{SNR} is the SNR at ΔQ = 0 dB for clearly showing the floor of $\hat{Q}_{\mathrm{hard}}$ for various cases. In the performance regime below the FEC threshold, while $\hat{Q}_{\mathrm{hard}}/\gamma_{\mathrm{Q}}$ (lines in the inset of Fig. 4(a)) was floored because the SD-FEC decoder input error was not fully corrected, $\hat{Q}_{\mathrm{soft}}/\gamma_{\mathrm{Q}}$ (circles in the inset of Fig. 4(a)) had no floor because the histogram could quantify the performance difference. Through the whole digital circuitry with random noise generated inside the logic, one second of error-free operations was observed in all examined formats including sparse-dense MLC 5-, 9-, and 16-QAM, and MLC 16-, 32-, 64-, 100-, and 128-QAM formats with PCS at throughputs from 200 Gb/s to 1.2 Tb/s and baud rates from 60 Gbaud to more than 100 Gbaud.

Secondly, we conducted optical back-to-back noise-loading tests for 400 Gb/s MLC 32-QAM with PCS. The sampled signals from the digital circuitry were converted to analog electrical signals via digital-to-analog converters (DACs). The continuous lightwave from the micro-integrated tunable laser assembly (ITLA) was modulated by the electrical signals in

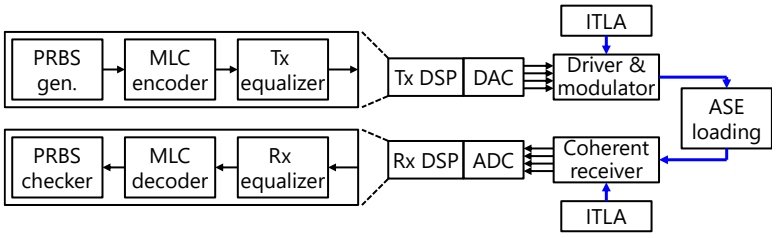

Fig. 3. Experimental setup.

driver and modulator to generate polarization-division multiplexed QAM signal. The examined wavelength and each linewidth were 1550.166 nm and 100 kHz, respectively. Amplified spontaneous emission (ASE) noise was loaded to the optically modulated signal and the optical SNR was swept. The integrated coherent receiver mixed the received and the local oscillator lights and performed balanced detection. The four-lane electrical signals were sampled in analog-to-digital converters (ADCs) at more than 100 Gsample/s and processed in the digital circuitry including timing and frame synchronization from the received signal. Fig. 4(b) shows the experimental results under the optical noise-loading tests, where error-free operation was observed during one minute in the high-SNR regime. While the estimated relative hard Q-factor $\hat{Q}_{\mathrm{hard}}/\gamma_{\mathrm{Q}}$ was floored below the FEC threshold (around SNR = 15 dB in Fig. 4(b)), the soft one $\hat{Q}_{\mathrm{soft}}/\gamma_{\mathrm{Q}}$ well corresponded to the optical SNR. In this second test, soft Q-factors showed larger values than the hard Q-factors by up to 0.9 dB due to different channel characteristics compared with the digital noise-loading tests, which needs further analysis.

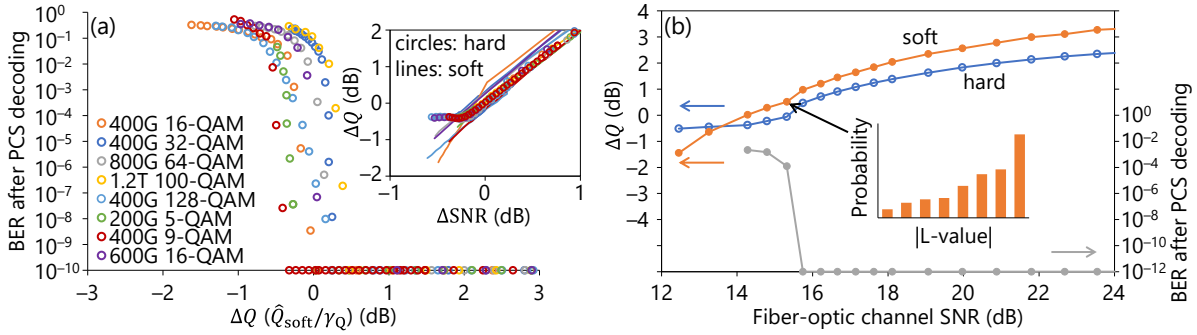

Fig. 4. Experimental results of Q-factors and BER after PCS decoding under (a) digital and (b) optical noise-loading tests. The inset of (a) shows relative estimated soft and hard Q-factors as functions of the relative SNR. The inset of (b) shows an example of the L-value histogram. Markers at the bottom of the figures indicate error-free operation during the measurement.

4. Conclusions

Two MLC schemes with granular PCS were implemented and experimentally evaluated at high throughputs under digital and optical noise-loading tests. Error-free operation was experimentally demonstrated for all examined formats. As live performance monitoring, the Q-factor based on the soft information with the implemented histogram monitor worked well below and above the FEC threshold, while the hard Q-factor based on the bit-flipping ratio in the FEC decoder was incorrect below the FEC threshold.

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