Comparison of FEC Design Concepts for Higher Error Correction Performance with Utilizing Turbo Product Code

Yohei Koganei, Kiichi Sugitani
Fujitsu Ltd., 4-1-1Kamikodanaka, Nakahara-ku, Kawasaki, 211-8588, Japan
koganei.yohei@fujitsu.com

Abstract: We investigate several FEC design concepts to enhance a turbo product code with higher overhead ratios. The result illustrates which concept would be effective to obtain higher performance according to the increase of the overhead. © 2024 The Author(s)

1. Introduction

Turbo product codes (TPC) [1] are forward error correction (FEC) codes, specifically belonging to the category of soft-decision (SD) FEC. TPCs can generate powerful error correction performance with a relatively low redundancy ratio, or FEC overhead. Such characteristic often suits the demands of high-speed optical communication systems with digital coherent technology. Particularly, Open FEC (OFEC) realizes a practical SD-FEC code which achieves the net coding gain of 11.6 dB for 16-QAM with about 15.3% FEC overhead [2].

The code structure of a TPC is typically based on a two-dimensional array of bits, made of orthogonally interleaved codewords of block codes. Practically, the Bose–Chaudhuri–Hocquenghem (BCH) codes are often chosen as the component codes. Although BCH codes belongs to the category of hard-decision (HD) FEC in the first place, they behave as SD-FEC in a TPC decoder by performing Chase decoding [3]. Soft bits, the soft-decisioned data indicating the reliability of bits, are iteratively processed in a loop of soft-in soft-out (SISO) decoding. The detail of decoding strategy has a significant impact on the error correction performance of a TPC. In [4], the effect of various parameters in the decoding is rigorously investigated using a OFEC compatible decoder.

The performance is also affected by parameters of code design for a TPC, for example, changing the code length, the minimum distance, or the order of Galois Field (GF) of the component BCH code. Applying such modifications lead to a TPC which is not compatible with the original one because the bit mapping in the code structure, besides the FEC overhead, is also changed. Nevertheless, there may be a situation that requires a higher error correction performance by modifying a TPC with allowing to have a higher FEC overhead.

In this paper, we compare the effectiveness of four concepts of FEC designing with a TPC. The four concepts we are going to investigate are: 1. Shortening message bits of the component codes, 2. Increasing the minimum distance of the component codes, 3. Lowering the order of Galois field used in the BCH codes, and 4. Concatenating an LDPC code as the inner code of the TPC. The aim is to obtain higher error correction performance while utilizing an existing model of a TPC which is originally designed for about 15% of the FEC overhead. Note that each concept would have different influence on the implementation complexity. The first and the fourth concept could realize customizing the overhead ratio above 15% almost continuously. On the contrary, using the second or the third concept would lead to limited overhead ratios because of the property of GFs. Besides, the first, the second, and the third method would lead to decrease the throughput of the TPC encoder and the decoder because they reduce the message bits in the unit of code structure. On the contrary, the fourth method does not change the throughput of TPC's processing.

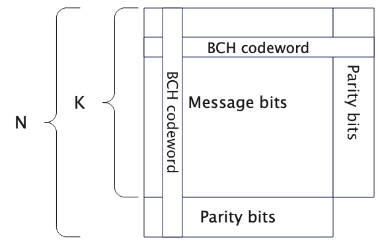
2. Comparison of FEC design concepts with a TPC

We firstly made a pair of TPC encoder and decoder as base models to be used in the evaluation the effectiveness of the four concepts by numerical simulations. The TPC is made of a single BCH code as its component code. The parameters of the BCH code of the base model are listed in the first row of the left part of Table 1, which can correct up to 2 bits in a codeword with the length of 254 bits. One extra parity bit is added in each codeword to reduce wrong corrections. We aimed that the base model to have a near error correction performance of OFEC, but not the same for convenience of our simulations. Other rows in the table defines configurations of the TPC modified from the base models. The values of the parameters were chosen according to the FEC design concepts we are going to evaluate. We considered those configurations to be realistic to some extent for optical communication. For example, those parameters are chosen theoretically not to cause the error floor above bit error ratio (BER) of 10^{-15}. For all the configurations, the TPC decoder commonly performs the Chase decoding with up to 3 flips in 6 least reliable bits in a BCH codeword. The soft-bits processed in the decoder is quantized to 4-bit granularity. A set of SISO iteration is performed three times. We did not attach HD iterations after the SISO iteration because we assumed that would not affect the evaluation by using numerical simulations.

Table 1. Parameters of FEC designs.

Concept of code design	BCH's Code-length (N)	BCH's Message length (K)	BCH's Correction bits (T)	BCH's Order of GF	TPC's Overhead [%]
Base model	254	237	2	8	15.5
(1) Shortening Message bits	224	**207**	2	8	17.9
	194	**177**	2	8	21.3
	144	**127**	2	8	31.0
	114	**97**	2	8	42.5
(2) Increasing Correction bits	254	229	**3**	8	24.5
	254	221	**4**	8	35.1
	254	213	**5**	8	47.7
(3) Lowering Order of GF	126	111	2	**7**	31.3
	63	*50*	*2*	*6*	*70.3*

Concept of code design	LDPC's Codelength	LDPC's Message length	LDPC's Overhead [%]	Overhead with TPC [%]
(4) Concatenating LDPC code	4320	4064	6.3	22.7
	4576	4064	12.6	30.0
	4832	4064	18.9	37.3
	5088	4064	25.2	44.6



Code structure of a TPC (Simplified image)

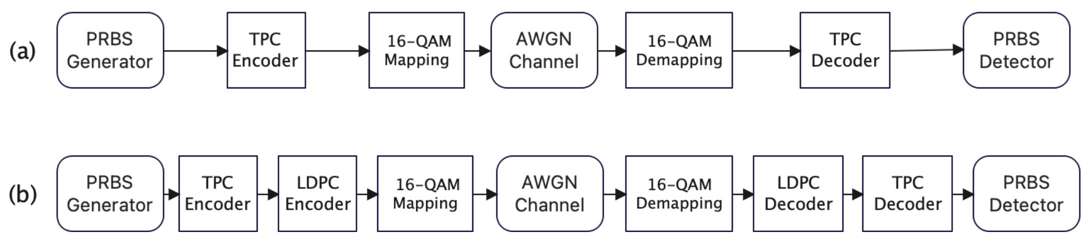


Fig. 1. Block diagrams of numerical simulations.

Figure 1 shows the block diagram of the simulations, in which a pseudo-random bit sequence (PRBS) is commonly used as the message bits. An AWGN channel with 16-QAM is commonly used as the channel model. For the first three concepts, as depicted in Fig. 1-(a), the message bits are processed by the TPC encoder and mapped into constellation points before entering through the channel model. After the channel noise is added, log-likely-ratios (LLRs) are calculated from coordinate values of the channel output by a demapping block and then processed by the TPC decoder for error correction. The LLRs are quantized to 4-bit granularity to be the same as that of the soft-bits in the TPC decoder.

For the fourth method, we made a pair of LDPC encoder and decoder models to be concatenated to the base model of the TPC. The LDPC codes used for the evaluation were designed to be irregular ones [5] with code lengths listed in the right part of Table 1. The difference of the block diagram from other concepts is that, as depicted in Fig. 1-(b), the LDPC encoder is inserted between the TPC encoder and the constellation mapping block, and an LDPC decoder is inserted between the de-mapping block and the TPC decoder. We set a limit for the LDPC decoder's iterations up to 30, without much consideration though. Although LDPC decoders usually output hard-decisioned values of LLRs after the iterative decoding, the LDPC decoder in this case outputs LLRs without hard-decisions because those LLRs can directly be the input of the TPC decoder. The quantization of LLRs for the LDPC decoder is in 4-bit to be the same granularity as the TPC decoder.

3. Simulation results for BER performance

Figure 2-(1) shows the result for the first FEC design concept, that is changing the message length (K) of the component BCH code in the TPC. The BER performance of the decoded bits against signal to the noise ratio (SNR measured as E_s/N_0) of the channel was improved by shortening the message length. Figure 2-(2) is the result of the second concept, that changes the number of maximum correction bits (T) or the minimum distance of the component BCH code in the TPC, showing the BER performance improves as T increases. Figure 2-(3) is the result of the third

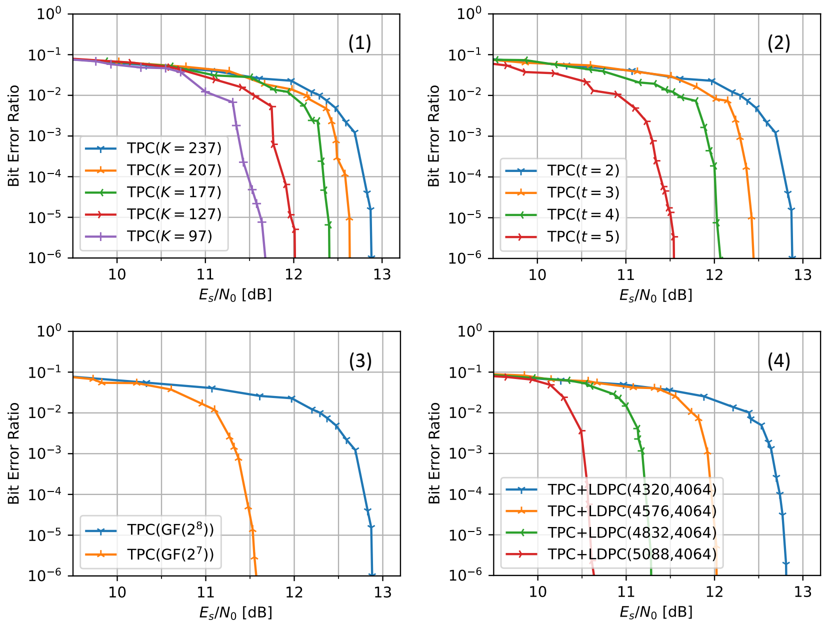


Fig. 2. BER performance of the four FEC design concepts.

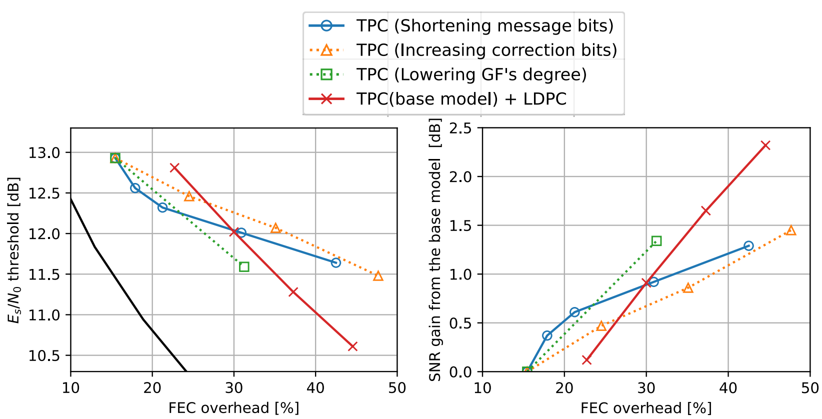


Fig. 3. Comparison of the four FEC design concepts.

concept, showing the BER performance improved by reducing the order of Galois Field (GF) from 8 to 7. We omitted the configuration of GF(2^6) from the evaluation because the overhead becomes too high with that order. Figure 2-(4) shows the result of fourth concept, in that the base model of the TPC is concatenated by an LDPC code with changing its parity bit length. It is shown that the BER performance improved as the code length of the LDPC codes grows, that was associated with increasing the number of parity bits.

We summarized the results of Fig. 2 into the left part of Fig. 3 to show the relationship between the threshold of E_s/N_0 at BER of 10^{-6} and the FEC overhead ratio. The same data is shown in the right part of Fig. 3 with a different manner to illustrate the improvement of the SNR threshold from the base model of the TPC. It is seen that the method of shortening the message length was efficient for a range of overhead ratios relatively near to the base model, but its efficiency decreased for 30% or higher overhead ratios. Compared to that, the way of increasing the correction bits was less effective for all the range of FEC overhead. Lowering the order of GF was the most effective at the limited overhead ratio where the code design is possible. That suggests combining the first and the third method may be effective for the range of higher overhead ratios, in this case, for over 30%. Concatenating an LDPC code was the least efficient for lower range of the overhead, but it was the most efficient for the higher range of the overhead. Such rapid change of the performance suggests that there might be a room for the code optimization on the concatenated LDPC codes, but at least this method could be useful for enhancing the performance of an existing TPC with additional overhead.

4. Conclusion

We investigated four FEC design concepts to enhance the error correction performance of a TPC, allowing to have higher overhead ratios. Shortening method was efficient for relatively small increase of the overhead. For a large increase of the overhead, lowering the order of GF with combining the shortening may be efficient for the error correction performance but with decreasing the throughput of the TPC. Concatenating an LDPC code to a TPC could be also effective for relatively a large increase of the overhead, without decreasing the thruput of the TPC.

5. References

[1] Mukhtar, et al., IEEE commun. Surv. Tutor, vol. 18, No. 4, 2016.
[2] 20181217a Open-ROADM-MSA-specification-ver-3-00.
[3] D. Chase, IEEE Trans. Inf. Theory, vol. IT-18, no.1, pp.170-182, 1972.
[4] Weiming Wang, et al., OFC2022, W3H.1, 2022.
[5] A. Roumy, et al., IEEE trans. Inform. Theory, vol.50, no. 8, pp. 1711-1727, 2004.