Improving FFE Performance by an Error Decorrelation Algorithm

Nebojša Stojanović, Stefano Calabrò, Lin Youxi, Tom Jonas Wettlin, Talha Rahman, and Maxim Kuschnerov
Huawei Technologies Duesseldorf GmbH, Germany Research Center, Riesstrasse 25, D-80992 Munich, Germany.
e-mail: nebojsa.stojanovic@huawei.com

Abstract: Two error decorrelation algorithms with negligible complexity and latency are developed to improve noise statistics after feed-forward equalizers. Performance improvement is demonstrated in simulations and experiments. © 2023 The Author(s)

1. Introduction

Data center (DC) connections require sophisticated switch architectures, the design of high-bandwidth electrical and optical components, and advanced integration. Currently, intensity-modulation and direct-detection (IMDD) using either two- or four-level pulse amplitude modulation (PAM2, PAM4) is utilized in DC links. Beyond 50 Gbaud IMDD optical transceivers will rely on new forward error correction (FEC) schemes [1], probably use advanced modulation formats (e.g. discrete multitone or digital subcarrier multiplexing) and equalization techniques [2], deploy optical amplifiers, avoid optical digital signal processing (DSP) in transceivers (co-packaged and linear drive pluggable optics) [3], etc. Next advanced generation of DC transceivers will likely carry 3.2T data, and because of severe bandwidth limitations, coherent techniques and IMDD PAM6/PAM8 modulation formats may be considered for rates above 200Gbit/s/lane.

A few-tap linear feed-forward equalizer (FFE) is usually implemented in IMDD DC transceivers to cope with inter-symbol interference (ISI). A few nonlinear FFE taps (Volterra equalizer) may significantly improve performance when components nonlinearities become critical. Likely at higher bit rates, advanced DSP algorithms such as decision feedback equalizer (DFE) or maximum likelihood sequence estimation (MLSE) (suffering from complexity and latency) will play more important roles. In this paper, we propose an algorithm having negligible latency and outperforming DFE equalizers by using only one multiplier and two adders per symbol. Superior performance is demonstrated in simulations and experiments.

2. FFE Error Decorrelation Algorithm

Most communication systems have a low-pass characteristic that can be approximated by a 1+aD function, where D is a delay of one symbol interval and a is a value between 0 and 1. Therefore, the noise after a full-response FFE has a shape ~1/(1+aD) with additive Gaussian noise at the FFE input. The FFE introduces noise enhancement that is avoided by the DFE. In high-speed optical systems, the ASIC works at much lower speed than the symbol rate so that hundreds of symbols are processed in parallel. To solve the feedback loop in parallel DFE equalizers, sophisticated algorithms as lookahead techniques are required [4] which seriously increase complexity and latency. Let us consider the FFE with an error e_k=d_k-y_k at symbol period k, where y_k is the FFE output and d_k is the decision. The error correlation factor α can be found by $\alpha = E[e_k e_{k-1}]/E[e_k e_k]$, where E denotes the expectation [5,6]. The error decorrelation algorithm (EDA) generates improved samples z_k by

$$z_k = y_k + \beta_A e_{k-1} + \beta_B e_{k+1},$$

where parameters β_A and β_A should be optimized. To simplify parameters optimization, we introduce two simple EDA variants

$$\text{EDA1: } z_k = y_k - \alpha e_{k-1}$$

$$\text{EDA2: } z_k = y_k - \alpha(e_{k-1} + e_{k+1})/2.$$

The parameter α is identical to the DFE feedback coefficient (1-tap DFE) and the first EDA variant (EDA1) provides similar performance as the 1-tap DFE over "mild" ISI channels (a<0.4). The second variant (EDA2) uses the errors from both neighbors to improve performance. In general, the EDA2 variant outperforms both the DFE and EDA1 for practical a value (a<0.5). Compared to the FFE, the EDA2 requires two additions and single multiplication per symbol (which can be done in a single ASIC clock) while α estimation can be done at very low speed with negligible DSP

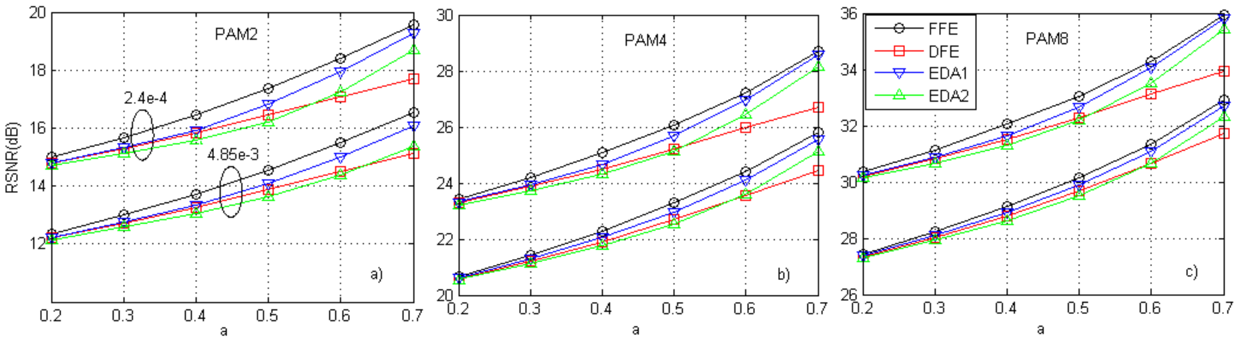

Fig. 1. Required SNR. a) PAM2, b) PAM4, c) PAM8.

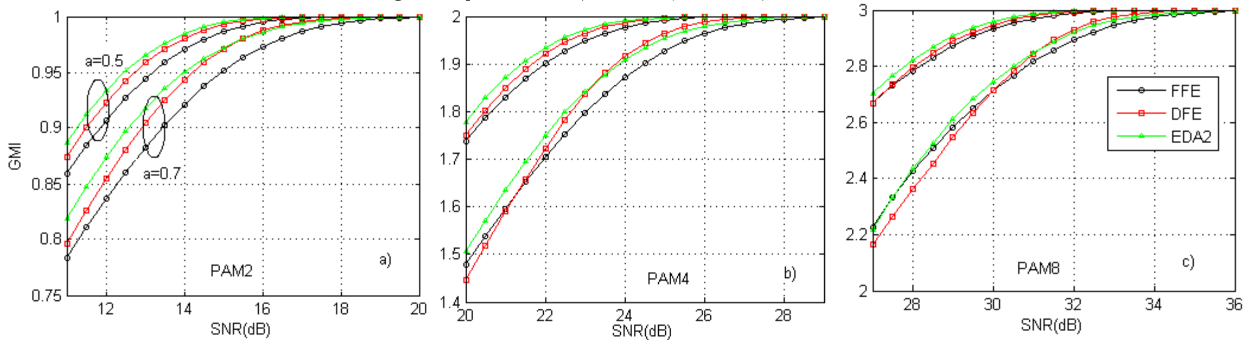

Fig. 2. GMI for *a* value 0.5 and 0.7. a) PAM2, b) PAM4, c) PAM8.

complexity. The 1-tap DFE utilizes one adder and one multiplier but loop unfolding techniques are very complex and require several ASIC clock cycles, which is critical for some DC links, since high-performance computing is seriously limited by DSP latency.

3. Simulation Results

In this section, we present simulation results for 1+*a*D channels with *a* varying from 0.2 to 0.7 in steps of 0.1. A unipolar PAM signal is first distorted by ISI (1+*a*D) and later by additive Gaussian noise. The FFE block uses 5 linear taps while the DFE equalizer is realized via a single feedback tap. In practice, more FFE taps are required to compensate for near (electrical) MPI as well as short optical link reflections. In general, an FFE is necessary to correct the frequency-dependent channel group delay and the precursor ISI. Fig. 1 shows the required signal-to-noise ratio (RSNR) for two FEC thresholds (2.4e-4 and 4.85e-3) versus *a* for PAM2, PAM4, and PAM8 formats. The EDA1 behaves well for a<0.4 while the EDA2 covers the whole *a* region very well. At higher SNR values, the DFE slightly outperforms the EDA2 for *a*=0.7 while for a<0.6 the EDA2 is always the best solution. Generalized mutual information (GMI; important when soft FEC codes are considered) for *a*=0.5 and 0.7 is presented in Fig. 2. The EDA2 shows the best performance at low SNR values (no error bursts thanks to the feedforward structure) whereas the DFE generates long error bursts (which could be broken by using differential precoding) and even degrades the FFE performance for PAM4 and PAM8 formats. Improved decisions at higher SNR values for *a*=0.7 help the DFE to outperform the EDA2 in GMI and RSNR especially at the lower FEC threshold.

3. Experimental Results

To verify the EDA2 in experiments, we carried out 106 Gbaud PAM4 back-to-back (B2B) experiments with the experimental setup shown in Fig. 3 that also includes information about the bandwidth of the components. The input sequence is generated by Gray mapping a pseudorandom binary sequence to the PAM4 alphabet. The symbols are then pulse shaped using a raised-cosine filter with roll-off factor of 0.1 and downsampled to the sampling rate of the digital-to-analog converter (DAC). On the resultant symbol sequence, digital pre-distortion (DPD) is applied. The DPD filter coefficients were calculated through an indirect learning architecture [7] by comparing the received and the transmitter waveforms. The main bandwidth limitations come from the DAC and the transmitter optical subassembly (TOSA) that integrates an electrical amplifier (driver) and an electro-absorption modulated laser (EML). The O-band EML output signal is attenuated by a variable optical attenuator (VOA) and then amplified by a praseodymium-doped fiber amplifier (PDFA), which is necessary because the photo diode (PD) does not include an electrical amplifier. After resampling, timing recovery is used to remove the clock offset and find the best sampling

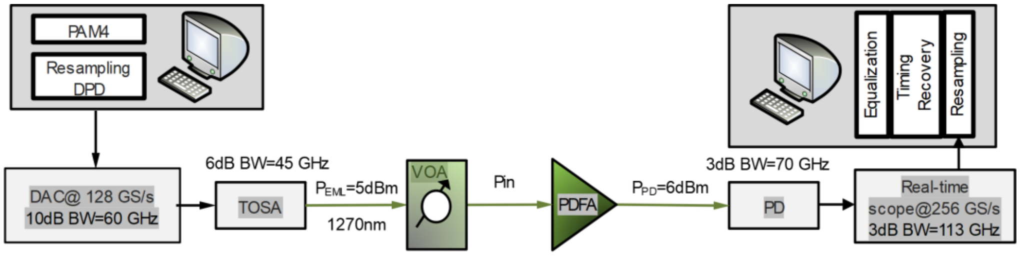

Fig. 3. 106 Gbaud PAM4 B2B experimental setup. DPD – digital predistortion, DAC – digital-to-analog converter, TOSA – transmitter optical subassembly, VOA – variable optical amplifier, PDFA – Praseodymium-doped fiber amplifier, PD – photo diode, BW – bandwidth.

phase and then the signal is down-sampled to 1 sps. The FFE consists of 41 linear taps. The performance of different equalization schemes i.e., their BER values vs input power (Pin) are shown in Fig. 4(a) for the optimum *a* value. The optimum value *a* depends on Pin e.g. at high Pin values *a* is around 0.44. The DFE includes the FFE taps and one more tap in the feedback loop. More than one feedback DFE tap did not improve performance. The DFE achieves 2 dB gain at the FEC threshold of 2.4e-4 compared to the FFE while the EDA2 outperforms the FFE by 0.4 dB. In this experiment, the EDA2 beats the DFE for each Pin value, which is consistent with our simulation results for a<0.5 (see Fig. 1(b)). The DFE and EDA2 achieve a gain over FFE of around 1 dB at BER=4.85e-3. Some additional insights can be gained by observing 2-dimensional constellations where odd and even samples are filled into two dimensions (similar to complex constellations). Fig. 4(b) compares FFE and EDA2 outputs at Pin=-4 dBm where the very noisy red FFE points are much improved by the EDA2 to more confined balls around the 2D centers. Fig. 4(c) compares the DFE and EDA2. The DFE shows some excursions that are reduced in the EDA2 case. All balls around 2D centers are pretty regular/round (not elliptical), however, the appearance might change at other (especially at lower) Pin values and different sampling phases. More elliptical/irregular balls indicate more residual correlation.

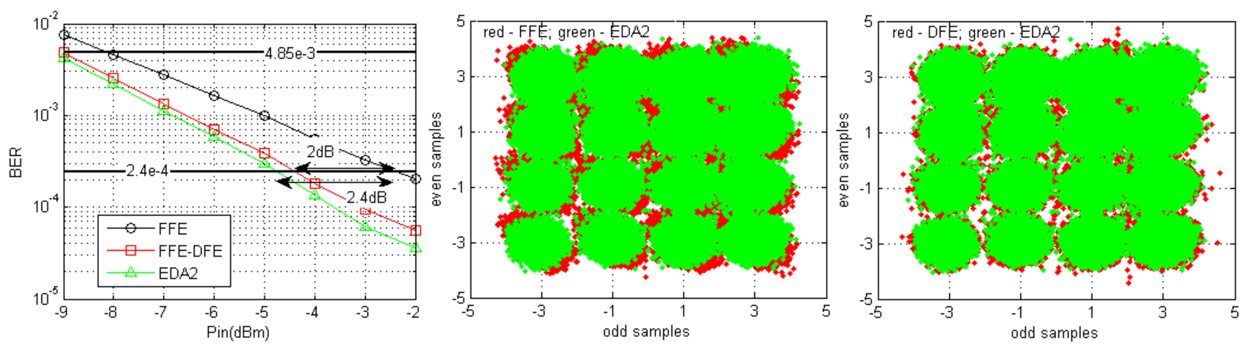

Fig. 4. PAM4 experimental results. a) BER vs Pin, b) 2D FFE-EDA2 constellation, b) 2D DFE-EDA2 constellation.

4. Conclusion

We introduced the EDA algorithm, which improves noise statistics after the FFE and achieves similar performance as the DFE. Excellent performance is demonstrated in simulations and experiments for channels with moderate ISI. Low latency and low complexity make the EDA algorithm a good candidate for next-generation DCN receivers.

5. References

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