Breaking the interconnection limit by integrating CMOS electronics on PICs

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Abstract: We demonstrate the integration of electronic functionalities into state-of-the-art photonic platforms with zero changes to the technology. This enables time-multiplexed closed-loop control of programmable silicon photonic meshes with a reduced number of electrical interconnections.

1. Interconnection limits in advanced PICs

Programmable photonic integrated circuits (PICs) are constantly increasing their complexity to keep up with the scaling requirements of emerging applications like optical communication, optical computing and quantum optics [1]. The functionality of programmable PICs, typically implemented as a mesh of Mach-Zehnder interferometers (MZI) and/or ring resonators, needs to be precisely controlled at run-time to define the overall chip behavior. A multitude of sensors and actuators connected to external electronic circuitry is thus needed for tuning the working point of each elementary building block (BB), as well as for stabilizing it against thermal or process-dependent drifts. As the number of BBs increases, the quantity of interconnections towards the control electronics also increases. Since the maximum practical number of bonding pads is in the order of few hundreds, merging electronics with photonics becomes imperative not to be limited by this issue.

We have followed the path of integrating CMOS electronics into Silicon Photonic platforms (Figure 1a) without modifying the technological steps already available in the production of state-of-art photonic devices [2]. This zero-change approach reflects into zero additional costs and high interoperability of the designed circuitry among foundries.

2. Monolithic CMOS electronics embedded in PICs

2.1. Side-wall CMOS transistors and analog/digital circuits

Lateral p- and n-MOSFET have been implemented on the side wall of the same silicon layer used for waveguides in standard SOI 220 nm technologies, as shown in Figure 1b. By opening a vertical trench in this layer, a side gate is created as close as possible to the transistor channel, resulting in a threshold voltage of about 1.5 V. The SOI thickness defines the width of the channel. The body of the transistor is locally doped (10^{17} cm^{-3}) to create the Drain (D) and Source (S) contacts. Numerical simulations were used to optimize the channel length $L = 4\,\mu$m and to achieve low leakage currents in the OFF state without significantly diminishing the device conductivity. The

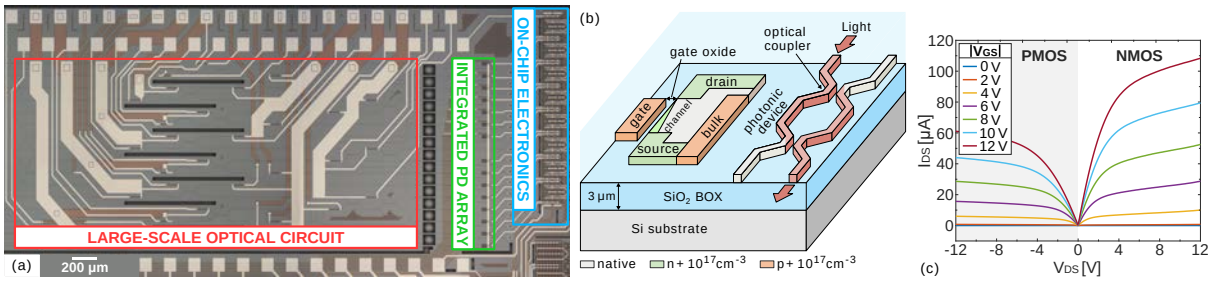

Fig. 1. (a) Microscope photograph of a programmable Silicon Photonic chip integrating zero-change monolithic electronics. (b) 3D sketch of MOSFET realization on the same silicon layer as the waveguides. (c) Measured characteristic curves of the fabricated p- and n-MOSFETS.

measured characteristic curves for nMOS and pMOS devices are shown in Figure 1c. Multiple transistor cells can be connected in series or parallel to achieve the desired electrical characteristics.

The proposed approach is technologically transparent, as transistors are produced without altering the manufacturing process and the design rules of the photonic stack. The most important parameter required by transistors is the width of the gate trench, set to 200 nm in our design. This value is slightly larger than the minimum needed to design directional couplers, gratings and other key optical elements, and it is thus guaranteed by most silicon photonics foundries. Our chip was fabricated by Advanced Micro Foundry, Singapore [3]. Technologies allowing for smaller trenches would result in better transistors, with a lower threshold voltage.

CMOS logic gates have been designed in this unusual technology (2a). They maintain their regenerative properties and can be connected in cascade without penalty to implement the desired logical function to support the operation of the photonic layer. User-selectable connection of the sensors/actuators on the photonic chip to the external readout/driving electronics can be provided by bidirectional analog switches, obtained by combining two pass transistors controlled with complementary gate voltages in a single-pole double-throw scheme (SPDT, Figure 2b). We used 16 transistors connected in parallel to lower the ON resistance of each switch to about 1.8 kΩ with a current handling of around 1 mA. Good insulation of the switch in the OFF state is ensured by a leakage below 5 nA even for high drain-source voltages. The OFF resistance results to be approximately 2 GΩ, demonstrating that the device correctly connects and disconnects the inputs to the outputs depending on the digital control. The signal bandwidth of the switches shows a cutoff frequency of approximately 100 MHz, well within typical frequencies (max few MHz) required in the control of photonic circuits.

2.2. *Multiplexed sensors readout and actuators driving*

Figure 2c highlights a possible application enabled by embedding basic electronic features into a programmable PIC [4]. The core of the photonic circuit is a binary mesh (at the center in the figure) of 15 MZI. The mesh has to be feedback-controlled to drive the light power coming from the 16 input grating couplers toward the single output port of the mesh. The tuning of each MZI is obtained by constantly monitoring its drop port with a photodiode (PD) and by properly operating the integrated heater to drive the PD current to zero.

The on-chip circuitry, a 16:1 multiplexer (MUX), is shown in the right side of the figure. The MUX sequentially accesses the 15 on-chip Germanium PDs and routes their signals toward a single readout circuit using only one bonding pad. The MUX has been made of SPDT switches that connect the selected PD to the virtual ground of an external transimpedance amplifier and the other PDs to ground, ensuring that all detectors are always biased at the same operating voltage, thus minimizing the switching time (about 500 ns).

Similarly, the heaters of each MZI have been driven in a sequential way through a 1:16 demultiplexer (DEMUX), to further reduce the number of interconnections by an additional factor of 16. Being thermal heaters volatile, i.e. they require a continuous bias for their operation, an analog electronic memory has been also inte-

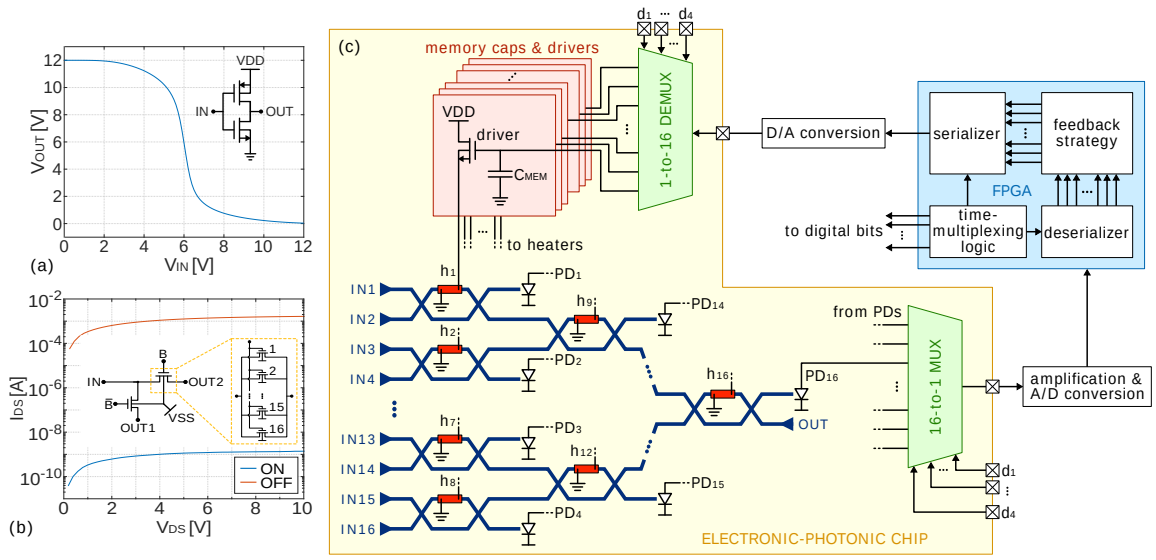

Fig. 2. a) Transfer function of the CMOS inverter. b) ON/OFF current of the SPDT switch. c) Schematic view of the photonic-electronic circuits integrated into the same chip, enabling a significant reduction in the number of interconnects to the external control processing logic, by a factor 16 in our realization. The pads for digital addresses of MUX and DEMUX are also indicated.

grated into the photonic chip. This has been achieved by designing a Sample&Hold (S&H) circuit at the gates of the heater drivers, needed to provide sufficient current to the actuators. The S&H exploits the switches of the DEMUX and a bank of memory capacitors of about 10 pF, obtained by interleaving the metal layers available in the technology. The obtained hold time, limited by the leakage current of the switches, is around 1 s, ensuring that few thousand actuators could be multiplexed without penalties if needed.

3. Time-multiplexed control of programmable silicon photonic circuits

The performance of the electronic-photonic single-chip system is summarized in Figure 3. Figure 3a shows the bit-error-rate (BER) when routing a 10 Gbit/s on-off keying (OOK) signal through the photonic chip, controlled by sequentially reading the integrated PDs with the MUX. Each BER point has been acquired for 4 minutes, for an overall experiment duration of about 3 hours. The measurement shows no relevant degradation with respect to the back-to-back case, certifying that the time-multiplexed readout does not worsen the control of the chip.

Figure 3b reports the performance of the sequential operation of volatile actuators with the on-chip electronic memory. When the refresh period of each heater is between 100 µs and 100 ms, the transmitted optical power remains almost constant. When the switching is faster, the MZI response is dominated by the time constant of the heater (about 10 µs). Instead, when the refresh takes longer than 1 s the limit is determined by the memory hold time. The two refresh times of 100 ms and 10 s have been highlighted in the interference experiment shown in Figure 3c. At the input of each MZI we have an OOK modulated signal at 10 Gbit/s. The first MZI operates in cross state and is driven using the S&H circuit, while the second MZI maximizes the optical power at the OUT port. When the first MZI deviates from its working point, its input signal acts as an interference for the second MZI. The BER measured at the output when the interference is switched off approaches a value of 10^{-11}. The same value has been measured for refresh periods below 100 ms. Instead, at low frequency the S&H discharge induces a drift of the MZI bias point, increasing the interference signal power and degrading the BER. This is confirmed by the eye diagrams measured for a 10 s and 100 ms S&H refresh rate.

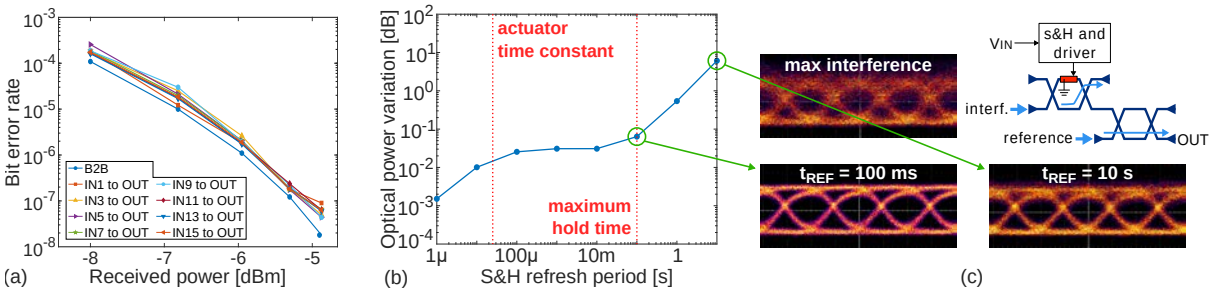

Fig. 3. a) BER measurement at the output of the 16-to-1 mesh, controlled through the readout MUX. b) Optical power variation at the output of a MZI when controlling the heater with the S&H. c) Eye diagrams at the output of the reported two-MZI structure, as a function of the S&H refresh time.

The measurements certify that sequential control of PICs enabled by proper on-chip electronics is a viable option to reduce the number of electrical lines without any optical penalty, thus targeting one of the main bottlenecks that limit further scaling of photonic circuits [5]. This approach will allow the management of future scalable systems, integrating thousands of photonic components [6].

References

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