Real-Time Demonstration of Softwarized Low-Complexity Timing Recovery by CMA Filter Interpolation for Baud-Rate Sampling DSP

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Abstract: This paper proposes a low-complexity timing recovery method and demonstrates the real-time softwarization of a baud-rate sampling DSP suite. It achieves a 38 % reduction in processing time with no penalty in sampling phase tolerance. © 2024 The Author(s)

1. Introduction

To meet fast-changing customer demands including extreme requirements, network systems, which were typically composed of dedicated hardware with long development cycles and high initial costs, have been replaced with general-purpose servers and accelerators [1]. In optical access networks, Broadband Forum (BBF) and Open Networking Foundation (ONF) are actively promoting access systems based on network function virtualization (NFV) and the software-defined network (SDN), which are named cloud central office (CO) and SDN-enabled broadband Access (SEBA), respectively [2, 3]. Both focus on shortening development cycles for new functions and expanding hardware choices in passive optical networks (PON) by abstracting differences in hardware specifications and softwarizing control and management functions. For further expansion of the software region, softwarization of dynamic bandwidth allocation (DBA) [4] and softwarization of physical coding sublayer (PCS) compliant with 10G-EPON [5] have been already demonstrated. As one of the candidates of future access technologies, softwarization of digital signal processing (DSP) functions has also been studied. While other works tried to softwarize the demodulation of high-order quadrature amplitude modulation (QAM) signals, and our works demonstrated the softwarization of carrier phase recovery (CPR) [6], frequency offset compensation (FOC) [7], and polarization demultiplexing [8], no study to date has focused on the softwarization of timing recovery. In order to softwarize DSP functions, high-throughput digital signals created by analog-to-digital converters (ADCs) must be input to servers for demodulation, e.g. 40 Gb/s server input is required for 5-GBaud quadrature phase shift keying (QPSK) signal reception using 8-bit ADC even without oversampling. To avoid increasing the computation load by oversampling, baud-rate sampling DSP is attractive for softwarization, where the constant modulus algorithm (CMA) is applied to interpolated baud-rate sampled signals yielding 2 samples with sinc filter [9]. This method has also high-computational complexity and its evaluation has been limited to offline experiments.

In this paper, we demonstrate a real-time DSP function suite, including timing recovery, polarization demultiplexing, frequency offset compensation, carrier phase recovery, and decoding, on a general-purpose server by proposing a low-complexity timing recovery method with CMA filter interpolation. Our implementation significantly reduces the processing time of timing recovery while improving sampling phase tolerance to achieve 5-Gb/s real-time demodulation.

2. Coherent receiver DSP with low-complexity timing recovery method

Figure 1(a) illustrates a coherent communication system, where the coherent receiver DSP is implemented on a general-purpose server with GPU. Dual polarization-quadrature phase shift keying (DP-QPSK) signals are generated in the transmitter side. The received signal is mainly impacted by polarization interference, frequency offset, and the difference in ADC sampling timing. As shown in Fig. 1(b), the server's GPU runs DSP including timing recovery for baud-rate sampled signals, polarization demultiplexing, FOC, CPR, symbol decision, differential decoding, and Gray decoding.

For timing recovery, we implemented and investigated two implementation methods. Figure 1(c) shows the conventional timing recovery method for baud-rate sampled signals based on sinc interpolation [9]. The buffered input signal, $\mathbf{S_T}$, is up-sampled to twice the number of input samples, $\mathbf{S_{T/2}}$, by interpolating zeros between the input signals. For the up-sampled signals, truncated T/2-spaced sinc filter, $\mathbf{W_{sinc}}$, calculated by $\sin(k\pi/2)/(k\pi/2)$, where $-L \leq k \leq L$ and $2L+1$ is the filter tap number, is executed in T-spaced systems yielding $\mathbf{W_{sinc}} * \mathbf{S_{T/2}}$, where $*$ is a convolution operator. Next, the interpolated signal is down-sampled from convolution results of T/2 CMA filter, $\mathbf{W_{T/2}} * (\mathbf{W_{sinc}} * \mathbf{S_{T/2}})$, while its coefficients are appropriately updated. Two streams run these processes; stream 1 is processing for signal data and stream 2 performs filter coefficient processing. In this timing recovery

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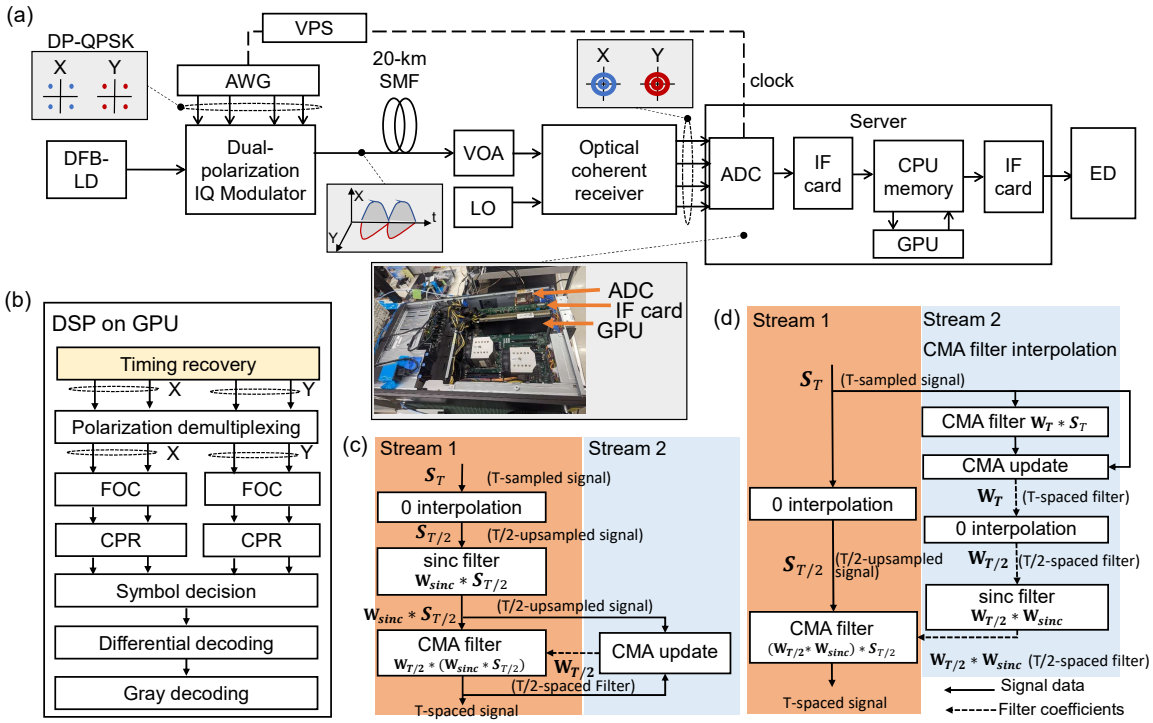

Fig. 1: (a) polarization-multiplexed coherent communication system where the DSP suite is implemented on a general-purpose server, (b) functional block of DSP on GPU, (c) conventional timing recovery method with sinc interpolation, and (d) proposed timing recovery method.

method, the addition of filter processes such as the sinc filter for signal up-sampling increases the computational load for softwarization.

Figure 1(d) depicts the proposed low-complexity timing recovery that eliminates the sinc filter processing for signal data by CMA filter interpolation. While stream 1 subjects the signal data executes 0 interpolation and T/2-spaced CMA filter without sinc filter, stream 2 executes sinc interpolation for filter tap processing in the CMA filter interpolation block. In the functional block, T-spaced CMA filter $\mathbf{W_T}$ is convoluted for partial input symbols without interpolation and CMA filter coefficients are updated. For the filter coefficients, 0 interpolation is executed and $\mathbf{W_{T/2}}$ is generated. Then, the filter coefficients after sinc filter, $\mathbf{W_{T/2} * W_{sinc}}$, are input to T/2-spaced CMA filter and $(\mathbf{W_{T/2} * W_{sinc}}) * \mathbf{S_{T/2}}$ is output. Although stream 2 performs more computations, the timing recovery method assumes that the clock does not change rapidly, so stream 2 can be run slowly and only the processing time of stream 1 must be considered in achieving real-time processing.

3. Performance evaluation

We conducted real-time experiments to assess the DSP with the proposed low-complexity timing recovery method using the configuration shown in Fig. 1(a). We utilized a general-purpose server equipped with Intel Xeon E5-2699v4 CPUs and NVIDIA Tesla A100 GPU. The periodic 134 Mbyte data input was stored in CPU memory and software-based DSP processing was iterated on the GPU. The interface (IF) card employed was an FPGA (Xilinx DK-V7-VC709-G) featuring four 1.25-GS/s 8-bit ADC modules (4DSP FMC125). We used an arbitrary waveform generator (AWG) and IQ modulator to drive a distributed feedback (DFB) laser diode (LD) operating at 1553 nm to generate 1.25-Gsymbol/s DP-QPSK signals with launched power of -4.45 dBm. Pseudo random binary sequences of (PRBS) 23 and PRBS 17 were generated for X and Y polarization, respectively. The signal was input to the coherent optical receiver (Fujitsu FIM24723EB) via a 20-km single-mode fiber (SMF) and a variable optical attenuator (VOA). The launched power of the local oscillator (LO) was 14 dBm. The signals were fed into the ADC module of the server, and the server's 5-Gb/s serial output was directed to an error detector (ED). A variable phase shifter (VPS) was used to adjust the clock input to the ADC.

First, the feasibility of real-time processing was verified by evaluating the processing time. Figure 2(a) shows the processing time of the conventional timing recovery and the proposed timing recovery method for 134 Mbyte data. The proposed method succeeded in reducing the computation load by approximately 38 % compared to the conventional method by omitting the sinc filter processing in stream 1. Note that, given that the clock fluctuations are not large and filter coefficients can be updated slowly, it is unnecessary to consider the processing time of Stream 2, which is operated in parallel. Figure 2(b) shows the processing time of the entire DSP processing including the proposed timing recovery method. In implementing DSP, the GPU handles data in 134-Mbyte blocks

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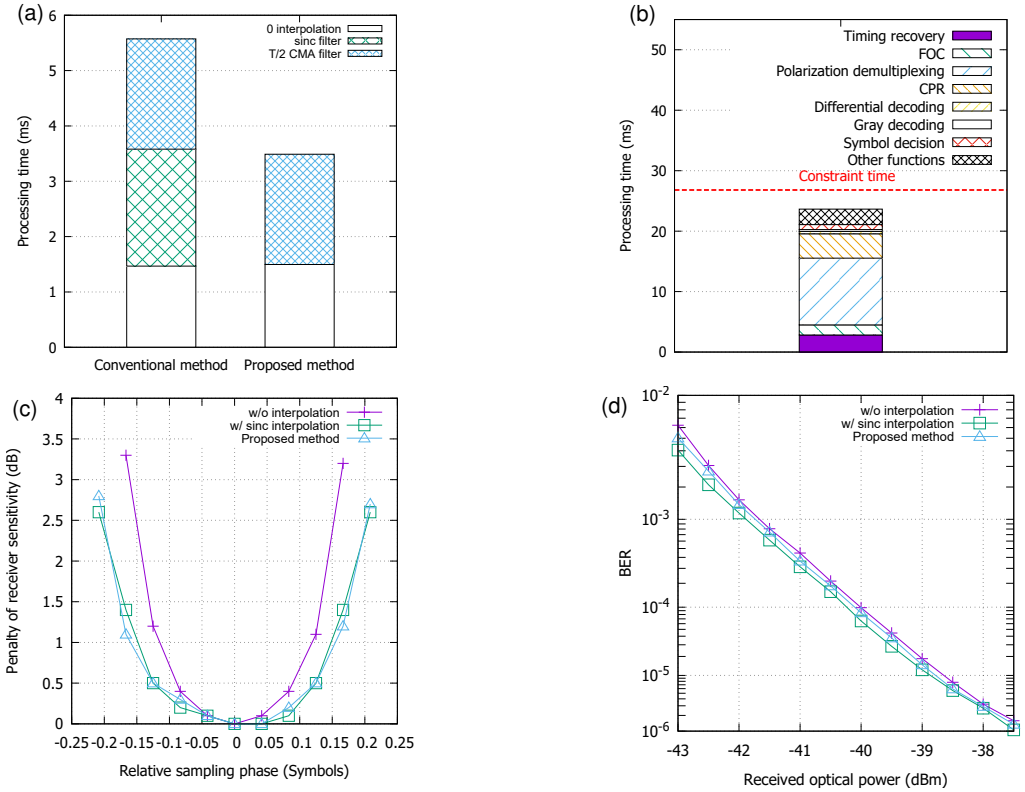

Fig. 2: (a) processing time of timing recovery for signal data, (b) total DSP processing time including the proposed timing recovery, (c) penalty of receiver sensitivity for each relative sampling phase, and (d) BER performance of each method.

across 4 channels. To achieve 5 Gb/s demodulation for a 40 Gb/s input signal (which corresponds to a 1.25-GS/s sampling rate, 4 channels, and 8-bit vertical resolution), it is imperative that DSP execution completes within 26.8 ms of the constraint time. The result verifies that the processing time satisfies the constraint time, confirming the successful 5-Gb/s DSP softwarization by our proposal. We then investigated the influence of timing recovery performance on receiver sensitivity. We define the received optical power yielding the bit error rate (BER) of 10^{-3} as the receiver sensitivity. Figure 2(c) shows the penalty in receiver sensitivity for each relative sampling phase. The relative sampling phase is a relative value when the phase of one symbol is set to 1. The result shows that sampling phase tolerance of the conventional method with sinc interpolation and that with the proposed method are higher than that of the T CMA method without interpolation; the performance of the proposed method almost matches that of the conventional method. Figure 2(d) shows BER performance of each method for the relative sampling phase of zero. Compared to the method without interpolation, there is almost no difference between the conventional method and the proposed method, but the receiver sensitivity is slightly improved since one filter is added before polarization demultiplexing.

4. Conclusion

This paper proposed a low-complexity timing recovery method and demonstrated a baud-rate sampling DSP suite. The experiment showed that our method reduced the processing time by 38 % and achieved 5-Gb/s real-time DSP softwarization with no penalty in sampling phase tolerance compared to the conventional method. As a further study, we will improve the sampling phase tolerance performance with a small number of oversamples.

References

1. NTT Docomo, “White Paper 5G Evolution and 6G (Version 5.0)” https://www.docomo.ne.jp/english/corporate/technology/whitepaper_6g/
2. BBF, ”TR-384 Cloud Central Office Reference Architectural Framework”, Jan. 2018.
3. S. Das, ”From CORD to SDN Enabled Broadband Access (SEBA) [Invited Tutorial],” in Journal of Optical Communications and Networking, vol. 13, no. 1, pp. A88-A99, Jan. 2021.
4. D. R. Mafioletti et al., ”Demonstration of a low latency bandwidth allocation mechanism for mission critical applications in virtual PONs with P4 programmable hardware,” 2022 Optical Fiber Communications Conference and Exhibition (OFC), pp. 1-3, 2022.
5. T. Suzuki, et al., ”Demonstration of Fully Softwarized 10G-EPON PHY Processing on A General-Purpose Server for Flexible Access Systems”, Journal of Lightwave Technology, vol. 38, Issue 4, pp. 777-783, Feb. 2020.
6. S.-Y. Kim, T. Suzuki, J.-i. Kani, T. Yoshida, ”Carrier Phase Estimation Softwarized on GPU Using Decision-Aided Phase Unwrapping for Flexible Optical Coherent Access Systems”, IEEE/OSA Journal of Lightwave Technology, Vol. 36, Issue 9, pp. 1706 - 1714, Dec. 2020.
7. T. Suzuki, S.-Y. Kim, J.-i. Kani and T. Yoshida, ”Real-time Software Implementation of Coherent Receiver DSP Adopting Multiplication-Based Parallel Frequency Offset Compensation for Fully Virtualized Access Networks,” Optical Fiber Communication Conference (OFC), 2023.
8. S.-Y. Kim, T. Suzuki, J.-i. Kani and T. Yoshida, ”Real-Time Polarization Demultiplexing by Multi-Thread Constant Modulus Algorithm for Fully Softwarized Access Networks,” Journal of Lightwave Technology, Early access, Dec. 2022.
9. D. S. Millar, D. Lavery, R. Maher, B. C. Thomsen, P. Bayvel and S. J. Savory, ”A baud-rate sampled coherent transceiver with digital pulse shaping and interpolation,” OFC/NFOEC, pp. 1-3, 2013.

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