A Gaussian Boson Sampling Based Ising Solver

H. H. Zhu[1*], H. S. Chen[2*], H. Cai[1], T. Chen[2], L. P. Chin[3], X. D. Zhang[2†], A. Q. Liu[1†]

[1] institute of quantum technology (IQT), The Hong Kong Polytechnic University, Hong Kong, Hung Hom, Hong Kong
[2] School of Physics, Beijing Institute of Technology, Beijing, China 100081
[3]Department of Electrical Engineering, City University of Hong Kong, Kowloon, Hong Kong Special Administrative Region
*[†]Email Address: eaqliu@ntu.edu.sg *These authors contributed equally to this work*

Abstract: This paper presents an on-chip Gaussian Boson Sampling microprocessor, powered by photonic technology, proficiently solving graph combinatorial problems like max cut and vertex cover. It demonstrates photonic quantum computing's potential to accelerate traditionally insurmountable computations.
OCIS codes: (130.3120) Integrated optics devices; (270.0270) Quantum Optics.

Introduction

Recent advancements in quantum computing and quantum simulation, such as quantum walks [1, 2] and Gaussian boson sampling (GBS) [3-5], have revitalized interest in leveraging quantum techniques to tackle challenging graph-related problems. However, within the realm of photonics platforms, a pressing challenge of significant importance lies in elevating the dimensionality of physically implemented systems and showcasing diverse practical applications, free from constraints imposed by the state space. In this research paper, we present our achievement in constructing a scalable microprocessor for Gaussian boson sampling on a sixteen-mode integrated nanophotonic chip. This innovation holds promise as an Ising solver, potentially accelerating the resolution of combinatorial problems linked to graphs.

Design and Theoretical Analysis

The experimental setup, as depicted in Figure 1, comprises three distinct modules: a pump laser system, a quantum chip with its corresponding control system, and a photon detection system. The microprocessor consists of two essential components. The first entails 16-mode squeezed sources with adjustable squeezed parameters, while the second encompasses a programmable 16x16 gate network, realized through an MZI network. Within the chip, the output photons undergo filtering and polarization, subsequently detected by single-photon detectors. Furthermore, a control system has been designed to independently generate essential control signals, oversee system status, and collect data. A server computer manages the control software and the fundamental quantum algorithms through a user-friendly interface, overseeing the chip's operation and all associated hardware. The chip is meticulously packaged to address optical, electronic, and thermal considerations. This involves the attachment of high-density electrodes to a printed circuit board (PCB) using double-line wire-bonding, employing a fiber array (FA) for light extraction from the chip, and integrating a water-cooling temperature controller beneath the chip.

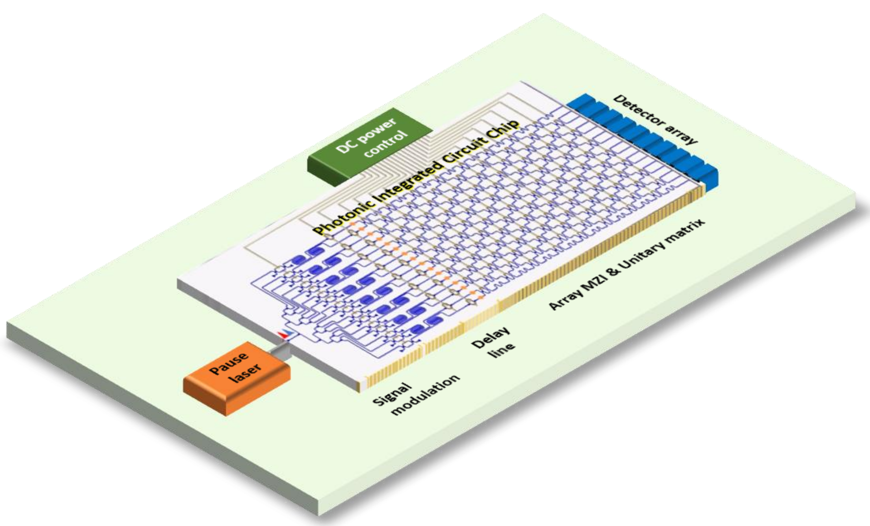

Fig. 1 Schematics of the photonic microprocessor chip.

The GBS-based algorithm and training process for solving graph related combinational problems is shown in Fig. 2. At first, the problem is specified by a graph with an associated adjacency matrix and a cost function by the Hamiltonian $H_{max-cut}$. Because the class of Hamiltonians described above is not differentiable and cannot be used straightforwardly within the training process, we generate a differentiable loss function $L(\theta) = \sum_{i,j} p_i(\theta) A_{i,j} p_j(\theta)$. Secondly, the graph is decomposed by the Takagi decomposition to determine the parameters of unitary matrix and squeezed light source on chip. Thirdly, these sampling results can further be converted to cost function. Through gradient descent or stochastic optimization, we can also update the weight values toward decreasing energy.

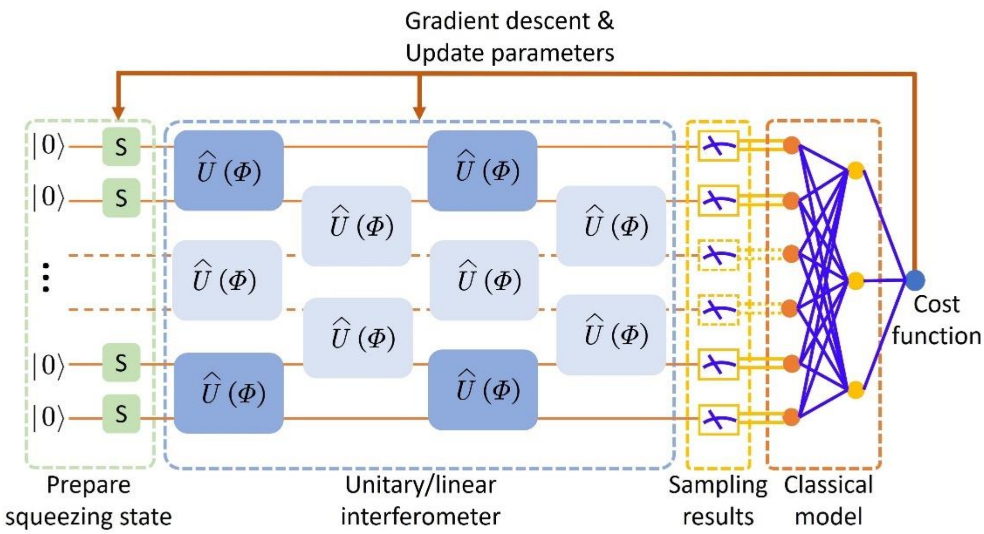

Fig. 2 Schematic of the GBS combined Ising solver algorithm, including quantum sampling and classical cost function calculation.

Results and Discussions

We experimentally demonstrate the applicability of this microprocessor for solving graph combinatorial problems, such as max cut and vertex cover problems of the 16-node graph. Figure 3 shows that the microprocessor can be used to solve max cut problems, which is a partition of the graph's vertices into two complementary sets S and T, such that the number of edges between S and T is as large as possible. Figure 3(a) gives the Ising energy as a function of the number of iteration steps. It is apparent from Fig. 3(a) that the system evolves toward solutions representing lower Ising energies, and subsequently settles into the Ising ground state (or a low-lying excited state). Comparing the Ising energy convergence rate of GBS sampling and uniform sampling in this process is shown in Fig. 3(b). We further solve 41 instances of the max cut for N = 16 random graphs and record the probability of finding exact solutions (ground states) in Fig. 3(c). 37 instances of the success rate of GBS sampling after 20 iterations is over 90%.

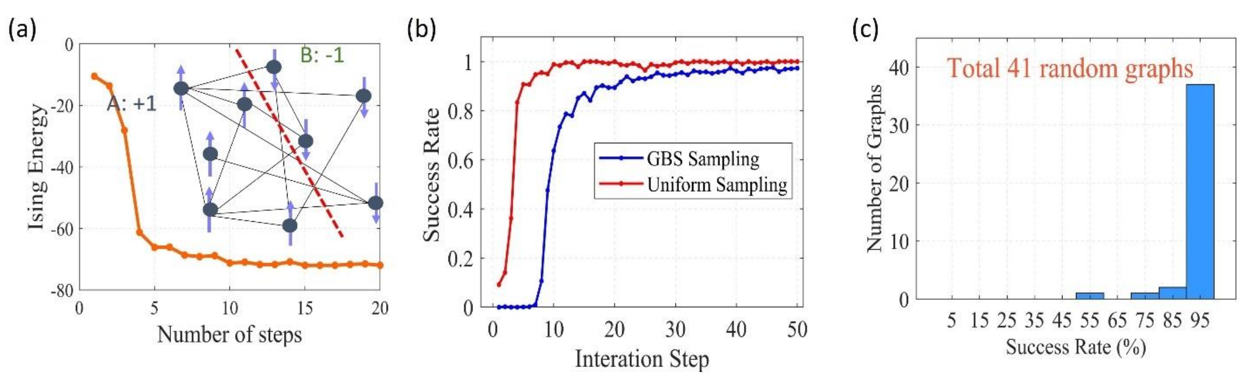

Fig. 3 (a) Ising energy is achieved as a function of the number of iteration steps. Inset: Solved graph and the cutting solution (red line). (b) Observed success rate of obtaining an accurate solution as a function of the iteration steps. Experiments were performed on randomly generated 40 graphs with 16 vertices. (c) GBS random search sampling rate.

Conclusions

In conclusion, we have experimentally demonstrated a gaussian boson sampling microprocessor in an integrated photonic platform: 16 squeezed modes injected into a 16-mode interferometer. The full programmability of our system enables its variable applications. We have further showcased the capabilities of the photonic chip with various graph related combination problem demonstrations with good performance.

Acknowledgment

This work is supported by the Singapore Ministry of Education Tier 3 grant (MOE2017-T3-1-001) and National Research Foundation grant (MOH-000926).

References

[1] J. Carolan, et al. On the experimental verification of quantum complexity in linear optics. Nat. Photonics 8, 621–626 (2014).
[2] Qiang, X.G., et al. Implementing graph-theoretic quantum algorithms on a silicon photonic quantum walk processor. Science Advances 7.9 (2021): eabb8375.
[3] Arrazola, et al. Quantum circuits with many photons on a programmable nanophotonic chip. Nature 591.7848 (2021): 54-60.
[4] Zhong, et al. Quantum computational advantage using photons. Science 370.6523 (2020): 1460-1463.
[5] Madsen, et al. Quantum computational advantage with a programmable photonic processor. Nature 606.7912 (2022): 75-81.