1.6 Tbps (224 Gbps/λ) Silicon Photonic Engine Fabricated with Advanced Electronic-Photonic FOWLP for Co-Packaged Optics and Linear Drive Applications

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Abstract: A 1.6 Tbps (8-channel 224 Gbps/λ) Silicon Photonic Engine, fabricated using advanced electronic-photonic FOWLP, is successfully demonstrated for the first time, enabling low-cost, volume-manufacturable and highly scalable terabit photonic engines for CPO and LPO.

1. Introduction

The exponential growth of optical data connectivity is driven by the insatiable demand for data. Besides architectural changes in hyperscale data centers, the demand for low power and latency optical interconnects are also being accelerated by the needs of AI/ML clusters. Co-Packaged Optics (CPO) is a promising technological approach to address future power dissipation and latency demands. However, many technological and engineering challenges with CPO need to be addressed, resulting in numerous efforts on this front. These include light source, optical packaging, high speed active devices and perhaps most importantly, electronic-photonic packaging [1, 2].

There are extremely challenging demands on electronic-photonic packaging for CPO. Key challenges are channel and bandwidth density, signal integrity of the electrical channels between the ASICs and the Optical Engines (OEs) and compatibility with manufacturable and reliable photonic packaging solutions. For high channel density at 200 Gbps/λ and beyond, it is crucial to completely avoid wire bonds [2] in the RF signal path in order to minimize inter-channel crosstalk, RF signal reflections and bandwidth degradation. It remains unclear what the ideal electronic-photonic packaging approach should be. Through-Silicon Via (TSV) is a possible approach from a technological perspective but has disadvantages of a complex process and high cost. Fan-Out Wafer-Level Packaging (FOWLP) is a mature low-cost advanced packaging technology with widespread and high-volume use in electronic chip applications. However, its use has so far been limited to electronics. In this work, we successfully demonstrate for the first time, a Silicon Photonic Engine fabricated using an FOWLP-based advanced electronic-photonic packaging approach. It is capable of aggregate transmit and receive data rates of 1.792 Tbps (8 channels at 224 Gbps/λ). Besides CPO, it can also be deployed in 224 Gbps/λ Linear-drive Pluggable Optics (LPO) modules.

2. Advanced Electronic-Photonic Packaging based on FOWLP

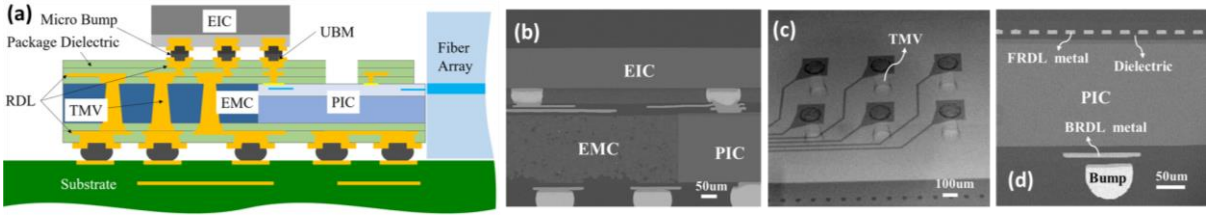

Fig. 1. (a) Schematic illustrating a silicon photonic engine in a FOWLP-based electronic-photonic package. (b) Cross-section SEM showing a FOWLP package on which an EIC is flip chip attached. (c) X-ray micrograph showing TMVs (d) Cross-section SEM showing FRDL above and BRDL below a PIC within a FOWLP package.

The electronic-photonic packages in this work were fabricated using a process platform [3] developed based on FOWLP. The packaging was realized on a 300-mm FOWLP line and adopted a Mold-first approach. A number of key challenges had to be addressed. These include the encapsulation of the PIC without affecting the photonic and RF performance, as well as the management of mechanical integrity, package stress and warpage. In addition, optical coupling ports on the photonic engines also had to be protected and kept pristine throughout the

entire process. In comparison to TSV, where TSV processing is typically performed on full wafers of each chiplet type, FOWLP is able to integrate various chiplets from different process nodes or with different functions using a low-cost packaging process flow through wafer reconstitution. Only Known Good Dies (KGDs) of each type of chiplet are used in the reconstitution of the FOWLP wafer. Fig. 1(a) illustrates the overall package design, while Fig. 1(b) to (d) shows features such as Through-Mold Vias (TMV), Front-side Redistribution Layer (FRDL) and Backside RDL (BRDL). Excellent S11 and S21 performance was obtained for the package RF interconnects. An example is shown in Fig. 2(a) and (b) for the structure illustrated in Fig. 2(c).

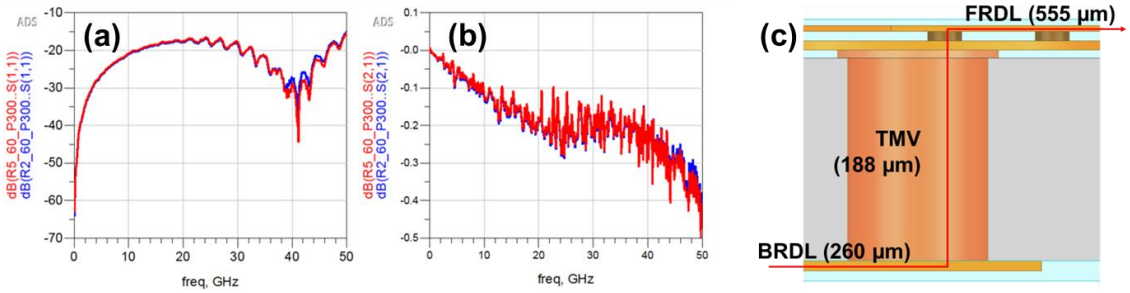

Fig. 2. (a) S11 and (b) S21 characteristics of a 60-Ohm RF interconnect from the backside of the FOWLP package to the front-side (tested on a double-sided probing system). The reflection coefficient is low even up to 50 GHz while the total S21 loss is <0.5 dB at 50 GHz. (c) Schematic showing the dimensions of the BRDL, TMV and FRDL in this RF interconnect.

3. Post-Packaging Wafer-Level Optical Testing

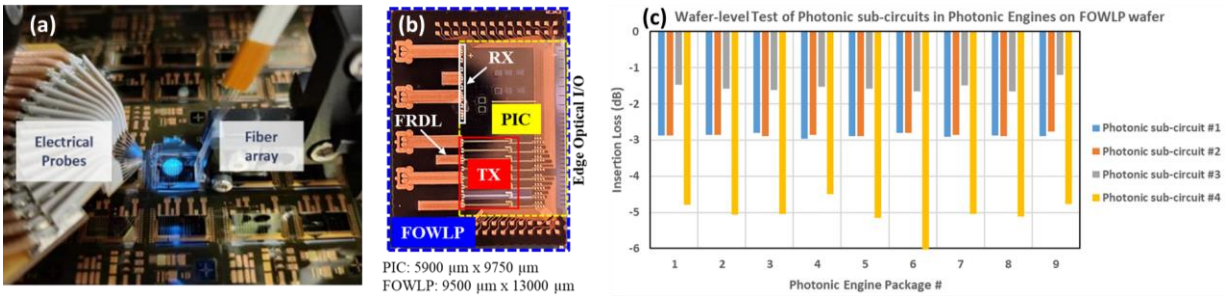

Figure 3. (a) FOWLP wafer with different package variants (b) Photo of 1.6 Tbps Photonic Engine package with dimensions. Package and PIC sizes were not optimized in this first demonstration. Actual transmit and receive sections only take up small areas on the PIC (c) Wafer-level optical test data of a FOWLP wafer showing the insertion losses of 4 different types of photonic sub-circuits on the 1.6 Tbps photonic engine for 9 Photonic Engine Packages (each reconstituted wafer was only partially populated with the 1.6 Tbps photonic engine chiplet).

Wafer-level optical testing was enabled through dedicated open windows in the RDL dielectric to expose the vertical couplers on the PIC. Photonic engine packages were tested at wafer-level on an electronic-photonic wafer-level tester to demonstrate automated high-throughput package optical testing (Fig. 3(a)). In this 1.6 Tbps demonstrator, each package (Fig. 3(b)) contained a single 8-channel Silicon Photonic Integrated Circuit (PIC) transceiver chiplet. The Electronic ICs (EICs), such as drivers and TIAs, were replaced with RF interconnects in the front-side redistribution layer (FRDL) emulating a direct drive architecture. Fig. 3(c) shows the wafer-level optical test data for 4 types of photonic sub-circuits on each PIC in package. These photonic sub-circuits are designed to be sensitive to changes in the physical properties of the PIC. With the exception of 1 sub-circuit due to a particle on the vertical coupler, the remaining 35 sub-circuits maintained consistent performance after FOWLP processing. This proves that the packaging process does not degrade the optical characteristics of the PIC chiplets.

4. Photonic Engine Package Receive and Transmit Characteristics

For receiver testing, reference transmitter optical signals were generated using an in-house silicon photonic Traveling Wave Mach Zehnder Modulator (TWMZM) transmitter board. Electrical modulation signals are generated using a Keysight AWG and amplified to drive the TWMZM. The optical signal is coupled into the photonic engine package using a fiber array and the received electrical signal is captured using a Keysight DCA. Excess losses introduced in the experiment setup such as the RF cables and connector losses were de-embedded. The generated reference transmitter 112 Gbps NRZ eye diagram is shown in Fig. 4(a), while the received electrical NRZ eye diagram is shown in Fig. 4(b). Transmitter-side 5-tap pre-emphasis was applied to compensate for the link impairment. The received electrical eyes from the photonic engine's PD are wide open without any further post-equalization. Due to the improved signal integrity, the electronic-photonic package supports 112 Gbps NRZ using

only few-tap FFE. No complex digital signal processing was required, demonstrating excellent potential for applications such as AI interconnect infrastructures where low power consumption and low latency are needed. The 224Gb/s PAM4 reference transmitter optical and received electrical eyes are shown in Fig 4(c) and (d) respectively. The received eyes are wide open with clearly distinguishable levels.

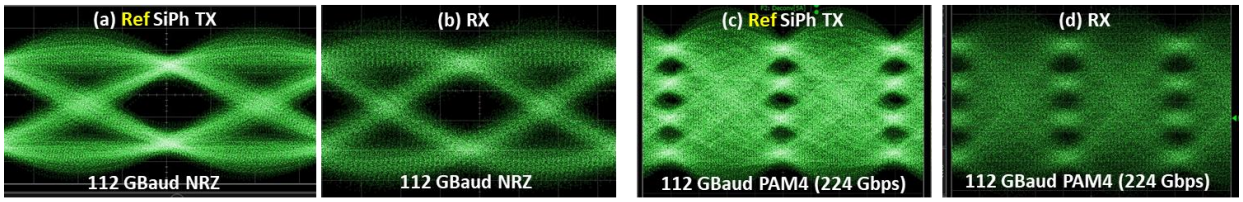

Fig 4. (a) 112 Gbps NRZ optical eye diagram of the reference transmitter. (b) Received 112 Gbps NRZ electrical eye diagram at the high-speed photodetector measured through a 1000 µm FRDL RF transmission line. (c) 224 Gbps PAM4 optical eye diagram of the reference transmitter. (d) Equalized (31 FFE taps) received electrical eye diagram measured through a 1000 µm FRDL RF transmission line.

For transmitter testing, the amplified signal from the AWG was applied to the TWMZM on the photonic engine package through a 900 µm FRDL RF transmission line. Excess RF losses from the setup were de-embedded. Fig. 5(a) shows the eye diagram after a 31-tap FFE TDECQ equalizer. TDECQ of 2.08 dB and ER of 4.066 dB was achieved for 224 Gbps PAM4. Fig. 5(b) to (e) show the effect of the number of FFE taps on the eye quality and TDECQ values. TDECQ of 2.44 dB can be achieved with just 9 taps. The performance can be further improved by optimizing the impedance matching between the RDL RF transmission line and the TWMZM. Like the receiver, the 112 GBaud NRZ eye is wide open with only transmit-side 5-tap FFE and even without post-equalization (Fig. 5(f)).

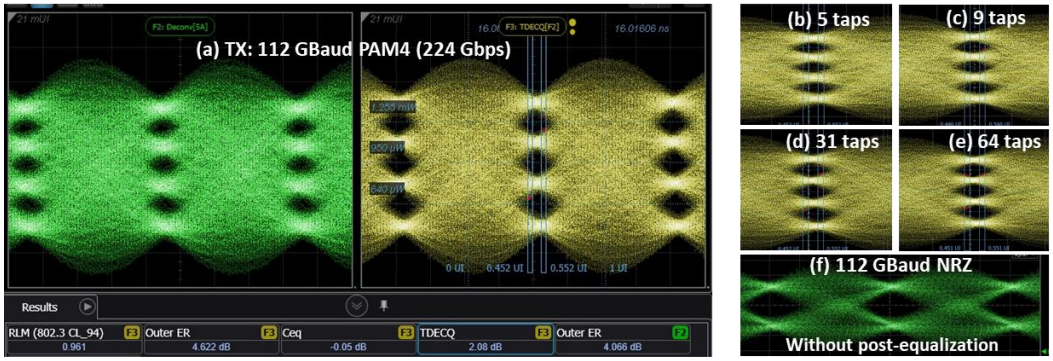

Fig 5. Photonic Engine Package Transmitter optical eye diagrams: (a) 224Gbps PAM4 (ER=4.066 dB, TDECQ=2.08 dB, 31 FFE taps) (b)-(e) Impact of TDECQ FFE tap number on eye openings and TDECQ (5T=3.46 dB, 9T=2.44 dB, 31T=2.08 dB, 64T=1.47 dB). (f) 112 GBaud NRZ shows wide eye opening with transmit-side 5-tap FFE pre-emphasis and even without post-equalization.

5. Conclusions

A low-cost and volume-manufacturable FOWLP silicon photonic engine package with an aggregate 1.79 Tbps (8 x 224 Gbps) transmit and receive capability has been demonstrated, proving the feasibility of silicon photonics for 200 Gbps/λ CPO and LPO. The aggregate transmission capability can be further scaled up by increasing the number and density of channels on the PIC or by doubling or quadrupling the number of PIC chiplets. Overall, we demonstrate 112 GBaud NRZ (112 Gbps/λ) and PAM4 (224 Gbps/λ) with minimized digital signal processing, enabling improved power consumption and latency to address hyperscale data center and AI/ML cluster bottlenecks.

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6. References

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