Latest Progress and Challenges in 300 mm Monolithic Silicon Photonics Manufacturing

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Abstract: In this paper we discuss the latest developments in the GlobalFoundries Fotonix™ program, including enhancements in device performance, packaging, PDK compact models, and in-house test capabilities. © 2024

1. Introduction

We have previously discussed the GlobalFoundries monolithic silicon photonics (SiPh) technology in [1], and [2], which laid the foundation on which we have continued to enhance with lower-loss photonic devices, packaging improvements, and more comprehensive models in our process design kit (PDK). In this paper, we discuss the progress in the 45 nm technology.

2. Devices Enhancements

In recent years, the higher bandwidth requirements for datacom systems using intensity modulated direct detect (IMDD) signaling require higher optical powers to close the links. It is therefore imperative to have devices that are impervious to damage or excess loss due to nonlinear phenomena at these higher powers especially on the transmit side. While some silicon-based active devices such as modulators must remain in silicon to modulate the optical signal, passive components such as waveguides and splitters can be made more robust at these higher optical powers. To that end, we have developed a suite of low-loss silicon nitride (SiN)-based passive devices including waveguides, tapers, 1×2 multi-mode interferometers (MMIs), 2×2 MMIs, directional couplers (DCs), Si to SiN transitions, and crossings [3]. SiN passives have the added benefit of being relatively temperature insensitive. With these SiN passives, we have designed and demonstrated an O-band coarse wavelength-division multiplexer (cWDM), see Fig. 1a, using Mach-Zehnder interferometers (MZIs). As can be seen in the simulated results in Fig.1b and measured results in Fig. 1c, the cWDM has the desired flat-top response as well as a 16 nm 1-dB bandwidth for each channel. The crosstalk can be further improved by minimizing the variation in the directional couplers, which adds unwanted wavelength-dependency especially at the edge of the channels and by using a clean-up filter at each stage. The channel center offset in the measured data can be adjusted by adding extra waveguide length in one of the MZI arms.

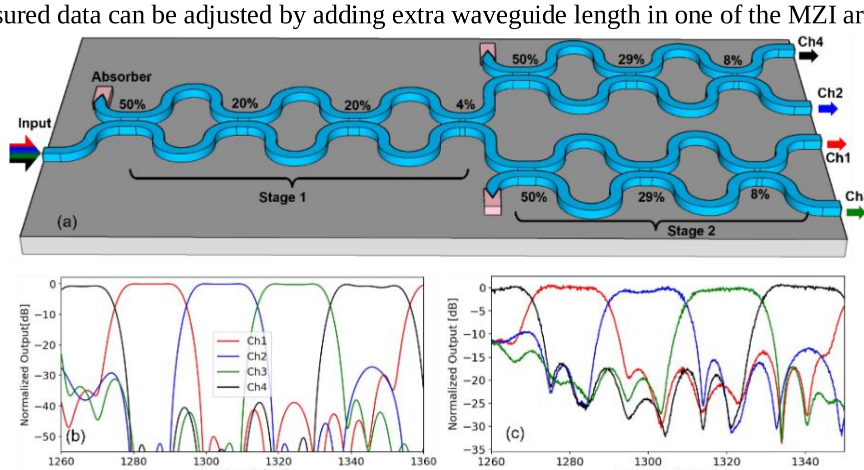

Fig. 1 (a) Schematic view of cWDM filter cascaded MZI structures. Stage 1 separate odd and even channels and stage 2 separate individual channels. (b) Simulated and (c) measured spectrum of the cWDM filter.

3. Packaging Enhancements

To accommodate the higher incoming optical power as well as the need for lower pitch optical I/O, we continue to make progress on SiN-based edge couplers. We have previously reported on our first SiN-based V-grooved edge coupler at 250 µm pitch having < 0.6/0.8 dB TE/TM insertion loss, < -39 dB back reflection, and > 520 mW high-power handling capability in [4], and discussed optical fiber packaging of 250 µm pitch fibers in [5]. We have also begun to develop a 127 µm pitch SiN-based V-grooved edge coupler. As with the 250 µm device, the spot-size converter mode-matches to a single-mode fiber mode while the reduced pitch is matched to a fiber with 80 µm cladding rather than the typical 125 µm cladding. In Fig. 2b, we show the thru-band performance of a loopback in a 32-channel Vgroove bank fiber attached to a 32-channel fiber ribbon. The average insertion loss across the bank is 0.57 dB and 1.24 dB for TE and TM, respectively at 1310 nm. In addition to continued development of the edge couplers, thru-silicon vias (TSVs) as well as laser attach remain part of our packaging roadmap. We have previously reported progress on laser attach in our 90 nm photonics technology in [6].

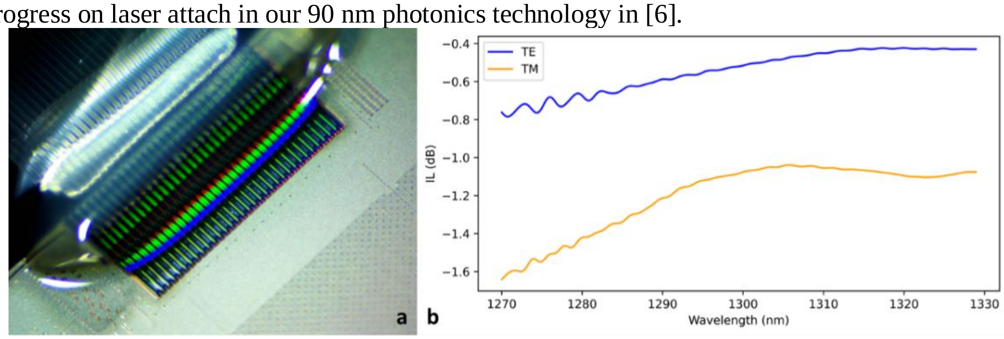

Fig. 2 (a) shows a 32-channel 127 µm pitch fiber ribbon attached to a 32-channel V-groove array, while (b) shows the thru-band performance of two reduced-pitch edge couplers connected by a short SiN waveguide in a loopback configuration.

4. Fotonix^{TM} PDK Enhancements

The advances described above have been added to our PDK, which is updated on a regular cadence such that customers can access new features in a timely manner as we continue to make improvements. While we support custom designs, we produce a PDK with standardized parameterized cells (p-cells) and hardware-based models, so that customers can use proven device designs in their PICs and model system-level performance. The PDK components are flexible to allow for a wide range of customer design points. Thus, to build hardware-based models, we extensively characterize our devices across a range of physical parameters, operating ranges, and combinations thereof [7] to provide customers with flexible, known-good designs. Since the compact models contain these operating and design points as Verilog-A and Spectre models, they can be used to simulate a photonic circuit alongside electronic ones, thus facilitating photonic and electron co-design.

Operating ranges built into our models include temperature-dependence in a range from -25° to 125°C, O-band and C-band wavelength-dependence for devices designed in the corresponding bands, voltage, input optical power, and TE/TM polarization dependence. Additional simulation capabilities include bidirectionality, reflection, phase, and multi-channel behaviors. A particularly complex device is a micro-ring modulator (MRM) in which model we have incorporated self-heating behavior that can affect the insertion loss, extinction ratio (ER), transmission penalty, EE and EO bandwidth, and eye diagram. Fig 3 (b)-(f) show measured data with the extracted data used to build the compact model.

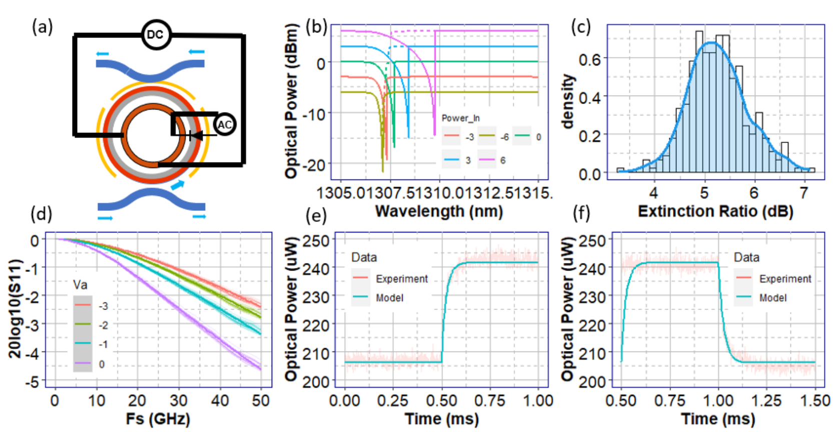

Fig. 3 Model-hardware correlations for: (a) a cartoon of GF Si MRM; (b) ring modulator transmission curve with bistable states at different power (-6,-3,0,3,6)dBm. (c) Micro-ring modulator extinction ratio at minimum transmission penalty; (d)Model hardware correlation: S11 parameter of ring PN junction with open-short de-embedding. (e)(f) Thermal constant characterization (heating and cooling transient).

5. Circuit Demonstrations and System-level Analyses

To benchmark our technology, we have designed and characterized circuits on our multi-project wafer (MPW) fabrication runs, which run a standard process flow. For example, we have demonstrated a transimpedance amplifier (TIA) with bandwidth up to 100 GHz by incorporating an optimized high-Q inductor using the monolithic RF CMOS devices that are part of the technology. With this optimal design, we increased the Q and self-resonant frequency (SRF) of the inductor by 18% and 9%, respectively, thus extending the TIA bandwidth from 94 GHz to 100 GHz.

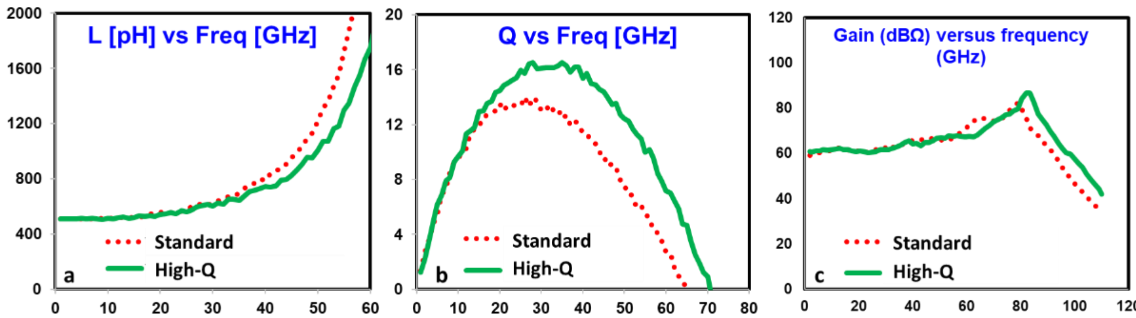

Fig. 4 Measurement results comparing the optimized high-Q inductor to the standard inductor design, showing (a) increased inductance and (b) increased Q, and therefore (c) increased bandwidth.

In addition to circuit demonstrations, we have done system-level analyses of differential group delay (DGD) [8] and propose a polarization-dependent compensation scheme in 200 Gb/s PAM-4 receivers. Due to the thin SOI thickness, the TM mode in the single mode waveguides is not as well-confined as the TE mode, thus giving rise to different modal properties, including group velocity and loss. This becomes a concern in the receiver where the incoming optical signal may be rotated to a hybrid TE-TM mode. To mitigate the resulting DGD and polarization-dependent loss (PDL), we propose utilizing a waveguide delay and variable optical attenuator (VOA) structure on both outputs of a polarization-splitter rotator (PSR) before inputting both signals into a dual-port photodetector (PD), as shown in Fig. 5. For 200 Gb/s PAM-4, a symbol period is T= 9.4 ps; in this case, the accumulated DGD from the edge coupler to the PSR is 8.6 ps that occupies 91% of T, thus an added waveguide length ΔL in the TM-to-TE path adds enough delay to compensate for the DGD. The VOAs can be used to balance the PDL and fine-tune the DGD minimization.

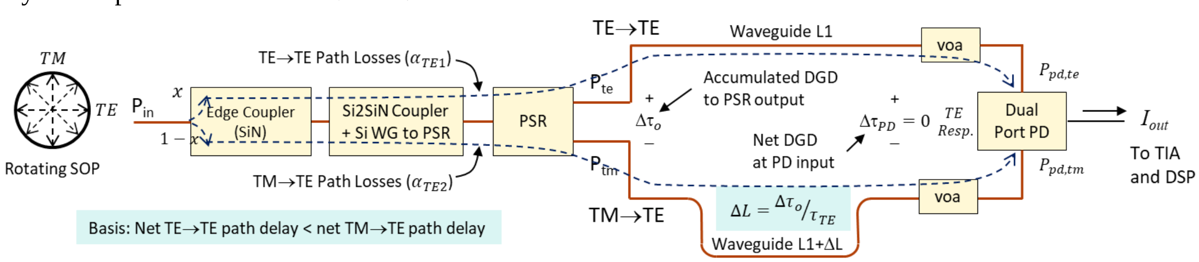

Fig. 5. PSR receiver structure for DGD and PDL compensation.

6. Summary

In this paper, we have discussed our recent progress in device development, packaging, and PDK models, as well as our circuit demonstrations and system-level analyses.

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