Reduced-Complexity Frequency Interleaved DAC for High-Speed Optical Communications

Juan Bonetti,[1,*] and Mario Hueda[1,2]

[1] *Fundación Fulgor, Ernesto Romagosa 518 (Córdoba 5000), Argentina*
[2] *Digital Communications Research Laboratory, FCEFyN, UNC, Argentina*

[*] *juan.bonetti@ib.edu.ar*

Abstract: We propose a new architecture of frequency-interleaved DACs for the all-electronic generation of high-bandwidth signals. We demonstrate significant reduction in both DSP complexity and PAPR, along with a simplified analog circuit design. © 2023 The Author(s)

1. Introduction

Next-generation communication systems demand high-bandwidth modulation (>120 GHz) of single-lambda optical carriers. While modern electro-optical modulators, like Thin Film Lithium Niobate (TFLN) [1] or plasmonic devices [2], meet the high-bandwidth requirement, generating the necessary electrical signals for driving these devices remains a challenge. Presently, integrated Complementary Metal Oxide Semiconductor (CMOS) Digital-to-Analog Converters (DACs) are constrained to around 70 GHz in bandwidth. Consequently, the electrical multiplexing or frequency interleaving of several DACs is commonly adopted as the straightforward solution to overcome this bottleneck. A promising method for implementing the multiplexing of DACs is the Digital Band Interleaving (DBI) scheme [3, 4], shown in Fig. 1 for the case of two bands. The high-bandwidth digital input $x[n]$, with a sampling frequency of f_s, is spectrally sliced in the digital base-band signals $x_L[n]$ and $x_H[n]$, separately converted via parallel DACs of bandwidth $f_s/4$. Digital Signal Processing (DSP) blocks in combination with proper analog filters are required to mitigate the inter-band aliasing caused by both the DAC images outside the first Nyquist zone and redundant bands in the electrical mixer. This approach was recently employed to achieve a DBI-DAC with a bandwidth of 114 GHz [5].

The DBI-DAC architecture shown in Fig. 1 poses implementation challenges that hinder its use in commercial devices, where minimizing power consumption, complexity, and area is crucial: 1) the highly selective digital filters required for band separation and compensation often demand high number of taps (e.g., > 250 taps); 2) the digital bands obtained through DBI exhibit higher Peak-to-Average Power Ratio (PAPR) at the input of DACs [7]; 3) a sharp analog filtering at the mixer output is required to eliminate the redundant band and the Local Oscillator (LO) leakage, and 4) DACs with higher sampling frequency or sharp lowpass filtering may be needed to eliminate images outside the first Nyquist zone [7]. In this work, we present an innovative DSP scheme for frequency-interleaved architectures, based on the concept of the Digital Pre-Inverse (DPI) of the electrical multiplexing process. Our proposal eliminates the need for band interleaving, significantly reducing (*i*) the number of taps (e.g., < 50 taps) of digital filters and (*ii*) the PAPR at the sub-DACs input. In addition, our proposal digitally pre-compensates the inter-band aliasing, eliminating the need for DAC oversampling or analog sharp filters, which significantly streamlines system design.

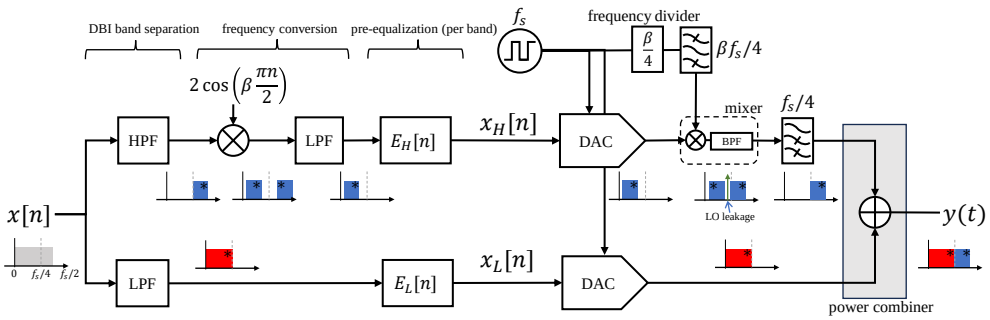

Fig. 1. Digital Band Interleaved (DBI) scheme for two bands.

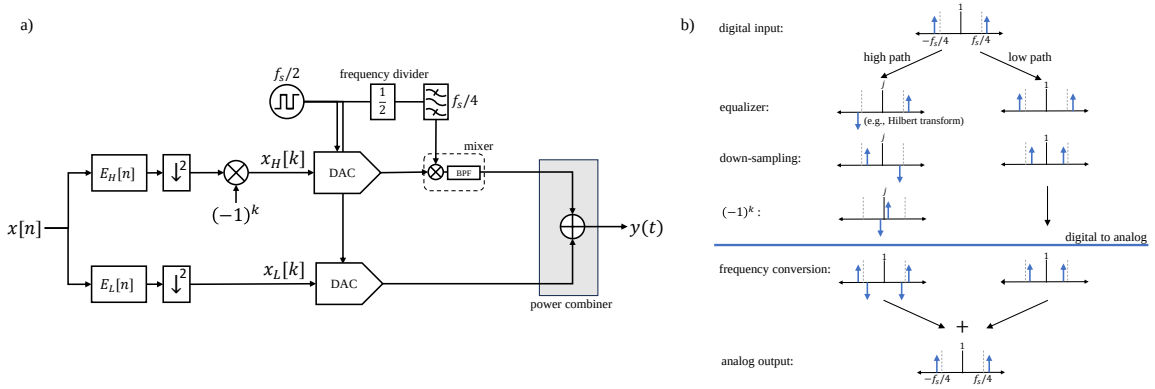

Fig. 2. a) Proposed DPI architecture and DSP scheme. b) Example: high-band single tone input.

2. Digital Pre-Inverse of Frequency-Interleaved DAC

The proposed architecture is shown in Fig. 2(a). The DACs digital inputs $x_L[k]$ and $x_H[k]$ correspond to the low and high bands, respectively, both with a sampling frequency $f_s/2$. The local oscillator for the electrical mixer is derived directly from the clock signal, using a frequency divider. The mathematical model of the architecture is given by

$$y[n] = y(n/f_s) = \sum_m \sum_k \sum_{i=\{H,L\}} E_i[2k-m]F_i[n-2k]x[m], \tag{1}$$

where $E_{H/L}[n]$ are the pre-equalizer digital filters and

$$\begin{cases} F_H[n] = 2\int c_H(t)h_H(n/2f_s - t)\cos(\pi n/2 - \pi f_s t/2)\,dt \\ F_L[n] = \int c(t)h_L(n/2f_s - t)\,dt, \end{cases} \tag{2}$$

being $h_{H/L}(t)$ and $c(t)$ the impulse response of the DACs and the power combiner, respectively. The impulse response $c_H(t)$ models the bandwidth limitation of the mixer output and the power combiner. The digital filters $E_{H/L}[n]$ are required to satisfy

$$\sum_{i=\{H,L\}} \sum_k E_i[2k-m]F_i[n-2k] = \delta[n-m-r], \tag{3}$$

where $\delta[n]$ is the Kronecker delta and r is an arbitrary integer delay ensuring causality. Utilizing the filters described in Eq. 3 for equalizing the digital input $x[n]$ guarantees $y[n] = x[n-r]$, rendering spectral slicing unnecessary. Since no highly-selective digital filters are required, the number of taps is expected to be reduced, as the PAPR of the digital bands $x_L[k]$ and $x_H[k]$. In practice, the digital filters $E_{H/L}[n]$ are trained through a Least-Mean-Square (LMS) method to optimize the output Signal-to-Noise Ratio (SNR), calculated as $\text{SNR} = 10\log_{10}\left(\xi\{x[n]^2\}/\xi\{(y[n]-x[n])^2\}\right)$, being $\xi\{.\}$ the mean value.

Figure 2(b) depicts a fundamental example to aid in understanding how DPI works: a single-tone input at a high-band frequency. It is evident that the low-frequency DAC generates an additional tone to compensate for the unwanted mixer image. While our scheme does not entirely eliminate the LO leakage, we can incorporate a cancellation technique to expand the application range of this proposal [6] (*e.g.*, a proper bias or DC offset can be added before the mixer).

3. Numerical Results

We perform a numerical comparison of the conventional DBI scheme (Fig. 1) and the proposed DPI architecture (Fig. 2). We model the DACs as Zero-Order Hold (ZOH) 8-bit resolution converters followed by fourth-order Butterworth LPFs with a bandwidth of $f_s/4$. The mixer output bandwidth is modeled as a fourth-order Butterworth Band-Pass Filter (BPF) of bandwidth $f_s/4$ and central frequency $f_s/4$. We consider a LO-output isolation of 40 dB. In the case of the conventional DBI we set $\beta = 0.85$ and model the analog HPF as a 15^{th}-order Butterworth filter. The power combiner is modeled as the passive sum of the bands followed by a fourth-order Butterworth filter of bandwidth $f_s/2$. We train the equalizers of both architectures for the same input signal: a random sequence of a 225 GBaud PAM4 modulation format at a sampling frequency f_s =300 GS/s (oversampling factor: 1.33)

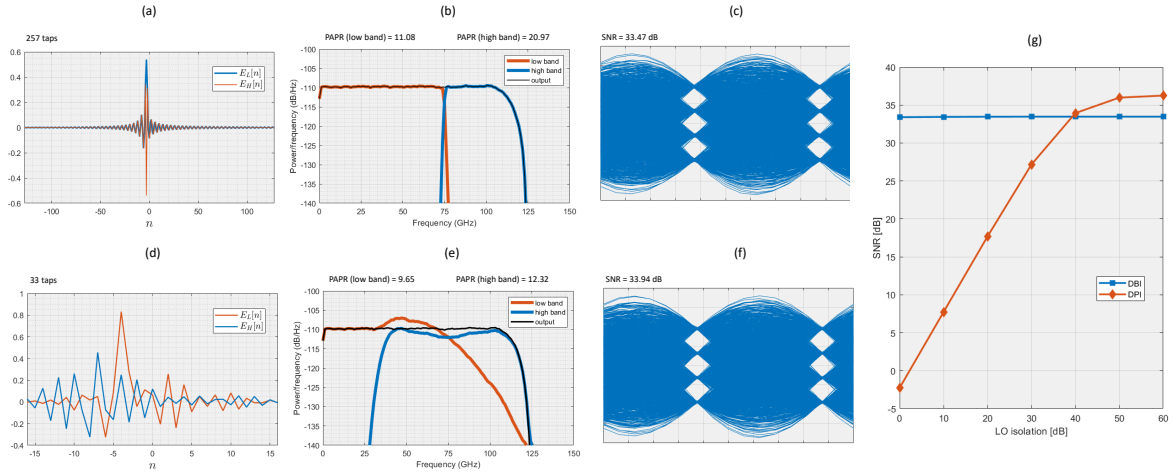

Fig. 3. Numerical comparison of the conventional DBI scheme and the proposed DPI architecture.

and root-raise-cosine pulse shaping with 10% roll-off. The PAPR of this sequence is 7.94. Figure 3(a) shows the optimized equalizers of the conventional DBI scheme, while Fig. 3(b) shows the output spectrum (black line) and the separate contribution of the high (blue line) and low (red line) bands. The output eye diagram is displayed in Fig. 3(c). Analogous results for the proposed DPI architecture are shown in Figs. 3(d), (e) and (f). We observe that the proposed architecture, with equalizers of only 33 taps, achieves a comparable performance to that of the conventional DBI, requiring 257 taps filters. In addition, the PAPR of the digital bands (sub-DACs inputs $x_L[k]$ and $x_H[k]$) is notably reduced, relaxing the requirement on the DACs resolution. A simple comparison of spectra unveils the main differences between the architectures. While the conventional scheme combines bands perfectly separated in the frequency domain, the proposed configuration produces highly-overlapped bands, conspiring to produce the desired output. Figure 3(g) compares the performance of both schemes for different levels of LO leakage. Although DPI exhibits higher sensitivity to LO leakage, it still delivers reasonable performance for isolation levels exceeding 30 dB.

4. Conclusions and Challenges

The digital pre-inverse of the frequency-interleaved process allows for the design of electrical multiplexing architectures with minimal demands on both DSP and analog circuitry. The proposed DPI scheme, not requiring DAC oversampling or sharp analog filters, achieves a similar performance to that of conventional DBI schemes with a reduction of 85% in the DSP size and a 40% of reduction in the maximum PAPR of the DACs inputs. Considering these advancements, the adoption of FI-DACs in commercial devices is primarily constrained by practical issues with the mixer, as nonlinearity, local oscillator leakage, and phase noise.

References

1. C. Wang, *et al.*, “Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages,” Nature **562**, 101-104(2018).
2. W. Heni, *et al.*, “Plasmonic PICs—Terabit Modulation on the Micrometer Scale,” in *ECOC‘2022* , paper Tu4E–3.
3. P. Pupalaikis, “High speed arbitrary waveform generator,” US Patent 7,535,394(2009).
4. X. Chen, *et al.*, “All-electronic 100-GHz bandwidth digital-to-analog converter generating PAM signals up to 190 GBaud,” J. Light. Technol. **35**, 411-417(2017).
5. D. Che, *et al.*, “2.4-Tb/s Single-Wavelength Coherent Transmission Enabled by 114-GHz All-Electronic Digital-Band-Interleaved DACs,” in *ECOC‘2023* , paper ThC2–5.
6. B. Faes, *et al.*, “Highly adjustable mixer-based UWB pulse generator architecture with leakage compensation integrated in 40 nm CMOS,” Electronics Letters **51**(2), 183-185(2015).
7. C. Schmidt, *et al.*, “Digital-to-analog converters for high-speed optical communications using frequency interleaving: Impairments and characteristics,” Optic Express **26**(6), 6758-6770(2018).