Performance Evaluation and Optimization of LDPC FEC for 100 Gbps Coherent Passive Optical Networks

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Abstract: Using both simulation and experimental data, we investigate performance of the LDPC FEC code used in current 25G/50G PONs through clipping optimization for coherent PONs, demonstrating its feasibility for future PON's applications. © 2024 The Author(s)

1. Introduction

It is envisioned that 100 Gb/s per wavelength and beyond will be required in the future to meet continuously growing bandwidth demands [1]. Existing intensity modulated optical technologies face the challenges in meeting power budget requirements through achieving high launch power, mitigating fiber dispersion, and finding suitable transmission wavelengths. Meanwhile, coherent optics has moved beyond its long-haul application origins to metro networks and now it has been introduced into access networks over the past decade. The utilization of coherent optics within a passive optical network (PON), known as Coherent PON (CPON), yields numerous advantages by enabling multi-dimensional modulation and coherent detection and DSP techniques to achieve unprecedently high degree of flexibility in terms of transmission distance, split ratio, and the optical access architecture [2-3]. In each case, forward error correction (FEC) has become an indispensable element for high-speed PON. The evolution of FEC has seen several advancements over time as shown in Figure 1. The [Nx25G-EPON] standard has adopted high-performance, hard-decision (HD), low density parity check (LDPC) FEC with a bitter error rate (BER) threshold of about 1E-2 and a rate of 0.849 and 9dB of net coding gain (NCG) while 25G-PON MSA and [GPON-G.HSP] are also utilizing the same mother code of this LDPC FEC. The industry is currently exploring leveraging this LDPC FEC for the CPON to allow only small changes with the existing chip design and the compatible operation across both physical and medial access control (MAC) layers [4].

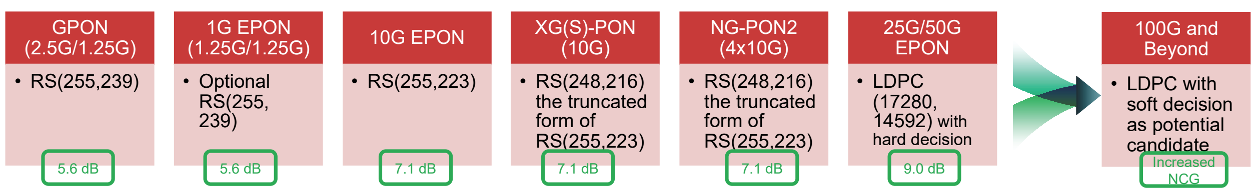

Fig.1 FEC evolution in PONs

In this work, we develop a fix-point simulation model implementing the LDPC code defined in the IEEE 802.3ca standard [5]. The model is verified against published IEEE 802.3ca results. Using co-optimized DSP and LDPC decoding, we evaluate the performance of this FEC with soft-decision decoding in 100Gbps CPON systems through extensive simulations and lab experiments. To the best of our knowledge, this represents the first demonstration of an existing PON LDPC code performing error correction for coherent PON.

2. Simulation Model and Results

The IEEE 802.3ca standard adopts a 12 by 69 proto-graph base matrix with an expansion factor of $z_c = 256$. The studied codeword size is 16774, including the 14392 message bits, 200 shortened bits, 3072 parity check bits (PCBs) with 512 of them truncated. We developed a soft-input-soft-output (SISO) iterative message passing decoder based on usual abstraction of Tanner graph i.e., each row operation of the PCM represents a single parity check code, and each column operation of the PCM corresponds to a repetition code. Layer-by-Layer decoding is used for faster convergence of the decoding process, and Min-Sum approximation is also used to compute the extrinsic information for each parity check node. Our simulation-based results with 10 decoding iterations are listed in Fig.2.

In Fig.2 (a), we optimized the signal clipping level for the quantization of the soft-input (SI) signal with 6-bit resolution. Note that the information BER is used to indicate the uncoded BER at a standard transmission rate. The coded BER indicates pre-FEC-decoding BER at a higher transmission rate considering the added overhead by FEC coding, assuming the same transmit power. The decoded BER vs. clipping level results in Fig.2 reveal that 1.4 is a good clipping level minimizing the decoding performance for BPSK with ± 1 as the signal levels in a discrete BSC channel model. Based on the findings of the optimal clipping level, simulation results are collected for various signal to noise ratio (SNR) levels and are presented in Fig.2 (b). In addition to the SI case, soft-decision performance with hard-input (HI) are also modeled. The expected performance gap indicates that SI may be the preferred choice for high performance systems. Note that the all the curves in Fig.2 (c) are plotted against the information bit SNR. We also plotted the coded BER curve, which is 10*log10(0.8484) = $-$0.7 dB away from the uncoded BER curve where the 14392/(14392+2560+10)=0.8484 is the code rate obtained with the transmitted 14392 message bits, 2560 PCBs, and the 10-bit codeword delimiter. In the following Lab test, only the SI decoding is studied.

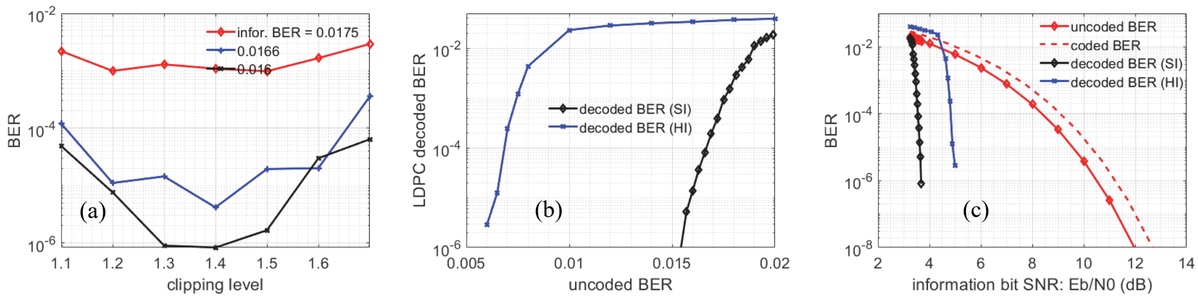

Fig.2 Simulation results: (a) clipping optimization, (b) LDPC output BER vs. uncoded BER, and (c) BER vs. Eb/N0

3. Lab Measurement and Processing Results

Fig.3 (a) illustrates the experimental configuration employed in the FEC coded modulation testbed. The transmitting system comprises an 80-GSa/s four-channel arbitrary waveform generator (AWG) serving as the four-channel signal generator, a 1550-nm external cavity laser (ECL) emitting at 15 dBm, which functions as the light source, and a dual-polarization coherent driver modulator (DP-CDM) employed as the electrical-to-optical signal converter. The signals is the standard Dual-Polarization Quadrature Phase-Shift Keying (DP-QPSK) format with LDPC coding. The signal's baud rate remains fixed at 25 GBd. The symbols undergo resampling to align with the 80-GSa/s sampling rate required for the digital-to-analog converter (DAC) of the AWG. To emulate real-world PON scenarios, an optical distribution network (ODN) is incorporated, consisting of a 50 km fiber link and a 1x32 passive splitter. Moving to the receiver end, the optical signal is combined with a local oscillator (LO) and subsequently detected by balanced photodetectors within an integrated coherent receiver (ICR). To optimize the signal power level for detection, an erbium-doped fiber amplifier (EDFA) operates as an optical pre-amplifier prior to the ICR. The signals then are directly fed into an optical modulation analyzer with an acquisition rate of 80 GS/s. Subsequently, offline processing is carried out with standard coherent DSP functional blocks. This includes tasks such as clock recovery, chromatic dispersion compensation, polarization mode dispersion compensation through the use of the least-mean-square (LMS) and constant modulus algorithm (CMA), carrier frequency offset estimation, and phase recovery.

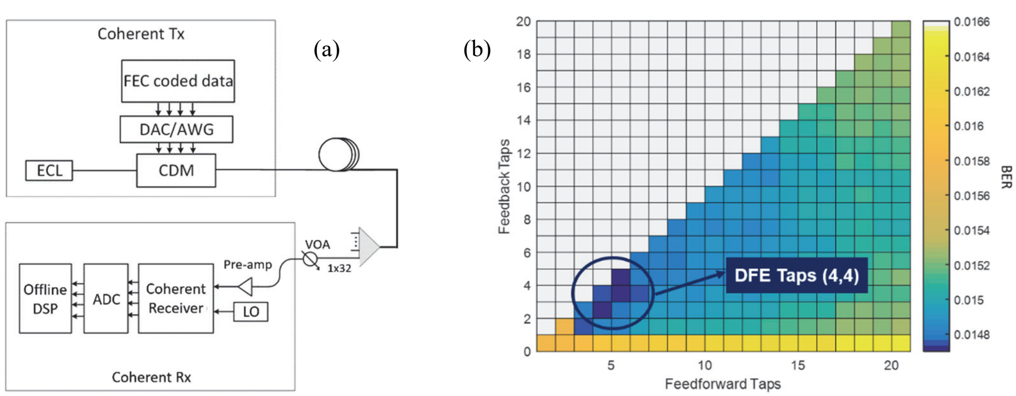

Fig.3. (a) Experimental setup for FEC coded modulation testbed, and (b) DFE Tap number optimization results

The offline processed baud rate samples are sent to the LDPC decoder for decoding. One key task in our work is to synchronize the transmitted and the received codeword sequences. To obtain enough data points, the VOA is fined tuned to change the received optical power (ROP) in a fraction of a dB scale. Multiple measurements are made to have enough data for decoding. To further enhance receiver sensitivity, we also added a decision feedback equalizer (DFE) model following the FFE-CMA and phase recovery stages. Register with 6-bit resolution is again used to store the LLR values for the input signal. Clipping optimization, although not shown here, leads to an optimal clipping level at 1.426. We have first optimized the DFE in terms of the number of taps in the feedforward filter (FFF) and feedback filter (FBF). The ROP used for this study is -41.3 dBm and the results are summarized in Fig.3 (b), showing that the combination of 4 FFF and 4 FBF taps is the best case, where the pre FEC BERin is 0.0148. Note that the residual dispersion is already compensated by the bulk CD compensation filter prior to the DFE. As a result, a causal structure is used for the DFE.

Both the cases of with DFE and without (w/o) DFE are studied for the performance evaluation of the LDPC code with SI soft-decision and the same decoder model used in Section 2. Because error propagation can happen when DFE is used and the generated burst error can have a negative impact for the LDPC decoding, we tested LDPC both with and without interleaving. Note that per the IEEE 802.3ca standard, the interleaver and de-interleaver are realized by using 10× 256 by 256 Omega networks and reverse Omega networks, for which we implemented in our LDPC programs with a specific random seed used for interleaving/de-interleaving. As shown in Fig.3a and c, for both the interleaving and the no-interleaving cases, the BER performance is better for the case with DFE vs. without DFE, as expected. Comparing Fig.4 (a) with Fig.4 (c), we found that the BER performance with interleaving is better than without interleaving. This may be caused by the reduction in the correlation among codeword bits.

The LDPC soft-decision decoding performance is summarized in Fig.4 (b) and d for LDPC with and without interleaving respectively. For comparison purpose, the preFEC BERin data from Fig.a and c are re-plotted in Fig.4 (b) and (d). As shown by Fig.4 (b), the BER performance with DFE is better than the case without DFE, indicating that the error propagation of the DFE is mitigated by the use of interleaving. However, from Fig.4 (d) with no interleaving is used, when the ROP is less than −42 dBm, the case with DFE has a worse BER performance than the case without DFE, indicating the negative impact of burst errors on LDPC decoding.

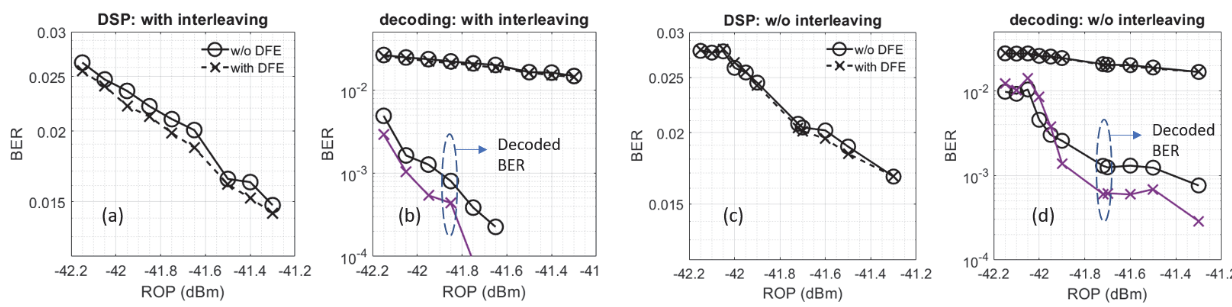

Fig. 4. Performance of the 100 Gbps CPON FEC coded modulation testbed with BER vs. ROP for LDPC with interleaving in (a) and (b) and LDPC without interleaving in (c) and (d).

4. Conclusions and Future Work

Our study leveraged simulation and experimental data to optimize the DSP and assess the performance of the LDPC FEC code that is currently implemented in current 25G/50G PONs for coherent PON applications. Clipping optimization can lower the LDPC decoded BER from ~1e-4 to 1e-6 for the studied range at with 6-bit resolution, which may lead to a lower preFEC BER threshold. DFE tap number optimization results in reduced preFEC BER with Lab data, yielding an enhanced LDPC decoded BER performance. The results confirm the code's viability, showcasing its potential for future PON deployments. Further investigations and optimizations can build upon these findings to unlock even greater efficiencies and capabilities in future PON systems.

5. References

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