Free-space optical receiver with real-time self-configuration using a fully integrated CMOS controller

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Abstract: We present a CMOS chip for closed-loop control of integrated photonic processors, able to configure 8 interferometers in 20ms while consuming 80mW. The chip autonomously mitigates the effect of atmospheric turbulence in free-space receivers.

1. Introduction

Photonic integrated circuits (PICs) are experiencing increasing application in the field of free-space optics (FSO) to address the need for wireless bandwidth and low latency associated with internet-of-things technologies in next-generation networks [1]. Performances, however, are degraded by the presence of obstacles and atmospheric turbulence, acting as a random phase and amplitude modulation that has to be compensated to ensure a correct reconstruction of the beam. These effects can be mitigated using a multi-aperture receiver, that samples the distorted wavefront in multiple points by means of an optical phase array (OPA) reducing the probability of fading and scintillation [2]. Since each portion of the optical signal has its own amplitude and phase, each input needs to be coherently combined to ensure correct reception. This operation can be performed directly in the optical domain by a programmable photonic processor, made of a mesh of Mach-Zehnder interferometers (MZI) arranged in a binary-tree configuration (Fig. 1a) [3].

To compensate for the time-variant effect of atmospheric turbulence, the configuration of each MZI needs to be constantly updated over time, by properly driving the thermal actuators integrated in each device. In particular, a coherent sum of all the input beams towards a single output port is automatically obtained by minimizing the readout current of the integrated photodiodes (PD) placed at one output port of each MZI. Previous demonstrations successfully validated this approach by controlling the operation of the photonic processor with a custom electronic platform [4]. Although effective, the area ($> \mathrm{cm}^2$) and power dissipation ($\approx$ W) of the electronic platform make it hardly scalable to photonic chips with more than a few tens of devices. In this work, we present an 8-channel CMOS application specific integrated circuit (ASIC) that can automatically stabilise and reconfigure 8 MZIs without any prior calibration, with a power consumption of only 80 mW and an area occupation of $12\,\mathrm{mm}^2$, providing a scalable solution for controlling programmable FSO receivers of growing complexity.

2. Architecture of the CMOS controller

Each MZI of the mesh has one output port connected to an on-chip germanium photodiode (PD) that feeds one channel of the electronic chip, whereas the tuning of the working point of the interferometer is made possible by acting on the power dissipated by a couple of integrated thermal phase shifters (nominal resistance of $\approx 400\,\Omega$ and $\approx 1\,\mu$s thermal time constant). The control loop that lies in between (Fig. 2a), fully integrated in our ASIC, relies on the dithering technique to implement a robust calibration-free feedback strategy [5]. The bias points of the heaters are set by a pair of DACs working in the 0-6V range, equivalent to a $\approx 0-3\pi$ shift unbalance between the two optical paths. Two orthogonal square-wave modulations (*dithering* signals) with selectable amplitude between 5 and 100 mV and frequency $f_{dith} \approx 8.3$ kHz are superimposed to the heater voltages. The current generated by the PD, which is modulated according to the dithering amplitude, is converted into a voltage and filtered by an analog front-end, digitized and demodulated so as to extract the dithering components, which are proportional to the partial derivatives of the MZI transfer function around the working point defined by the heaters biases. The demodulated signals are then accumulated to implement an integral controller that updates the working point of the heaters every $T_{dith} = 120\,\mu$s and drives them to bring to zero the measured dithering amplitude, thus maximizing or minimizing the power impinging on the PD according to the user-defined sign of the feedback loop.

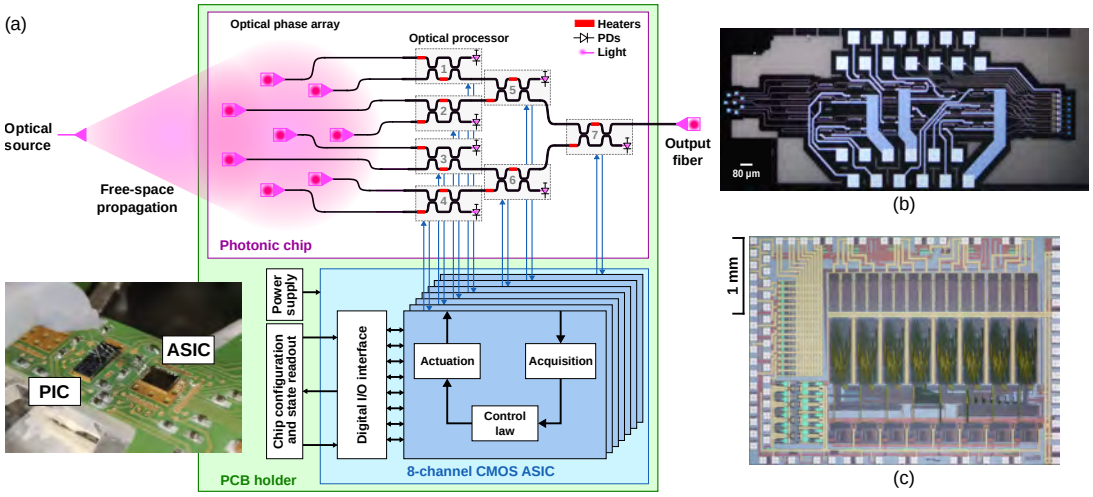

Fig. 1. a) Architecture of the free-space optical receiver, connected to the CMOS controller, and picture of the realized prototype. b), c) Micrographs of the photonic and CMOS chips, respectively.

The ASIC is designed to automatically adjust the gain of the analog stage in order to handle an optical power at PD ranging from about 0 dBm to less than −50 dBm allowing an optimal operation at both maximized and minimized PD current. To improve the linearity of the control loop, a square-root operation is performed at digital level on the value that is fed to the DAC. It allows to compensate for the quadratic non-linearity intrinsically arising from the fact that, despite controlling the voltage V_H applied to the actuators, the phase shift is proportional to their dissipated power $P_H \propto V_H^2$.

The digital part of the circuit is provided with a serial interface that lets the user set several working parameters, including the bandwidth of the control loop and the dithering amplitude, which may be modified to optimize the circuit for different optical powers received by the OPA. Two programmable thresholds trigger the reset of the integral controller at a user-defined value whenever it gets too close to the power supplies. Furthermore, it is possible to fix the working point of each channel either to the state previously reached by the control loop or to whatever configuration manually set by the user. This latter feature is useful for the characterization of the transfer function of each MZI in the PIC. Finally, a second 2-wire serial interface is available to monitor the voltage applied

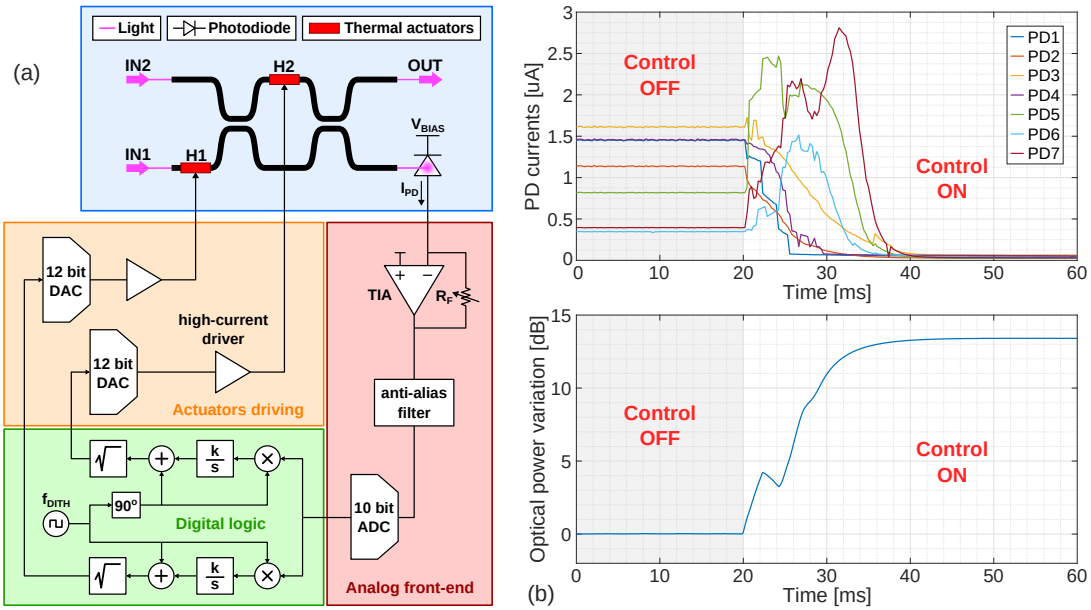

Fig. 2. a) Schematic view of the internal structure of the CMOS controller. b) Experimental measurement showing the successful minimization of the current detected by the on-chip PDs when activating the chip action, resulting in a maximization of the optical power at the mesh output in 20 ms.

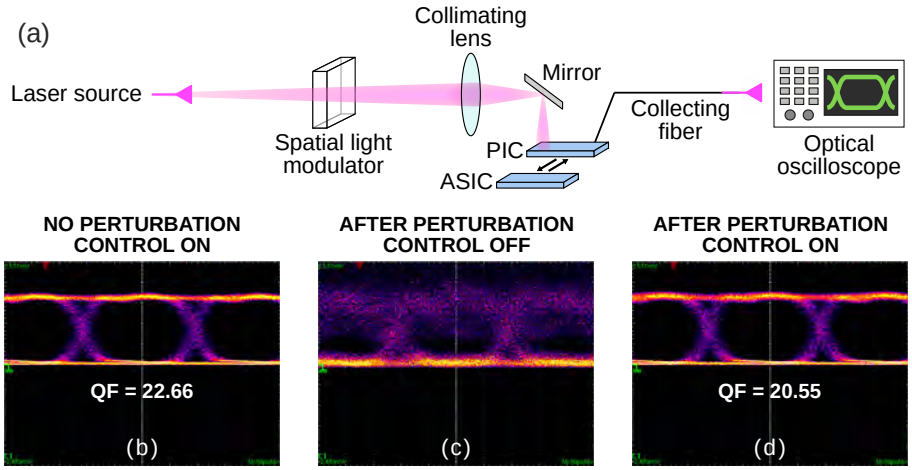

Fig. 3. a) Schematic of the free-space optical setup. Eye diagrams at the output of the optical processor b) before and c) after the placement of the phase mask while keeping the ASIC control action off and d) after the activation of the controller, that successfully compensates the perturbation.

to the actuators and the corresponding current flowing in the PDs.

3. Experimental results

An initial experimental validation was carried out to estimate the bandwidth of the controller, with results reported in Fig. 2b. First, the control loop is deactivated with the PIC set to a random working point, so that only a fraction of the optical power in each MZI is steered towards the correct output. At $t = 20\,\text{ms}$, the loop is turned on, and each interferometer is driven independently from the others to minimize the current in each integrated photodetector. As a result, the total output power of the mesh is increased by $\approx 13\,\text{dB}$ within $\approx 20\,\text{ms}$, although the interferometers connected to PD1-4 reach their stable equilibrium point in less than 10 ms. These are the interferometers located immediately after the OPA, hence phase and amplitude of their input beams are only determined by the sampled free-space wave. The following MZIs, instead, while being controlled simultaneously with the previous ones, are affected by the amplitude and phase perturbation resulting from the former interferometers when they reach a stable equilibrium point. This effect is ultimately present in the output power of the PIC (Fig. 2b, bottom), which is coupled via fiber to an external photodiode, with a non-monotonic transient response.

A second experiment, whose setup and results are shown in Fig. 3, demonstrates the effectiveness of our system in improving the performances of the optical processor as a free-space receiver for a modulated $5\,\text{Gbit/s}$ on-off keying (OOK) data stream. Light from the input fiber was projected through a system comprising a spatial light modulator (SLM), a collimating lens, and a rotating mirror, emulating a free-space propagation of hundreds of meters [4]. The SLM has been used to generate arbitrary phase masks and perturb the propagation of the beam. First (Fig. 3b), a reference eye diagram was measured with no obstacles along the path and the control loop activated, resulting in a *quality factor* QF=22.66. When the ASIC controller is turned off and a phase mask is placed between the input fiber and the OPA (Fig. 3c), the waves sampled by the OPA interfere with the wrong phases. As a consequence, a power loss of $\approx 15\,\text{dB}$ and a complete degradation of the quality of the eye is observed at the output of the PIC. Finally, when the control loop is re-activated, the optical processor is reconfigured, compensating for the perturbation introduced with the mask and restoring a QF=20.55.

References

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