Low-loss, multi-reticle stitched SiN waveguides for 300mm wafer-level optical interconnects

Pengfei Xu[1], Chiara Marchese[1], Guy Lepage[1], Negin Golshani[1], Ruben Van Eenaeme[1], Andrea Mingardi[1], Joost Van Ongeval[1], Rafal Magdziak[1], Luc Halipre[1], Darko Trivkovic[1], Peter Verheyen[1], Maumita Chakrabarti[1], Dimitrios Velenis[1], Andy Miller[1], Filippo Ferraro[1], Yoojin Ban[1], Joris Van Campenhout[1]

[1]imec, Kapeldreef 75, 3000, Leuven, Belgium

e-mail: pengfei.xu@imec.be

Abstract:

We present 56-cm long LPCVD SiN waveguides traversing a full 300mm wafer, targeting future optically interconnected wafer-scale multi-chip compute systems. High-precision reticle stitching (loss below 0.01dB/interface) enables intra-wafer waveguide loss of just 0.15dB/cm in the O-band.

1. Introduction

The growing adoption of artificial intelligence (AI) and machine learning (ML) is driving an increasing demand for high-bandwidth, low-latency, and low-power interconnects between compute chips (XPU) and high-bandwidth memory (HBM) in AI/ML clusters [1,2]. Wafer-level optical interconnects (WL-OI) are an emerging technology to interconnect several tens of XPU's or HBM's on a single 300mm wafer with superior bandwidth density, energy efficiency and latency compared to fiber-coupled links, and with much longer reach compared to on-wafer electrical interconnects [3]. As interconnect distances in the envisioned WL-OIs (see Fig. 1d) are expected to amount to several tens of centimetres, there is a strong need for ultra-low loss waveguides (<0.2dB/cm) that can traverse the entire 300mm wafer, along with sufficiently dense waveguide pitch (<10µm) and sufficiently tight bending radius (<100µm). In this paper, we present a 300mm wafer-scale SiN waveguide technology, combining low pressure chemical vapor deposition (LPCVD) SiN waveguides with high-precision photolithographic reticle stitching yielding stitching losses below 0.01dB. In combination with the low linear propagation loss and the high optical confinement of the 400nm thick LPCVD SiN waveguides, cross-wafer loop-back waveguides up to 56cm long are demonstrated with all-in waveguide loss of just 0.15dB/cm including up to 20 stitch interfaces as well as 56 100µm-radius 90-degree bends.

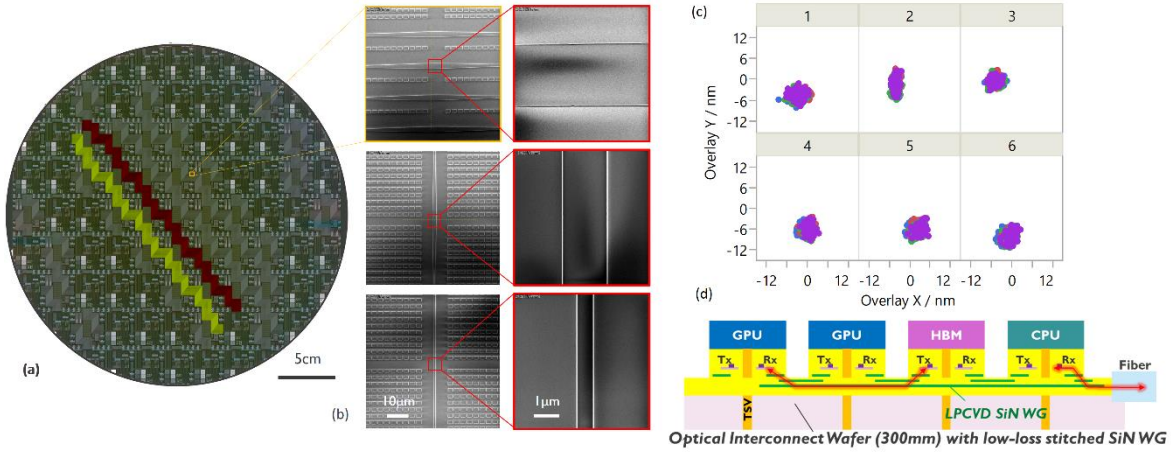


Fig. 1. (a) Photograph of a fabricated 300mm wafer with reticle-stitched SiN waveguide bundles (cross-wafer waveguides highlighted in yellow and red), (b) detailed top-view SEM images of stitched regions, (c) stitching overlay accuracy statistics, and (d) schematic view of the envisaged optically interconnected wafer-level multi-chip compute system.

2. Wafer fabrication and reticle stitching

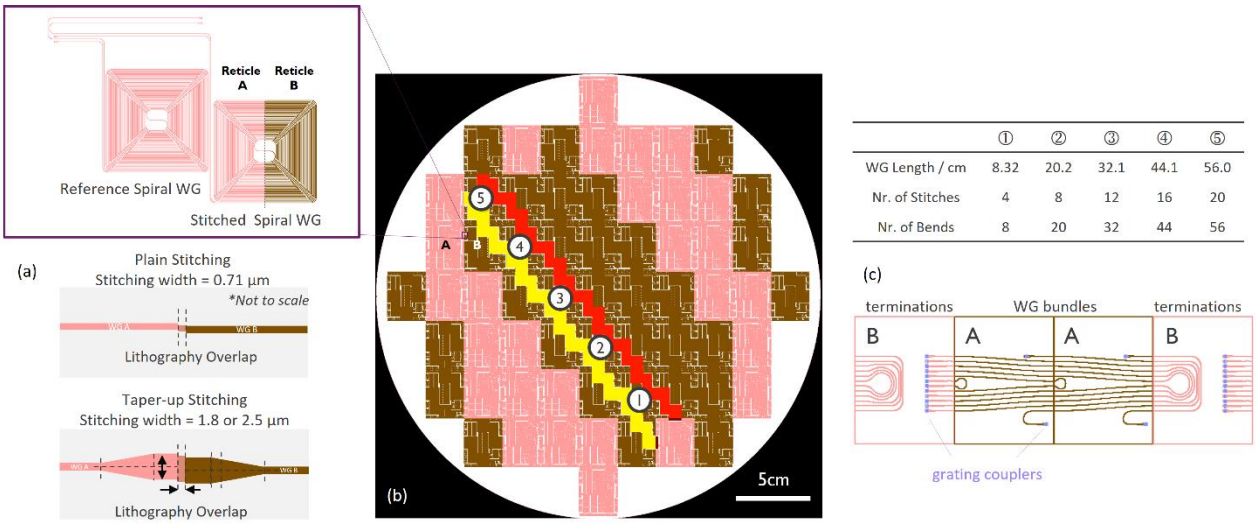
The work presented in this paper has been carried out in imec's 300mm CMOS pilot line. The 300mm wafer processing starts with a 2.7µm thick silicon oxide deposition. Next, a 400nm-thick LPCVD SiN layer is deposited. The LPCVD SiN layer is patterned using 193nm immersion lithography, using two different reticles each covering a full 26mm x 33mm die. Each die is exposed with the reticle of choice via a dedicated photolithography job, resulting

in the full wafer exposure as shown in Fig1(a). To enable the reticle stitching between neighbor dies, each single die overlaps with all adjacent dies, overlay structures are placed in this die overlap in order to characterize the die-to-die misalignment. Several scanning-electron microscope (SEM) pictures of stitching interfaces are shown in Fig1(b), revealing a very smooth transition without any major waveguide shape irregularity. The misalignment between neighboring dies was measured with dedicated overlay marks on six separate locations per die. A full-wafer measurement was carried out on a total of four wafers and the maximum observed x- or y- misalignment was 12nm Fig. (1c). After the SiN patterning, an oxide top cladding layer is deposited and subsequently planarized, targeting 2.6µm of remaining oxide on top of the SiN after the final planarization an optical test is performed.

3. Design of the stitching interface and optical test structures

Leveraging the high alignment accuracy of reticle stitching with advanced 193-nm lithography, as described in the previous section, we designed relatively simple, abrupt stitch interfaces with a compact footprint, similar to earlier work using Si waveguides [4]. Two key design parameters were explored, targeting low optical loss for TE modes in the O-band: (1) the waveguide width at the stich interface, optionally tapering up to 1.8 µm or 2.5µm from the nominal 710nm SiN waveguide width (using compact low-loss tapers with length below 35µm) and (2) the overlap between the two lithographic exposures, ranging from 10nm to 50nm. According to full 3-D FDTD simulations, such interfaces are expected to yield optical loss below 0.006dB for overlay errors up to 20nm. Dedicated spiral waveguide structures with 100 stitching interfaces were implemented along with reference spiral waveguide without stitching to extract the stitching loss at wafer scale (see Fig. 2a).

As a simple proof-of-concept demonstrator, we also included several cross-wafer loop-back waveguides by arranging waveguide bundles (on the first reticle) and bending/termination structures (on the second reticle) as shown Fig. 2b-c. Loop-back waveguides with varying total propagation length (up to 56cm), number of stitching interfaces (up to 20) and number of 100-um radius 90-degree bends (up to 56) are included, for the same stitching taper-width design sweep. For all test structures, SiN grating couplers are implemented to perform wafer-scale testing.



	①	②	③	④	⑤
WG Length / cm	8.32	20.2	32.1	44.1	56.0
Nr. of Stitches	4	8	12	16	20
Nr. of Bends	8	20	32	44	56

Fig. 2. (a) Design parameters of the stitch interface and test structure, (b) schematic top view of the 300-mm stitched wafer, showing the cross-wafer loop-back SiN waveguides, (c) detailed view and design parameters of the loop-back test structures.

4. Measurement results

First, SiN waveguide loss and bending loss measurements were carried out from standard test structure consisting of cut-back spiral waveguides with 50-µm radius 90-degree bends, revealing a nominal linear propagation loss of 0.165dB/cm and bending losses of 0.007dB/bend (Fig. 3a). Next, the stitched spiral test structures were measured. The extracted stitching loss values are generally very low (Fig. 3b), in some cases negative due to imperfect fiber coupling repeatability during wafer-scale testing (~1dB variability). As such, we can conservatively derive the upper limit for the stitching loss to be 0.01dB/interface.

Subsequently, the cross-wafer loop-back waveguides were measured as shown in Fig. 3c. The extracted all-in (length-referred) waveguide loss was derived from linear fitting to be 0.15dB/cm for all sets of loop-back waveguides

measured on the wafer, and independent of the stitching taper width. Even the non-tapered SiN waveguide with 710nm width obtained such low stitching loss, which is a further confirmation of the high alignment accuracy during lithography. In addition, the demonstrated taper-less stitching interface has the lowest possible footprint.
Although lower stitching losses have been demonstrated for lowly-confined 100-nm thick SiN waveguides on 200mm wafer size [5], such waveguides don't support low-loss waveguide bends with radius below 100µm, which are deemed critical for on-wafer optical networks in multi-chip compute systems. For such applications, the highly confined 400-nm thick SiN LPCVD waveguide platform may provide better performance.

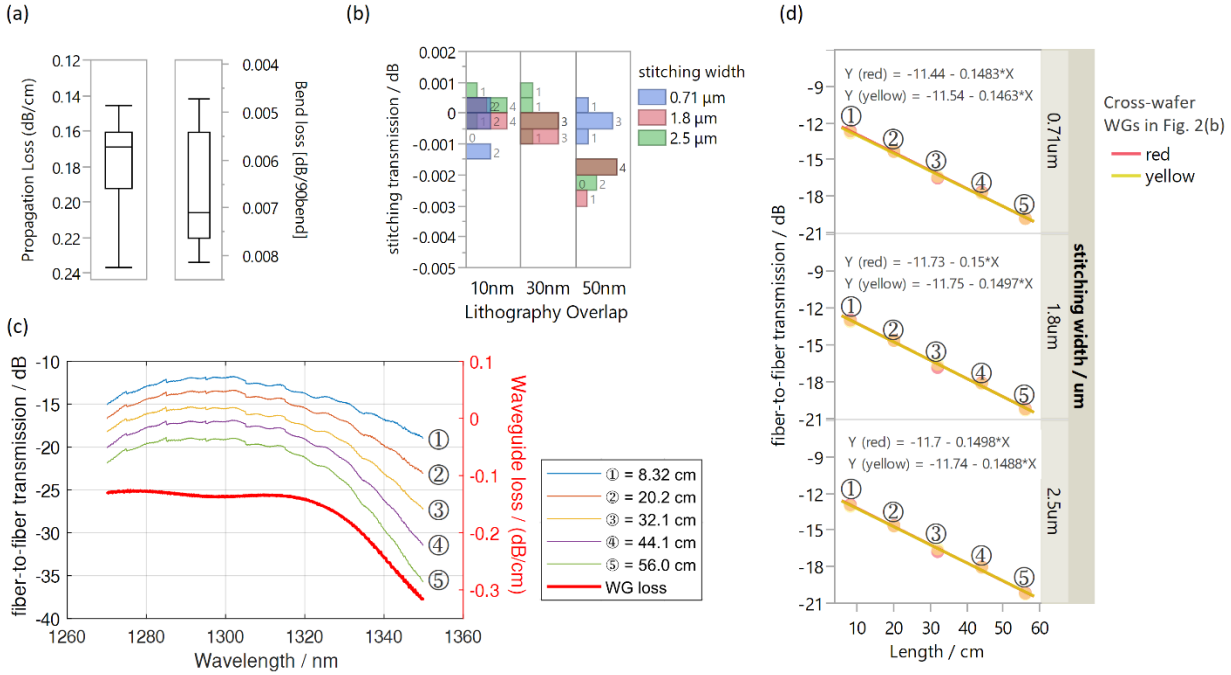


Fig. 3. (a) SiN waveguide propagation loss and 90-degree bend from spiral waveguides on standard test structures across the wafer. (b) Measured stitching loss from test structures vs. lithography overlap and taper width, (c) Measured fiber-to-fiber insertion spectra from cross-wafer loop-back SiN waveguides and linear fitted all-in waveguide loss spectrum (in red), (d) loop-back insertion loss and fitted waveguide loss vs. stitching taper width.

5. Discussion and conclusion

In this paper, we present a 300-mm wafer-level highly-confined LPCVD SiN waveguide technology, featuring low-loss (<0.01dB/interface) and compact (<1µm) reticle stitching interfaces, along with tight bending radii down to 50µm (0.007dB/90-degree bend). Cross-wafer loop-back waveguides of up to 56-cm long are demonstrated traversing 20 dies across the wafer, passing through 20 reticle stitches and 56 90-degree bends at an all-in propagation loss of just 0.15dB/cm at 1310nm wavelength. By leveraging the demonstrated low-loss SiN waveguide technology for wafer-level optical interconnect fabrics, we envisage the realization of future wafer-scale multi-XPU compute systems with unparalleled interconnect bandwidth, energy efficiency and latency.

Acknowledgement
This work was supported by imec's industry-affiliation R&D program "Optical I/O".

References
[1] H. Liu et al., "Lightwave Fabrics: At-Scale Optical Circuit Switching for Datacenter and Machine Learning Systems," in Proceedings of the ACM SIGCOMM 2023 Conference, 2023, pp. 499–515.
[2] M. Khani et al., "SiP-ML: High-Bandwidth Optical Network Interconnects for Machine Learning Training," in Proceedings of the 2021 ACM SIGCOMM 2021 Conference, 2021, pp. 657–675
[3] S. Pal et al, "Architecting Waferscale Processors - A GPU Case Study," 2019 IEEE International Symposium on High Performance Computer Architecture (HPCA), Washington, DC, USA, 2019, pp. 250-263
[4] Tae Joon Seok, Kyungmok Kwon, Johannes Henriksson, Jianheng Luo, and Ming C. Wu, "Wafer-scale silicon photonic switches beyond die size limit," Optica 6, 490-494 (2019)
[5] Warren Jin, Avi Feshali, Mario Paniccia, and John E. Bowers, "Seamless multi-reticle photonics," Opt. Lett. 46, 2984-2987 (2021)