Ultra-Compact and Ultra-Broadband Mode (De)Multiplexer Utilizing an Asymmetrical Coupler with SWG and Cascaded Tapered Waveguide

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Abstract: A 25 µm two-mode (de)multiplexer on a silicon-on-insulator platform is demonstrated. Operating in 200 nm bandwidth, it achieves low insertion-loss (< 0.9 dB), minimal crosstalk (< 18.8 dB), and clear eye diagrams at 64 Gbit/s. © 2024 The Author(s)

1. Introduction

In the context of high-density on-chip interconnects, waveguide mode-division multiplexing (MDM) stands out as a remarkable technique for attaining significant bandwidth scalability. Conventional approaches such as wavelength-division multiplexing (WDM) and polarization-division multiplexing (PDM) have built-in drawbacks. WDM is constrained by the system's limited number of wavelength channels, whereas PDM only offers two degrees of freedom for data handling [1,2].

For an MDM link to be effective, high-performance mode (de)multiplexers are required. These multiplexers have been implemented on the silicon-on-insulator (SOI) platform using a variety of design methods. These approaches include multimode interferometers (MMI) [3], asymmetric Y-junctions [4], asymmetric directional couplers (ADC) [5], and adiabatic couplers [6]. MMI-based couplers have a high fabrication tolerance but a complex structural design and a sizable device footprint. Significant insertion losses are introduced by asymmetric Y-junctions. Broad bandwidth operation and low fabrication sensitivity are two benefits of adiabatic couplers; however, adiabatic mode evolution necessitates a sufficiently long coupling length. Tapered ADCs require longer coupling lengths, regardless of their higher fabrication tolerance. Recent work on mode multiplexers integrating adiabatic couplers with subwavelength gratings (SWGs) has demonstrated compact devices with a broad wavelength range and support for numerous higher-order optical modes. However, their footprint, exceeding 50 µm for a single device, remains a challenge for dense integration, prompting the need for more compact wideband mode multiplexers [7].

In this work, we present an ultra-compact (25 µm) and wideband (200 nm) subwavelength grating (SWG)-based two-mode (de)-multiplexer integrated on an SOI platform. The device attains state-of-the-art performance by employing a novel configuration that combines a cascaded tapered strip waveguide with an SWG-based waveguide. Here, two tapered waveguides are cascaded to effectively phase match shorter and longer wavelengths centered around 1550 nm. Furthermore, the device's performance was evaluated under a non-return-to-zero (NRZ) data transmission link experiment. This is the first system demonstration at 64 Gbit/s speed of an on-chip SWG-based mode demultiplexer on an SOI platform, to the best of our knowledge.

2. Device Design and Operation Principle

Figure 1 depicts the schematic of the proposed multiplexer. This design features an asymmetrical coupler, which consists of an SWG-based single-mode waveguide named "access waveguide" separated by a constant gap (G) from a second single-mode waveguide referred to as the "bus waveguide." The bus waveguide tapers (cascaded) into a multimode waveguide.

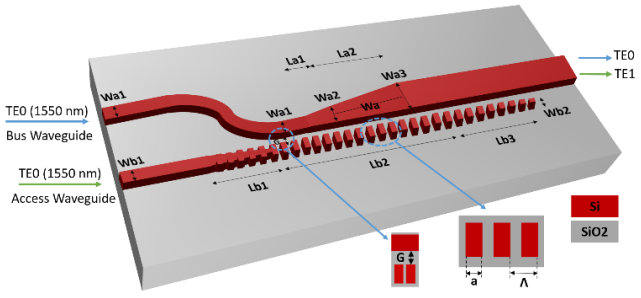

Fig. 1. Schematic of the proposed two-mode multiplexer.

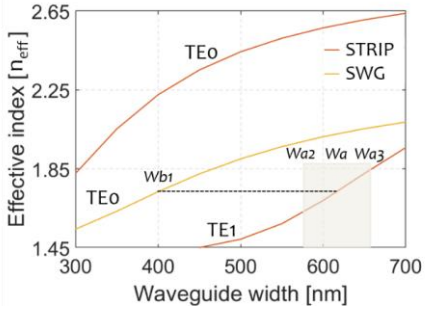

Fig. 2. Effective indices determination with width variation for the bus and access waveguides at 1550 nm.

The functionality of this device relies on mode coupling between the two waveguides, governed by a phase-matching condition. Specifically, the effective refractive index of the TE0 mode in the access waveguide phase matches the effective refractive index of TE1 in the bus waveguide. Simultaneously, the fundamental TE mode injected into the bus waveguide remains TE0 due to a phase mismatch, resulting in minimal crosstalk.

In Figure 2, we illustrate the critical phase-matching condition that must be met between the TE0 mode in the access waveguide and the TE1 mode in the bus waveguide. Specifically, we focus on achieving phase matching at a center wavelength of 1550 nm, where the width of the access waveguide (Wb1) aligns with the width of the bus waveguide (Wa). It's important to note that this phase-matching condition is susceptible to disruption due to even minor variations in the fabrication process. Such deviations are especially problematic in the context of typical asymmetrical directional couplers (ADCs). To address this challenge and enhance the stability and performance of these couplers, we propose the implementation of a multi-section tapered ADC. In this approach, the bus waveguide is tapered in multiple sections, centered around the initially determined phase-matching width. The first section of the strip waveguide in the coupler region is tapered from Wa1 to Wa2 (specifically, 570 nm) over a length of La1 (1 µm). A second section, extending the taper to Wa3 (655 nm) with a length of La2 (4.5 µm), enables phase matching at higher wavelengths. By allowing for a width variation of ±60 nm, we ensure that strong coupling remains achievable throughout the entire L- and C-bands, thereby stabilizing higher-order modes in the waveguide. In the case of the SWG-based waveguide, we select widths of Wb1 (400 nm) tapered to Wb2 (200 nm) and introduce a length of Lb3 (3.9 µm) to prevent back coupling and effectively diffract any remaining light in the single-mode waveguide.

3. Simulations and Measurements

3D FDTD simulations are used to assess the (de)multiplexer performance at a 1550 nm central wavelength. Figure 3 (a) and (b) display the simulated light propagation for a complete multiplexer-demultiplexer link, involving I1/O1 and I2/O2 ports. In this design, light entering I1 maintains TE0 mode across device sections and exits at O1. Light in I2 transitions from TE0 to TE1 and back to TE0 at O2 (causing insertion loss), with any residual light traveling to O1 as crosstalk.

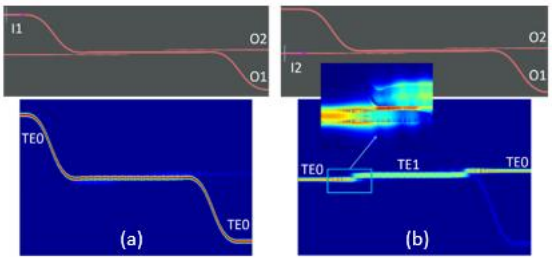

Fig.3. Simulated light propagation at 1550 nm for light coupled to (a) port I1 and (b) port I2.

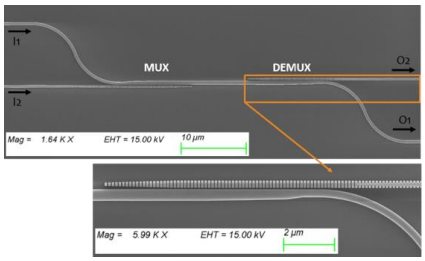

Fig. 4. SEM capture of the fabricated MDM link.

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Table 1. Performance comparison with the literature

Ref	Structure	Length [µm]	Bandwidth [nm]	IL [dB]	CT [dB]
[3]	Cascaded MMI	136	1520-1580	<1.8	<20
[4]	Asymmetric Y-Junction	60	1513-1619	< 0.56	<9.1
[5]	Tapered ADC	68	1525-1590	<1.6	<26
[6]	Adiabatic coupler	260	1460-1640	<1	<13
[7]	AC +SWG	50	1460-1625	<1.9	<15
This work	Cascaded Taper +SWG	25	1450-1650	<0.9	<18.7

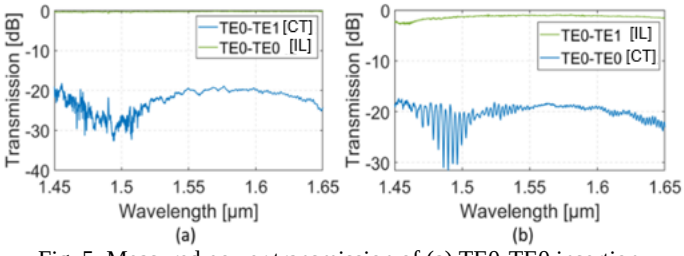

Fig. 5. Measured power transmission of (a) TE0-TE0 insertion loss [I1O1] and TE0-TE1 crosstalk [I1O2], and (b) TE0-TE1 mode conversion loss [I2O2] and TE0-TE0 crosstalk [I2O1].

The two-mode multiplexer was fabricated on an SOI platform with a 220 nm silicon layer and a 2 µm box oxide using the NanoSOI process at Applied Nanotools Inc. Figure 4 presents SEM images of the device. Experimental characterization was conducted through edge coupling. The MDM link, spanning 200 nm around the C-band, demonstrated high performance. At 1550 nm, the TE0-TE0 (I1/O1) insertion loss [IL] and crosstalk [CT] (I1/O2)

measured 0.9 dB and -18.7 dB (refer to Fig. 5a). For TE0-TE1-TE0 mode conversion (I2/O2) and TE0-TE0 crosstalk (I2/O1) [Fig. 5b], the maximum IL and CT were 2.3 dB and -18.6 dB, respectively. Table I provides a performance comparison with similar SOI multiplexers. Notably, our device achieves a compact footprint with a 25 μm length (the entire MDM link [Mux+Demux] spans 55 μm) while maintaining high performance and broadband response. Moreover, our device exhibits a straightforward design with minimal sensitivity to fabrication variations. In contrast, prior mode multiplexers often compromised footprint or bandwidth to improve other metrics.

4. System Demonstration

The fabricated device underwent further comprehensive characterization utilizing an amplitude-modulated signal. This experimental setup is depicted in Figure 6. To generate a NRZ-OOK pseudorandom binary sequence (PRBS) of length 2^{31}-1 at data rates of 40 and 64 Gbit/s, a Keysight 64 Gbaud M8045A pattern generator was employed. The signal modulation of a tunable laser centered at 1550 nm is performed by means of a Thorlabs LN05S 40 gigahertz (GHz) intensity Mach-Zehnder modulator. The modulator was DC-biased at 3.5 V. Furthermore, it was driven by an SHF S807C RF amplifier. To enhance the optical signal's strength prior to its introduction to the silicon chip, a polarization-maintaining booster optical amplifier (Thorlabs S9FC1004P) was incorporated into the setup. Additionally, polarization controllers were positioned both before the modulator and after the amplifier to ensure the maintenance of TE-polarized light throughout the experimental configuration.

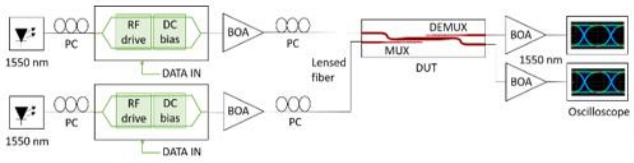

Fig. 6. Experimental setup for on-chip two-mode division demultiplexing

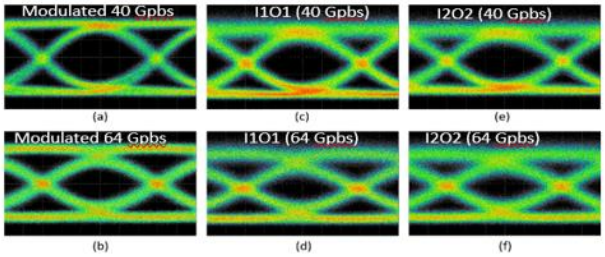

Fig. 7. Captured eye diagrams of the modulated input signal with (a) 40 Gbit/s, and (b) 64 Gbit/s. Eye-diagrams of the demultiplexed signal at I1/O1 insertion loss with (c) 40 Gbit/s, and (d) 64 Gbit/s; and at I2O2 mode conversion loss with (e) 40 Gbit/s, and (f) 64 Gbit/s.

Figures 7 (a) and (b) illustrate the optical input and the subsequently pre-amplified signal, modulated at rates of 40 and 64 Gbps, respectively. Following this initial phase, the output signal undergoes further amplification employing a polarization-insensitive semiconductor optical amplifier (Thorlabs S7FC1013S). The optical signals corresponding to the input/output pairs, designated as I1/O1 and I2/O2 (as illustrated in Fig. 5), are then captured through the application of a Keysight Infinium DCA-X 86100D wide-bandwidth oscilloscope. Figures 7 (c-f) portray open-eye diagrams for each of the demultiplexed signals. These diagrams serve as a clear indicator of the device's performance, characterized by a high extinction ratio.

Acknowledgment

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