# 304 channel MicroLED based CMOS transceiver IC with aggregate 1 Tbps and sub-pJ per bit capability

**Bardia Pezeshki, Suresh Rangarajan, Alex Tselikov, Emad Afifi, Ivan Huang, Jeff Pepper, Sarah Zou, Howard Rourke, Rowan Pocock, Alasdair Fikouras, Farzad Khoeini, Vahid Mirkhani, Steve Novak and Rob Kalman**

*Avicena Tech Corp., 1225 Bordeaux Dr. Sunnyvale, CA 94089 – USA,*
*bardia@avicena.tech*

**Abstract:** 1Tbps 16nm-CMOS transceiver IC with microLED array-based transmitter and hybrid silicon detector array runs at about 1pJ/bit using 304 channels at 3.3Gbps per lane. Initial results are shown for single lane and in various configurations.

## 1. Introduction

Data connections are limiting the performance of advanced computing applications like ML/AI and HPC systems. Their energy efficiency, density, and cost requirements are critical for performance and are pushing the fundamental limits of copper interconnects. Optical interconnects are considered a potential solution to this bottleneck. Silicon photonics (SiPh) links over single mode fiber (generally with external DFB sources) have demonstrated low power results (~5pJ/bit) [1,2]. VCSEL-based links in multimode fibers have demonstrated results down to 1pJ/bit [3], typically with simpler packaging than SiPh. These conventional optical links typically run at many tens of Gb/s over a few lanes and require SerDes on each end.

GaN micro-LEDs (µLEDs), originally developed for displays, have been modulated up to 10Gb/s [4] for Visible Light Communications (VLC) [5-7]. By using arrays of hundreds of these µLEDs on silicon ICs, high capacity and wide data links for chip-to-chip communications can be implemented. Their wide and relatively slow per-lane speed avoids the power consumption and latency associated with SerDes and matches the fundamentally parallel nature of processor and memory buses. Highly parallel optical interconnects have fundamental potential advantages over electrical interconnects in terms of power and crosstalk. The architecture for such links is shown in Fig. 1a.

We previously showed a 32-channel link with each lane operating up to 2Gb/s [8]. We now extend that with a 304-channel link, nominally at 3.3Gb/s per lane with a full digital interface. Initial results are presented for links between ICs and with external reference components. This LightBundle link is capable of 1Tb/s bidirectional with an areal density of 1.5Tb/s/mm$^2$, resulting in the world's smallest and lowest power optical transceiver IC.

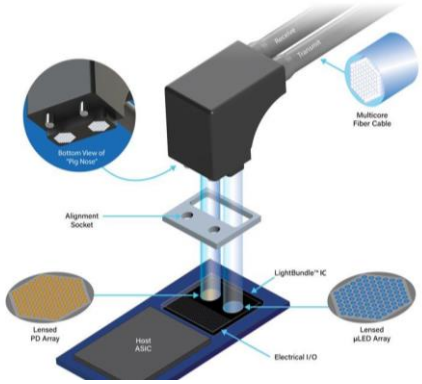


Fig 1a: LightBundle architecture

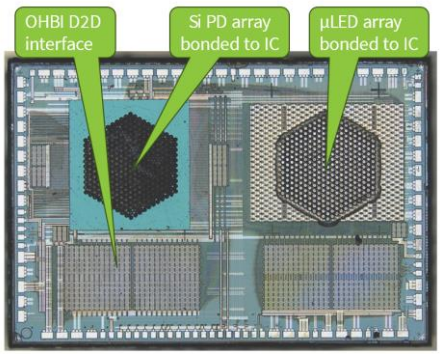


Fig. 1b: Photo of completed 16nm IC

## 2. Transceiver ASIC design

The 2.7mm x 4.2mm transceiver ASIC, shown in Fig. 1b is designed in 16nm finFET process and includes a parallel OHBI interface with each lane running at 6-8Gb/s. Each lane of the electrical data stream is split into two streams to be transmitted optically at half rate (3-4 Gb/s).

On the optical transmit (Tx) side, the chip has 304 active cells where each cell contains a µLED driver with cathode drive and a single tap pre-emphasis stage. A bias current source is connected to the cathode to set the zero level and extinction ratio. The GaN µLEDs are directly mounted on top of the driver circuitry. The chip also contains 304 receiver (Rx) cells, each containing a TIA, LIA and a retimer, including a digital DC offset cancellation circuit. A differential shunt feedback TIA design provides high supply and ground noise immunity. An external photodetector (PD) chip is mounted directly on top of the receive array.

Each Tx and Rx word uses a DLL to align the phases of the incoming data lines. Several built-in self-test (BIST) capabilities are integrated. Each data word is equipped with 2 PRBS generators and a checker to allow for BER measurement in the presence of aggressor signals. An Open Eye Monitor (OEM) allows monitoring of each Rx signal and is accessible through I2C.

## 3. Optical elements

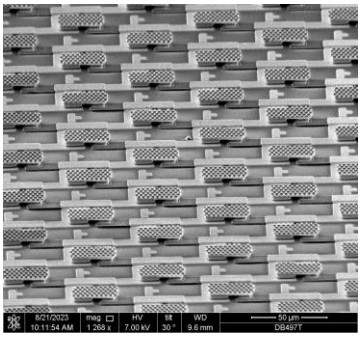

Fig. 2a: uLED array

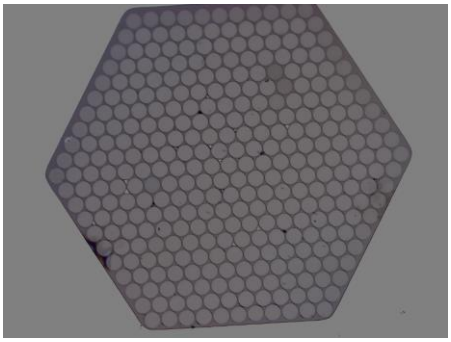

Fig. 2b: End view of fiber array

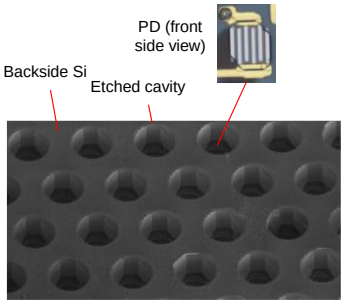


Fig. 2c: Photodetector array

Multiple quantum well (MQW) GaN epi was grown on sapphire and processed into µLEDs operating at ~425nm with an 8µm diameter aperture, using a "lateral" structure with both the n and p contacts on the same side of the chip. 331-element µLED arrays were transferred onto the transceiver ASIC using a standard laser-lift-off (LLO) and laser soldering process originally developed for multi-million-pixel RGB display applications. These types of transfer processes for displays typically achieve 99.99% yields [9] so our 304-element array can achieve extremely high yields. Fig. 2a shows an SEM photograph of the transmitter array on the transceiver ASIC. A microlens array was then stamped onto the array to couple light efficiently into a 0.3 NA multimode fiber.

The fiber connection was a 331-element array of 50µm diameter borosilicate fibers such as are commonly used in lighting fixtures. These fibers were assembled into hexagonal ferrules (Fig. 2b) in a "coherent" manner such that the ordering was the same on both ends. The placement accuracy of the fibers in the ferrules has an x-y standard deviation of < 2µm. MTP/MPO-like fiber cables were fabricated with two 331-element bundles in each connector. The alignment tolerance to the Tx and Rx arrays was measured to be ±7µm to keep crosstalk between adjacent fibers to less than -20dB with both the lensed Tx and Rx. This was both simulated and measured in a DC setup.

Unlike our previous work on a planar 130nm CMOS process, the standard TSMC 16nm finFET process does not readily support high-performance integrated lateral PDs. Therefore, a back-illuminated silicon PD array was developed, producing a 1.2mm x 1.2mm chip with 331 PDs that was flip-chip bonded onto the ASIC. The PDs were fabricated on an SOI wafer with ~1µm thick absorbing silicon layer and ~1µm thick buried oxide layer. Lateral interdigitated p-i-n structures, similar to previous work [10], were realized by phosphorous and boron implantation and metallized for low resistance. The fingers were ~0.8µm wide and spaced 2.5µm apart. To enable light to reach the PDs from the backside, the Si substrate was thinned to ~30µm and ~35µm diameter cavities were etched through the Si, stopping at the buried oxide. The entire PD array was bonded to the ASIC using < 10µm AuSn diameter solder bumps. Much like the LED array, a polymer micro-lens array was stamped on backside of the PD array to optimize optical coupling from the fiber array. The detectors had similar performance to the previous 130nm XFAB process [8].

## 4. Results

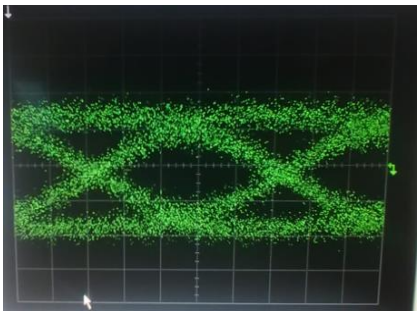

Fig. 3a: Transmit eye at 4Gb/s

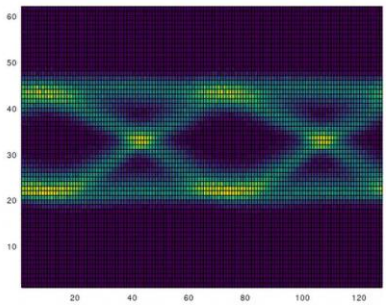


Fig. 3b: Received eye OEM at 3.3Gbps

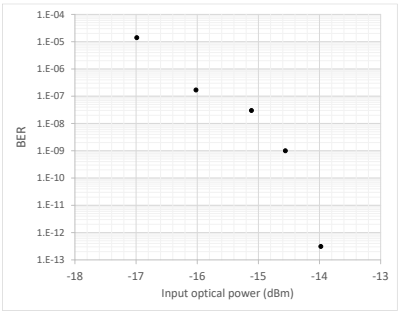


Fig. 3c: BER vs Input power at 3.3Gbps

We first tested the IC with a free-space connection using external Tx and Rx reference receivers. The reference Tx was a directly modulated laser coupled into a lensed fiber. The reference receiver was an Avicena-built detector with a 10Gb/s datacom TIA. Each element of the Tx array could be modulated by the integrated driver up to 1.5mA and showed high speed performance up to 4Gb/s. Fig. 3a shows the RF eye of one of the Tx array channels operating at 4Gb/s. At 3.3Gb/s (the nominal rate for the chip) the link was error-free at a drive current of 0.85mA, which is ~1 pJ/bit for the complete transmitter. At lower currents, and thus lower energy consumption, the error rate increased as expected.

The total power consumption of the receiver, including linear and limiting circuits, was about 0.35pJ/bit at 3.3Gb/s. Using the 420nm reference transmitter, Fig 3b shows the open-eye monitor generated by the ASIC at this speed. Fig. 3c shows the BER reported by the internal monitor as a function of the coupled power. The BER decreases to down to about $10^{-13}$ at about -14dBm of received optical power. The link also closed with the IC on both ends and the fiber bundle in between, but at poorer BER. Data for multi-lane transmission will be presented at the conference.

## 4. Summary

We demonstrate a high density and low power CMOS-compatible fiber interconnect. Initial results indicate the approach is robust, scalable and compatible with the current IC ecosystem. With further device and packaging optimization, power consumption well below 1pJ/bit and bandwidth density of > 10Tb/s/mm$^2$ are achievable.

## 5. References

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