A Partially Etched Silicon Spot-Size-Converter for O Band High NA Fibers

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Abstract: An O band partially etched silicon edge coupler for 3.3 μm MFD fiber is proposed to enhance coupling efficiency and fabrication tolerance. It's experimentally demonstrated with < 1.25 dB/facet coupling loss and <0.1 dB PDL.

OCIS codes: (130.3120) Integrated optics devices; (060.1810) Buffers, couplers, routers, switches, and multiplexers

1. Introduction

Fiber-to-chip coupling has become a critical part of silicon-photonics-based optical engines. Nowadays, edge coupler (also known as spot size converter SSC) is chosen to be the mainstream candidate for most applications due to its broad bandwidth, high efficiency, and low polarization dependence. Although there are numerous research efforts on edge couplers to support standard single single-mode fiber (SMF-28) [1,2], a low-loss scheme with good packaging reliability is still not widely acknowledged. Instead, using fibers with reduced mode field diameter (MFD), such as high NA and lensed fibers, becomes more practical.

Due to its strong birefringence, silicon waveguide is not straightforward to deliver O band SSC with low polarization dependent loss (PDL). The main challenge lies in the inverse taper tip at facet should be close to a square shape in order to provide polarization independent facet modes. However, mainstream SOI cross-section based on 220 nm silicon layer thickness cannot offer a square tip facet to match with even reduced MFD since mode effective area is too small. This would require to use a "smaller" square tip on thinner silicon layer or to build a square tip on modified silicon refractive index. One proven solution is to use a subwavelength silicon structure to reduce birefringence [3], which effectively modify silicon refractive index by tweaking duty cycles. However, such subwavelength structures are composed of multiple isolated pillars whose reliability and cross-wafer uniformity remain questionable [1,2]. Another solution is based on a partially etched silicon taper [4], which uses shallow etch process to create a small square tip with reduced thickness and then it gradually evolves to full thickness single mode waveguide. Nonetheless, mode overlap design becomes restricted since partial etch depth is typically dictated by the foundry, and additionally, the partial etch depth control will strongly affect coupling efficiency.

This paper proposes a trident-shaped partially etched silicon SSC to overcome its predecessors' limitations. It aims to enable a more flexible overlap design to target higher coupling efficiency and, more importantly, solve the etch depth tolerance pain point. Based on a CMOS-compatible SOI platform, our benchmark SSC experimentally achieves 1.25 dB worst-case insertion loss over the O band with a PDL as low as 0.1 dB. A good performance uniformity is demonstrated by the results measured from devices on multiple chips.

2. Si SSC Design

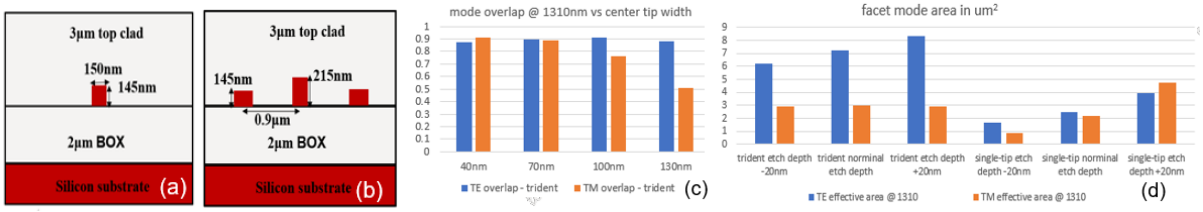

Fig. 1 (a) facet view of conventional single-tip design (b) facet view of trident design (c) mode overlap with 3.3 μm MFD Gaussian spot with varying central tip width (d) mode effective area under ±20 nm etch depth variation

From previous knowledge, using tips of either full silicon thickness or reduced thickness alone cannot offer TE & TM facet modes with similar spot sizes that is also fabrication tolerant. Therefore, we propose to use tips of mixed thickness as shown in figure 1(b). The facet contains a full-thickness silicon tip in the center and two partially etched silicon tips on two sides. Then width of the central tip becomes critical, since a wide tip will once again dominate the mode profile with strong birefringence. With a 70 nm wide central tip and 130 nm wide side tips, the facet demonstrates > 89% overlap with a 3.3 μm MFD Gaussian spot. Figure 1(c) shows the mode overlap @ 1310 nm when only the center tip width changes. It shows the polarization-independent facet matching the MFD target is only

possible when the tip width is relatively small. Hence, 70 nm is chosen here to comply with the DRC rule of a 65 nm node foundry process. It's also interesting to see the mode effective area listed in figure 1(d) that clearly central tip contributes primarily to TM mode on trident design hence the spot size is not affected by etch depth variation.

The SSC taper is based on a two-segment design that in stage 1 central tip width linearly expands to 200 nm and then further expands to 380 nm in stage 2 while side tips keep unchanged. The tip is placed 2 μm away from the edge to comply with the foundry DRC rule. FDTD simulation assumes the facet contains an 85-degree slant angle and a UHNA4 fiber is in intimate contact with the facet. The simulation also uses water as background to mimic the gel used in packaging. As shown in Figure 2, the optical field will initially couple to the facet of the tips with mixed thickness, and then it will gradually couple to the full-thickness central taper as the taper width expands. Figure 2 (b) shows the simulated transmission spectrum, delivering a sub-decibel coupling loss and a 0.3 dB PDL over the entire O band. The impact of ±20 nm partial etch depth is also tested, and the result is quite robust that a less than 1.1 dB/facet worst-case coupling loss can still be maintained. Intimate contact between fiber and facet is not always achieved during actual measurement or packaging. A simulation is done to explore the effect of the extra gap between them. Results indicate that approximately a 0.3 dB extra loss will be introduced with a 2 μm coupling gap.

On the other hand, a conventional single-tip partial etch design [4], is also simulated with the same simulation setup. The simulation results show a 1.45 dB worst-case IL with a nominal etch depth, but TM loss will quickly deteriorate to 2.8 dB when there is a 20 nm over-etch. Hence, from the design point of view, the trident-shaped partially etched SSC indeed shows superb tolerance on etch depth control, leading to superior performance. But it's only applicable to 65 nm node foundry with advanced lithography process.

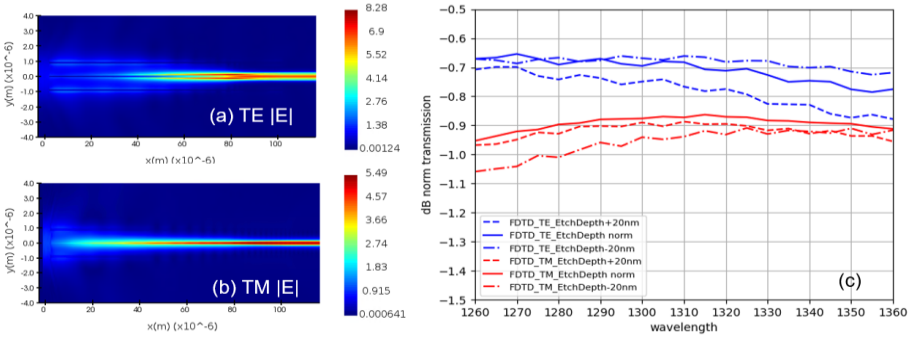

Fig. 2 (a) FDTD simulated |E| of TE input of trident design (b) FDTD simulated |E| of TM input of trident design (c) Calculated transmission under ±20 nm etch depth variation

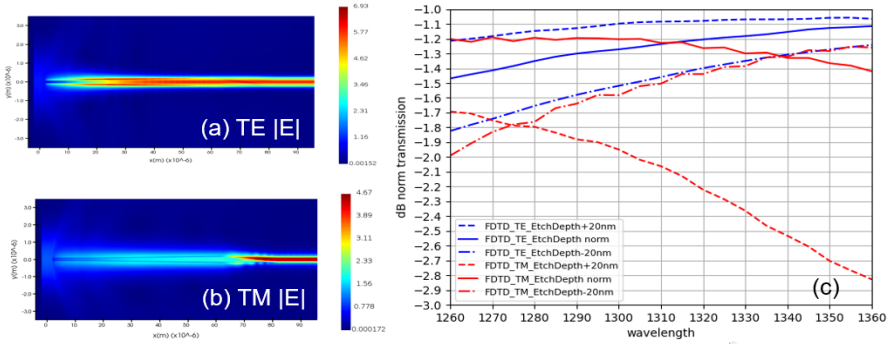

Fig. 2 (a) FDTD simulated |E| of TE input of single-tip design (b) FDTD simulated |E| of TM input of single-tip design (c) Calculated transmission under ±20 nm etch depth variation

3. Fabrication and Measurement

The SSC is fabricated on a passive short-loop wafer flow at a commercially available 12-inch foundry. For testing, two identical SSCs are deployed on left and right edges with routing waveguide connecting in between (contributes to ~0.3 dB propagation loss). UHNA4 fibers are spliced with SMF-28 fibers to form fiber arrays with 0.35 dB loss per splice. A Keysight Tunable laser injects a beam passing through a polarization controller, and then it's connected to the fiber under test. Two fiber arrays are used on both edges as input and output, respectively. The optical coupling is done by an in-house developed automatic coupling stage based on a spiral algorithm. The coupling is first carried out in the air, and then water is dipped on the chip to mimic the effect of the packaging gel. The polarization is manipulated to record the maximum and minimum power transmission spectrum.

Figure 4 shows the characterized coupling loss spectrum of an identical trident-shaped partially etched SSC from 3 chips. The loss is characterized by using power before the input fiber as a baseline, while the splicing loss and the waveguide propagation loss are calibrated out from the link budget. The measured spectrum is plotted together with the simulated loss with a 2 μm coupling gap, which also complies with packaging accuracy. The SSC of the best-performing chip shows the worst-case 1.25 dB/facet coupling loss and a PDL as low as 0.1 dB. Other chips show similar metrics that the worst-case coupling within 1.4 dB together with 0.1 dB PDL is obtained. Noticeably, the TE loss increases (around 0.3 dB) to become comparable with the TM. This additional loss is most likely to originate from the sidewall roughness induced scattering, where the TE polarization mode becomes more lossy [5].

The performance of a conventional single-tip partially etched SSC is also experimentally evaluated. Figure 5 (a) shows the characterized transmission spectrum of the best-performing chip, where a 1.9 dB/facet worst-case coupling loss and a 0.25 dB PDL are measured. It shows the performance of our trident design surpasses that of the single-tip design, even on the best die. Overall multi-die metrics are plotted in figure 5(b). It's clear that the conventional single-tip design indeed shows larger die-to-die variation.

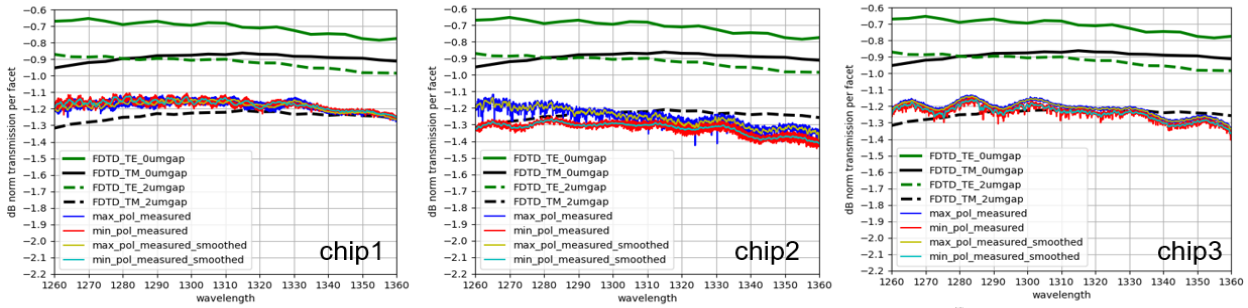

Fig 4. Characterized coupling loss spectrum of identical trident design from 3 chips

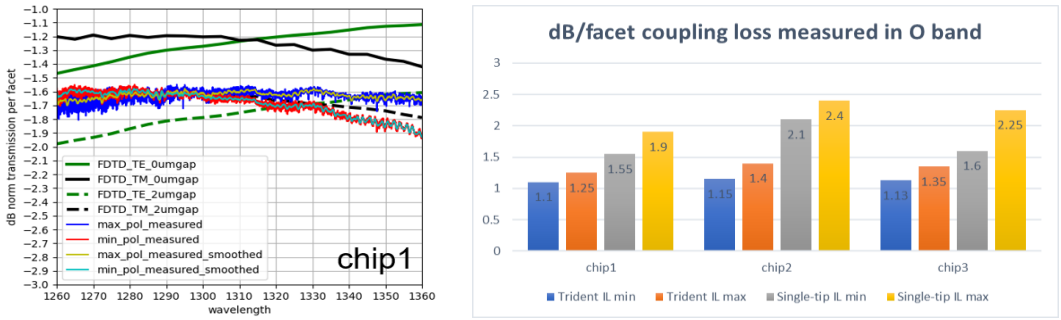

Fig 5. (a) Characterized coupling loss spectrum of single-tip design (b) overall metrics die-to-die comparison

4. Summary

In summary, a partially etched Si SSC for O band high NA fiber is explored and demonstrated. The conventional approach based on single-tip shallow etch Si taper cannot achieve desirable etch depth tolerance. This paper proposes a novel trident-shaped Si taper, which anchors the facet mode to a combination of full-thickness and partial-thickness tips. This design is more robust against etch depth variation at the cost of a stringent minimum feature size requirement. We experimentally show such a design is able to deliver 1.4 dB coupling loss + 0.1dB PDL for O band coupling to UHNA4 fiber, on multiple chips fabricated at a 12-inch fab. Its overall performance and die-to-die variation are notably superior to conventional single-tip counterparts. Therefore, this work offers a favorable solution to deliver O band high NA fiber edge coupling for foundry with a high-resolution lithography.

5. References

[1] T. Barwicz, *et al*., "An O-band Metamaterial Converter Interfacing Standard Optical Fibers to Silicon Nanophotonic Waveguides", OFC 2015, paper Th3F.3
[2] B. Peng, *et al*., "A CMOS Compatible Monolithic Fiber Attach Solution with Reliable Performance and Self-alignment", OFC 2020, paper Th3I.4
[3] P. Cheben, *et al*., "Broadband polarization independent nanophotonic coupler for silicon waveguides with ultra-high efficiency", Opt. Express, **23**, (2015)
[4] A. Dewanjee, *et al*., "Experimental Demonstration of A High Efficiency Compact Bilayer Inverse Taper Edge Coupler for Si Photonics", IPC 2016, paper TuG2.2
[5] M. Teng, *et al*., "Effect of waveguide surface roughness on the fiber coupling efficiency of inverse tapers", OFC 2015, paper Th3F.6