Demonstration of real-time receiver for 30-GBaud PAM-6 signal in IM/DD system

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Abstract: Using baud-rate timing recovery algorithm and a simple blind synchronization method, we experimentally demonstrate a real-time reception of 30-GBaud 6-level pulse amplitude modulation (PAM-6) signal with a baud-rate analog-to-digital converter (ADC). © 2022 The Author(s)

1. Introduction

To meet the growing demand of Internet applications (e.g., 5G, virtual/augmented reality, and online video conference), the capacity requirements of transmission in optical access network and datacenter interconnects (DCIs) increase rapidly. High-dimension modulation formats with coherent transceivers have been widely investigated to extend the net rate as well as transmission reaches. However, with the advantages of low cost, small footprint and low power consumption, intensity modulation direct detection (IM/DD) systems still occupy a dominant position in short-reach communication. Currently, the deployment of 400-GbE has been put on agenda and 200-Gbps/λ is showing to be the most promising way for 800-GbE and beyond. To cope with the rapidly growing data traffic, the main challenge is to achieve maximum data throughput with bandwidth-limited electronic front-ends. A real-time receiver with minimal oversampling rate and high spectral efficiency could lower the demand on sampling rate of the analog-to-digital converter (ADC), which is thus the most essential technique to optimize receiver resource utilization and to reduce power consumption. Traditional real-time receivers usually work at 2 samples/symbol to realize timing recovery and equalization. Recently, with the help of digital interpolation, real-time DSP has been realized and transmission of 50-Gbps/λ PAM-4 signal over 25-km span length has been demonstrated using ADC operating at 1.6 samples/symbol [1]. Moreover, applying signal processing in the frequency domain with an over-sampling rate of 8/7, a real-time receiver for 28-GBaud PAM-8 signal has been reported [2]. In that experiment, the bit-error-ratio (BER) is relatively high which cannot reach the 20% soft-decision forward error correction (FEC) threshold. Since much higher signal-to-noise ratio (SNR) is required in PAM-8 than PAM-4 to achieve required BER, its achievable bit rate is limited. To further reduce the oversampling rate, with baud-rate timing error detector, J. Verbist et al employed pre-equalization at the transmitter side and realized real-time transmission of 64-GBaud PAM-4 signal sampled at 1 sample/symbol in a 1-km scenario [3]. However, the spectral efficiency is still limited. Compared to PAM-4/8 signals, PAM-6 modulation format would be able to balance the required SNR and achievable spectral efficiency, thus has drawn significant interest. Nevertheless, PAM-6 modulation format requires extra mapping and demapping process, since it is not an integer power of 2. To cope with this problem, a 32-QAM constellation-based mapping rule has been proposed to generate PAM-6 signal [4]. However, it is necessary to propose an effective way for synchronization at the receiver side.

In this paper, we report the first real-time reception of 30-GBaud PAM-6 signal with baud-rate sampling ADC based on field programmable gate array (FPGA). Applying baud-rate timing recovery and our proposed blind symbol synchronization method, 75-Gbps net data rate has been achieved under hard-decision forward error correction (HD-FEC) with a pre-FEC BER threshold of 3.8e-3.

2. Receiver architecture

Fig. 1(a) shows the picture of the real-time receiver. The input signal is first converted to the digital domain through a self-made 6-bit ADC operating at 30-GSa/s with ~16-GHz bandwidth. The information of sampled waveforms is then sent to FPGA (Xilinx, XCVU13P) by 24 high speed de-serializers. Signal processing techniques including channel imperfection compensation, digital timing recovery and symbol demapping are implemented in FPGA. Cooperating with a voltage-controlled oscillator (VCO, 10 MHz) and phase locked loop, the sampling clock source generates 15-GHz clock synchronized with the input signal under the control of a 16-bit digital to analog converter (DAC). The recovered binary data as well as intermediate data during processing could be obtained by integrated logic analyzer (ILA).

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Fig. 1(b) shows the details of the function blocks in our real-time receiver. Working at 234.375 MHz, the signal is processed with 128 parallelization channels (30GHz/234.375MHz=128). To realize 48 taps feed-forward equalizer (FFE) and Mueller-Müller timing error detector (MMTED), the data buffer aligns the input digital waveform, then passes 128 samples in parallel to the linear equalizer and timing recovery module. Finally, the original 32-QAM symbols are regained with blind symbol synchronization algorithm and de-mapped into binary data.

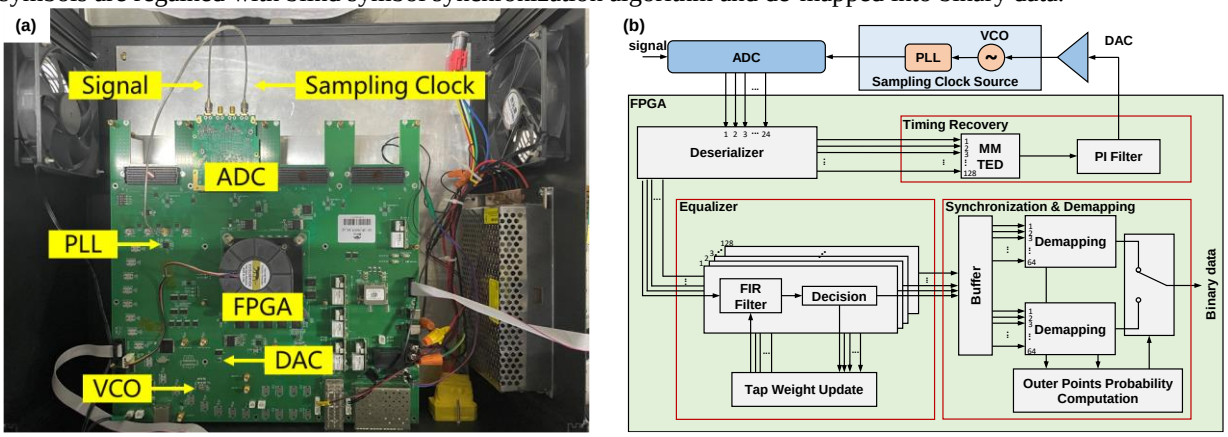

Fig.1. (a) Picture of the real-time receiver consists of ADC, sampling clock and FPGA. (b) Details of the DSP and hardware design.

Timing recovery is an essential part of the overall design. We implemented the timing loop with phase-locked loop controlled by a digital timing recovery algorithm. In order to squeeze the capability of ADC, digital MMTED operating at baud rate is utilized here instead of traditional oversampling TEDs. For the purpose of stabilizing the timing loop, a digital proportion-integral (PI) filter is placed following the TED to mitigate the out-band noise of recovered timing information. The filtered signal is then sent to the DAC to control the VCO and thus lock the sampling phase of the ADC. In addition to synchronizing the sampling clock with input signal, channel imperfection compensation is another important task. To mitigate severe inter symbol interference, linear equalizer is adopted with T-spaced 48-tap FFE structure. The filter coefficients are updated in blind mode with decision-directed least mean square algorithm (DD-LMS). In order to reduce the usage of multipliers, sign-sign LMS adaptation algorithm is implemented to the recovered symbols and decided symbols of 128 parallel FFE blocks in each circle [5].

The maximum information rate of PAM-6 signal would be $\log_2(6) = 2.585$ bits/symbol. However, tedious coding and decoding process would be then introduced. In this work, the constellation of 32-QAM is used to generate the PAM-6 signal. At the transmitter side, each 32-QAM constellation point is generated with 5-bits and then mapped into two PAM-6 symbols. In such an approach, symbol synchronization is indispensable at the receiver side. An alternative way to synchronize the symbol is to insert known symbol stream. However, the spectral efficiency would be reduced accordingly. In this paper, we apply a simple and effective method to align the 32-QAM constellation points. PAM-6 signal from linear equalizer are buffered and fed into two channels with different starting positions. Every two symbols build up a QAM point. The constellation of the unsynchronized channel would behave as a 36-QAM diagram and the probability of 4 outer points appears to be about 1/16 in independent and equiprobable distributed PAM-6 sequences. To align the PAM-6 symbols into 32-QAM constellation, the probability of outer points is real-time calculated and updated by $P_n = P_{n-1} \times (1-\alpha) + P_o \times \alpha$, where P_n is the probability, α denotes update coefficient and is set to 1/128, and P_o is the probability of outer points in a single cycle for 64 parallel paths. The channel with minor P_n is selected to output binary data.

Table 1. Utilization of FPGA resources

Key Blocks	LUT	Register	DSP Block
Equalizer	223396(12.9%)	303469(8.8%)	6144=128×48(50%)
Timing Recovery	9337(0.5%)	14668(0.4%)	0
Synchronization & Demapping	7466(0.4%)	19138(0.6%)	0
Total	259319(15.0%)	364989(10.6%)	6144(50%)

Table 1 shows the utilization report of the key blocks and total implemented resources. With continuous time linear equalizer and much reduced number of parallel lanes, the DPS blocks could be shrunk in the ASIC design. It

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is worth to point out that the block random access memory (BRAM) is used only during the ILA data acquisition and is thus not listed.

3. Experimental setup and results

The experimental setup is depicted in Fig. 2(a). DSP at the transmitter side are offline realized in MATLAB. A pseudo random binary sequence (PRBS) is used as data and then mapped into 32-QAM signal. By interleaving the I and Q components, the PAM-6 symbols are obtained. Signal quality is improved by replacing equal-spaced PAM-6 signal with unequal-spaced PAM-6 signal [6]. The signal is then resampled and sent to arbitrary waveform generator (AWG, Keysight M8195A, ~25-GHz 3 dB bandwidth) operating at a sampling rate of 60-Gsa/s. A continuous-wave laser is used here as the optical source. Mach-Zehnder modulator (MZM, Fujitsu FTM7938EZ, ~25-GHz 3dB bandwidth) upconverts the signal from electrical domain to optical domain. At the receiver side, a variable optical attenuator (VOA) is utilized to adapt the received optical power (ROP). A photodiode (PD, Finisar XPDV2120RA, ~40-GHz 3dB bandwidth) is applied to detect the signal, which is then captured and recovered by the designed real-time receiver.

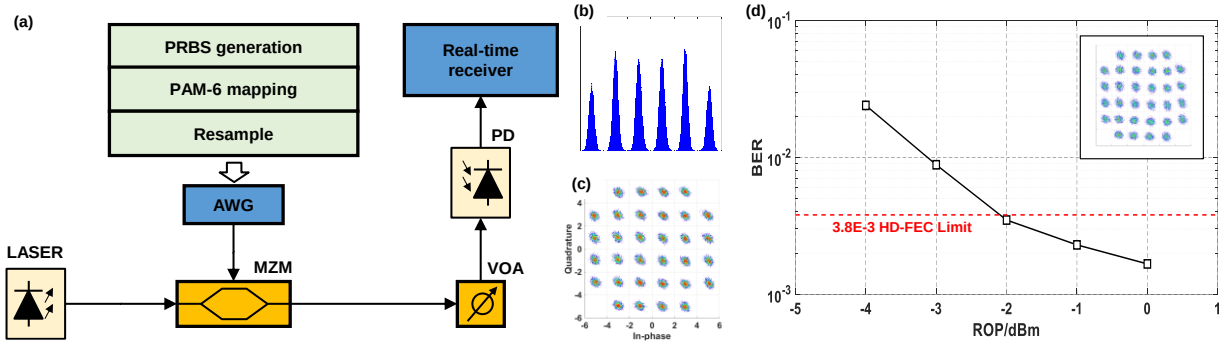

Fig.2. (a) Experimental setup. (b) Histogram, and (c) 32-QAM Constellation of PAM-6 signal in electronical back-to-back measurement. (d) BER measurements of 30-GBaud PAM-6 signal.

Fig. 2(b) shows the normalized histogram of PAM-6 signal after equalization. After symbol synchronization, the PAM-6 signal could be presented by 32-QAM constellation as depicted in Fig.2 (c). The diagrams clearly show that our proposed receiver architecture realized real-time signal synchronization and recovery. The experimental results in optical back-to-back channel are shown in Fig. 2(d). We measured the BER performance versus ROP. About 1.6×10^5 bits are used for BER counting in our experiment. BER of 1.67e-3 is achieved at 0 dBm, and the receiver sensitivity at HD-FEC limit is lower than -2 dBm. Received PAM-6 signals with ROP at 0dBm is presented by 32-QAM constellation diagram and displayed in the insert figure.

4. Conclusion

We experimentally demonstrate the first real-time reception of 75-Gbps PAM-6 signal in optical IM/DD system with single channel ADC operating at 30-Gsa/s. Error-free threshold of HD-FEC with 7% overhead is achieved under -2dBm receiver sensitivity. With higher bandwidth electronical and optical chips, the line rate could be further extended to be deployed in high-capacity short reach communications.

Acknowledgements

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