Highly Optimized O-band Si Ring Modulators for Low-Power Hybrid CMOS-SiPho Transceivers

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Abstract: We present O-band Si ring modulators with up to 58pm/V electro-optic and 610pm/mW thermo-optic modulation efficiencies and >24GHz modulation bandwidth, enabling a hybrid CMOS-SiPho transceiver with error-free operation at 40Gbps NRZ with <4pJ/bit link energy.

1. Introduction

Over the past decade, Silicon Photonics (SiPho) has emerged as a key enabling technology for datacenter optical interconnectivity and is now considered to enable high-bandwidth optical interconnect networks in future HPC and machine learning systems [1]. The compute nodes in such systems will require multi-Tbps optical transceivers with low power (<5pJ/bit) and low bit-error ratio (BER<1e-12) at low link latency. Ring-based SiPho transceiver architectures have shown great potential to realize such performance metrics, leveraging wavelength-division multiplexing (WDM) to scale aggregate bandwidth at relatively modest lane rates in the range of 16-64Gbps NRZ, without requiring power-hungry forward-error correction (FEC) for error-free operation, as demonstrated previously in monolithic [2] and hybrid integrated EIC-PIC transceiver prototypes [3-5]. As the power consumption of Si ring-based optical links is often dominated by thermal tuning and laser power, it is essential to optimize the electro-optic and thermo-optic modulation efficiency of the employed Si ring modulators (RM) at the same time. In this paper, we report Si ring modulators combining best-in-class electro-optic and thermal-optic efficiency, through in-depth optimization of the vertical p-n phase shifters and implementation of a local Si-substrate undercut process improving the efficiency of the integrated heater. As a proof-of-concept, the optimized Si ring modulators are implemented in a hybrid flip-chip FinFET CMOS-SiPho WDM transceiver prototype, showcasing error-free operation (BER<1e-12) at 40Gbps NRZ with ~3.5pJ/bit link energy, including the laser and thermal tuning power.

2. Ring modulator optimization

Over the past several years, Si ring modulators have been optimized to operate at higher modulation bandwidths, e.g., targeting 200Gbps PAM-4 lane rates as required with future Ethernet standards [6, 7]. However, increasing the RM bandwidth to 50GHz typically degrades the optical loss and/or requires higher drive swing, resulting in higher required driver and laser power. Fig. 1(d) shows the transmitter penalty (TP = 2 P_{IN}/OMA) and bandwidth for several recently reported RMs, when driven with 1Vpp, and with modulation bandwidths without exploiting optical peaking effects. RMs with vertical p-n junctions (VPN) have been successfully adopted [6, 8] to improve the TP-BW trade-off, and typically have ~2dB lower optical loss compared to LPN RMs. In our current work, we extend the VPN RM design concept to reduce the TP also at lower modulation bandwidths, as desired for low-power, low-latency WDM optical interconnects running at lower (NRZ) lane rates. Following the VPN junction and RM design optimization, a 5um-radius RM is realized operating at 1310nm wavelength with 24GHz bandwidth and a minimum TP of just 7.4dB from 1-V_{pp} drive swing, as shown in Fig. 1(b) and Fig. 1(c).

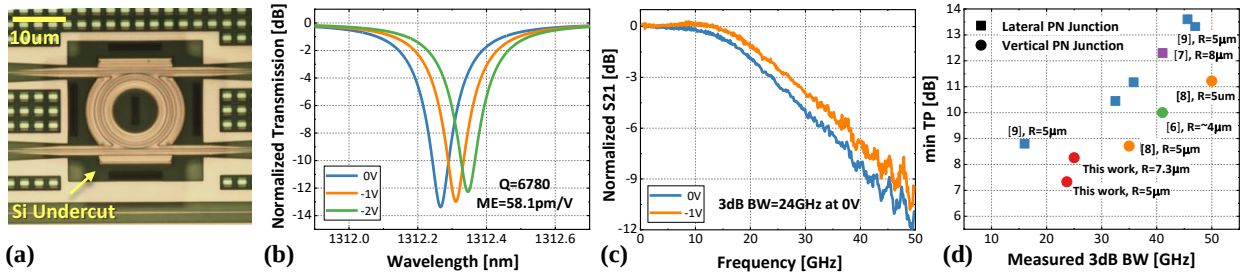

Fig. 1. (a) Microscope image of a RM with Si undercut (before metallization). (b) Transmission spectra and (c) frequency response for a VPN-RM with R=5um vs. E-O bias voltage. (d) Minimum TP vs. E-O bandwidth for best-in-class RM's.

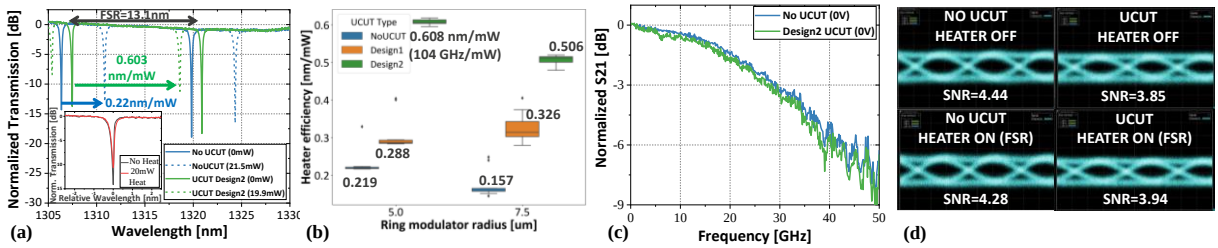

Fig. 2. (a) RM transmission curves for different heater powers with and without UCUT. (b) RM heater efficiency for different radii and undercut designs. (c) LPN-RM E-O frequency response and (d) 50-Gb/s NRZ eye-diagrams without and with UCUT.

Next, to increase the thermal tuning efficiency of the RM, we introduce a silicon substrate undercut (UCUT) process, which locally removes the silicon substrate below the 2-um buried oxide to improve the thermal isolation of the RM tungsten heater. The UCUT processing module is carried out after the SiPho active device formation but before the heater and BEOL metallization steps, and results in a sealed air/vacuum cavity below the RM, as shown in Fig. 1(a). It is fully compatible with subsequent micro-bumping and underfill processes, as required for hybrid flip-chip integration with a CMOS chip. The UCUT process was implemented in a 200mm SiPho process flow, both on optimized LPN and VPN-type ring modulators. Fig. 2(a) shows typical transmission curves of the "no-UCUT" RM and a "design2" UCUT RM with 5um radius. Each device was measured on more than 10 dies across the 200mm wafer. Fig. 2(b) shows the heater efficiency of Si RMs with two different radii (5 and 7.5um) and two different UCUT designs with partial ("design 1") and complete undercut ("design 2"). The 5um radius RM has the highest heater efficiency of 0.61nm/mW after UCUT, which is a 2.7x improvement as compared to the same RM without UCUT. As expected, the RM with 7.5um radius has worse heater efficiency (0.51nm/mW) but sees a higher improvement of 3.2x with UCUT adoption. To check for a possible effect of the UCUT module on RM performance, we measured the static RM transmission curve (inset of Fig. 2(a)) and made a relative comparison for heater powers of 0 and 20mW, showing no significant change in resonance and quality factor (Q). In addition, we verified the modulation bandwidth of a 5um radius LPN RM with and without UCUT as shown in Fig. 2(c). No significant change in 3dB bandwidths was observed, with 29.1-, 27.8-GHz measured without and with UCUT, respectively. Finally, Fig. 2(d) show 50-Gb/s NRZ PRBS31 eye-diagrams with 1.6-V_{pp} electrical driving signal for different devices with the heater dissipating 0mW, 62mW (without UCUT) and 0mW, 20mW ("design 2" UCUT) power (reaching a full FSR spectral shift). Again, no significant change in eye-diagram quality such as signal-to-noise ratio (SNR) was observed when applying the UCUT module and turning on the heater to tune a full FSR. In conclusion, the UCUT improves heater's efficiency without any sacrifice of the RM's modulation performance.

3. Low-power hybrid CMOS-SiPho transceiver

3.1 Test chip design, flip-chip assembly and packaging

In order to showcase the potential of the optimized VPN-UCUT ring modulators, we implemented them in a SiPho WDM transceiver test chip along with fiber grating couplers, ring-based demultiplexing filters and high-speed Ge photodetectors (0.94A/W responsivity) at the receiver (RX) side. On the transmitter (TX) side, a VPN-RM with UCUT ("design 1") and radius of 7.3um was chosen to accommodate up to 8 wavelengths with 200GHz channel spacing. The test macro reported here included four cascaded RM wavelength channels, adding 0.8dB insertion loss. The SiPho chip was co-designed with a previously reported FinFET CMOS chip, including 1.3Vpp RM driver and transimpedance amplifier (TIA) arrays optimized for power-efficient operation at 40Gbps NRZ [4, 5]. After SiPho wafer processing and dicing, the FinFET die is flip-chip assembled onto the SiPho die through the 50-µm pitch Cu microbumps. Afterwards, the CMOS-SiPho assembly is glued on a test printed-circuit board and wirebonded for ground and power supplies (Fig. 3(a)). Finally, a SMF V-groove array is actively aligned and glued to the assembly, achieving 3.65dB fiber-to-chip coupling losses at peak wavelength. After assembly, the tuning efficiency of the RM was measured to be 0.17nm/mW, which is lower than the stand-alone RM (0.32nm/mW), but still ~50% higher than in our previous demonstrator without UCUT [4]. This is likely caused by heat sinking through the bonded CMOS chip, as suggested by thermal modeling. Further design improvements of the SiPho TX BEOL wiring are expected to mitigate this efficiency reduction. On the RX side, double-ring-based filters with UCUT can be efficiently tuned (0.54nm/mW per ring) and add 0.6dB insertion loss.

3.2 Measurement results

Fig. 3(b) illustrates single-lane TX and RX performance. To characterize the RM E-O TX, CW light from an external tunable laser was coupled into the SiPho chip. An external bit-pattern generator and tester were used to generate and analyze the PRBS data streams. RF probes were used to feed the electrical signals into the SiPho chip, as shown in Fig. 3(c). With 9 dBm nominal fiber-referred laser power, the RM shows a fiber-coupled OMA of about -3.4 dBm up to 40 Gbps NRZ, with an extinction ratio greater than 5dB and SNR of 7. The energy efficiency is independent of the data rate at 170 fJ/bit [5]. To test the O-E RX, an external LiNbO Mach-Zehnder modulator is used to generate an NRZ optical reference signal with ER ≈ 15 dB. We achieved wide-open eye diagrams up to 44 Gbps. The TIA and limiting amplifier consume 270 fJ/bit with 0.79 ps RMS jitter and 13.8 SNR of 13.8 with -6 dBm OMA at the photodetector.

Finally, a loop-back link between the TX and RX achieved an open eye up to 40 Gbps NRZ with fiber-referred laser power of 8.8 dBm. Fig. 3(c) illustrates the measurement setup for the loop-back measurement. 8.8dBm laser power is coupled into the SiPho chip, resulting in -3.4 dBm fiber-coupled OMA at the TX output. With 0.7dB link loss, the modulated light is coupled back into the RX. The resulting 40Gbps electrical eye diagram recorded at the RX output (Fig. 3(d)) is wide open with 5.7 SNR. In addition, an initial BER measurement was carried out at 40Gbps NRZ: one bit error was recorded for 3.14T transmitted bits, resulting in a BER of 3.2x1e-13. Assuming a fiber-referred laser wall-plug efficiency of 10% and a temperature range of 60 degrees C, we estimate the laser power consumption to be 1.9pJ/bit, and thermal tuning power of 0.71pJ/bit (TX) and 0.38pJ/bit (RX). As such, the optical link is expected to operate with ~3.5pJ/bit power consumption, excluding clocking and data recovery.

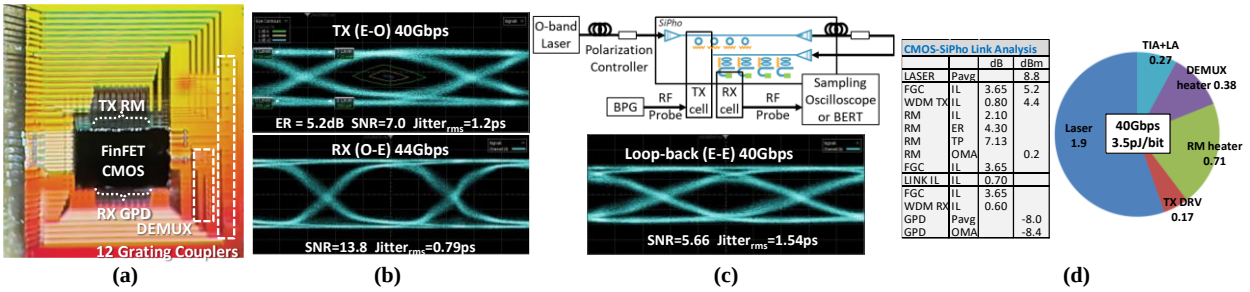

Fig. 3. (a) Microscope image of the flip-chip FinFET CMOS-SiPho transceiver prototype. (b) Separately measured TX and RX eye diagrams at 40-44Gbps NRZ. (c) Simplified test schematic (BPG = bit pattern generator, BERT = BER tester), and measured E-E loop-back eye diagram at 40Gbps NRZ. (d) Measured power consumption breakdown and link budget analysis (FGC = fiber grating coupler, GPD = Ge photodetector).

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