Real-Time Demonstration of a Low-complexity PS Scheme for 130Gb/s WDM-OFDM-PON

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Abstract: We experimentally demonstrated a low-complexity probabilistic shaping scheme in a real-time 16QAM-OFDM-based WDM-PON. The PS-OFDM signal with a net rate of 131.88-Gb/s transmission over 25-km SSMF can be achieved with the BER less than 3.8×10^{-3}.

1. Introduction

With the rapid growth of bandwidth requirements such as cloud computing, big data and virtual reality, current communication systems are confronting severe challenges in improving transmission rates and capacity. Since WDM-OFDM-PON has the advantages of large bandwidth and low delay, it is considered as a promising technology for future heterogeneous access networks with large channel rate [1-2]. In recent years, many low-cost and high-capacity transmission schemes with real-time reception for IM-DD-based OFDM have been proposed [3-5]. Furthermore, recent research results suggest that probabilistic shaping (PS) technology has significant advantages in improving the optical SNR tolerance, extending the transmission distance and supporting flexible spectral efficiency [6]. At present, some research results on PS schemes have been reported, such as Gallager many-to-one (MTO) mapping [7], hierarchical DM (HiDM) [8] and constant composition distribution matching scheme (CCDM) [9]. The MTO shaping method requires the deployment of a joint iterative scheme at the receiver, which applies the outer iteration between the PS demapper and the LDPC decoder in addition to the inner iteration in the LDPC decoder. This means that the solution comes at the cost of computation time, memory and power consumption, and has high hardware implementation complexity. Furthermore, for applying a symbol-level CCDM, the labels representing the desired probabilities still need to be converted/mapped into binary sequences to be compatible with cascaded LDPC-based FEC coding and higher-order modulations. Therefore, the computational complexity and the difficulty of hardware implementation will increase significantly. Compared with MTO and CCDM, HIDM does not require complex high-precision computation, but requires complex binary tree structures. In [6], a simple PS scheme based on bit-weighted distribution matching was first proposed. The proposed PS scheme has the advantages of lower computation and hardware complexity, and only relies on bit-class processing.

In this work, a low-complexity PS-16QAM-OFDM transceiver based on intra-symbol bit weight distribution matching (Intra-SBWDM) (referenced from [6]) is investigated over 25-km SSMF with real-time reception for WDM-PON. 131.88 Gb/s PS-16QAM-OFDM signal transmission is achieved with the BER under 3.8×10^{-3} after real-time reception.

2. PS-16QAM architecture based on Intra-SBWDM

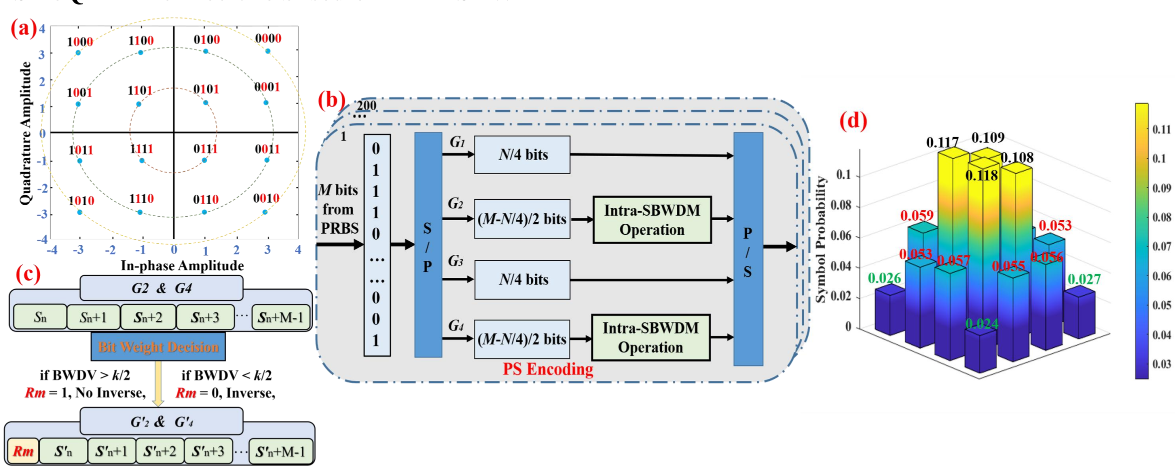

Fig. 1. PS architecture (a) The constellation labeling design, (b) PS encoding, (c) Intra-SBWDM example of $k = 4$, (d) Probability distribution constellation example of $k = 4$.

The principle of PS-16QAM based on Intra-SBWDM is shown in Fig. 1. The 16QAM uses Gray mapping rules, as shown in Fig. 1(a). The red bits are PS-encoded amplitude bits, and the black bits are non-PS-encoded sign bits. Fig.

1(b) elaborates PS encoding processes based on Intra-SBWDM. Firstly, the serial M bits, which are the number of bits contained in one clock cycle before PS encoding, from PRBS ROM are divided into four parallel sequences, G_1, G_2, G_3 and G_4. The lengths of G_1, G_3 and G_2, G_4 are $N/4$, $(M\text{-}N/2)/2$ respectively. N is the number of bits contained in one DMT symbol after PS encoding. $N = N_{sc}*\log_2 16$, N_{sc} is the number of data subcarriers. Then, G_2 and G_4 are bit-wise divided into groups of k bits each, weighted according to their original k elements. One more bit is introduced as the newly-added effective weight bit (EWB) in each set. Through the bit weight decision operation, if the bit weight decision value is greater than $k/2$, the corresponding EWB (R_m) is defined as '1', and the original k elements remain unchanged. Otherwise, the EWB is set to '0', and the bit inversion operation will be performed on the remaining k bits in the set. In this way, the probability of '1' in the G_2 and G_4 will be significantly increased, and the probability of constellation points mapped in the inner circle of the constellation diagram will be significantly improved after series-to-parallel conversion. Fig.1(c) shows the example of k = 4 for Intra-SBWDM operation, in which R_m refers to the EWB. The probability distribution constellation for PS-16QAM based on Intra-SBWDM is shown in Fig. 1(d). In our experiments, the number of N_{sc} is 48, the value of k is 4, 5, 6 and 7. PS encoding is performed once per clock cycle, one frame of PS-encoded DMT symbol can be implemented for 200 clock cycles. It is worth noting that when k is 4, 5, 6 and 7, the number of redundant bits in a clock cycle is 18, 16, 14 and 12, respectively. Different from the PS scheme in [6], the PS-encoding scheme based on Intra-SBWDM proposed in this paper only needs to perform PS coding on a small number of bits in a clock cycle controlled by the control unit (CU) module, which has a low implementation complexity and less on-chip resource usage.

3. Experimental setup

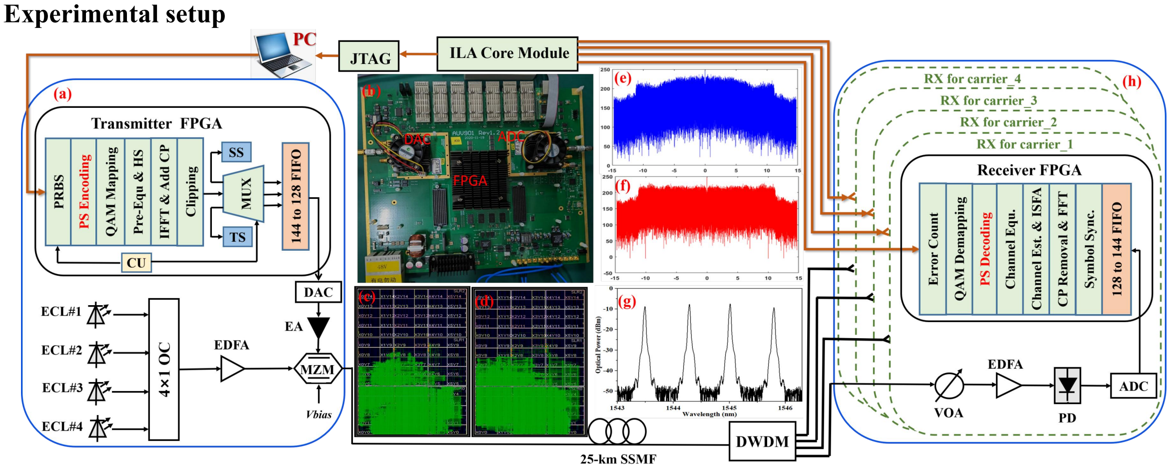

Fig. 2. Experimental setup, (a) block diagram of Transmitter, (b)DAC+ADC+FPGA real-time processing, (c) and (d) FPGA chip planner views for OFDM and PS-OFDM with k=4, (e) and (f)The electrical spectra w/o pre-equalization and w/ pre-equalization, (g) The optical spectrum after 25-km SSMF, (h) block diagram of Receiver.

Fig. 2 shows the experimental setup for PS-16QAM-OFDM with real-time reception in the WDM-PON system. In the modulation of PS-16QAM-OFDM, as shown in Fig. 2(a), the PRBS is generated to encode with PS-16QAM mapping rules and stored in the read-only memory of FPGA. In addition, the PRBS is pushed into the PS encoding module under the control of the CU. Due to the unsatisfactory frequency response of DAC/DAC, the pre-equalization technology is used to realize high-frequency component compensation. The compensated signal is conjugated and arranged to be Hermit symmetric, and then the 128 complex-valued QAM symbols per cycle in parallel are sent to a 128-point IFFT module to obtain 128 real-valued data in parallel per cycle. Add a 16-point cyclic prefix to resist ISI. Subsequently, the PS-OFDM signals are digitally clipped with a clipping ratio of 11 dB to reduce the PAPR and DAC quantization noise. The clipped signals are scaled to 6 bits to match the resolution of the 29.4912GSa/s DAC (ADA06S032G). It is also necessary to convert the clipped 144-path in parallel 6-bit wide data into 6×128bits serial data and send it to the First Input First Outputs (FIFO) module for buffering. Moreover, one 144-point synchronization sequence (SS) and eight 144-point training symbols (TSs) are generated offline and used for symbol synchronization and channel estimation, respectively. There are four optical downstream carriers with 100 GHz wavelength spacing generated by external cavity lasers with an output power of 13.5-dBm and the linewidth < 10 kHz. An optical coupler is used to combine four WDM carriers. An EA and EDFA are utilized for the power amplification of electrical PS-OFDM signals and the coupled optical signal, respectively. Then, the electrical PS-OFDM signals are used to drive MZM to realize E/O conversion. The electric spectra of OFDM signals before and after pre-equalization are shown in Figs. 2(e) and (f), respectively. After 25-km SSMF transmission, at the receiver, the received optical signal is first coupled into a DWDM, which is used to filter out four optical carriers into four branches. Then, an optical attenuator is cascaded in each branch to adjust the optical power to EDFA and the gain of the EDFA is 25dB. A PD with 15GHz 3-dB bandwidth is applied for signal O/E conversion. The 6-bit ADC (AAD06S032G) operating at 29.4912 GSa/s sampling rate are used to capture PS-OFDM signals from four branches. After that, the ADC outputs are fed into Xilinx AUV901 FPGA (XCVU9P-2FLGB2104I). Fig. 2(b) shows the DAC+ADC+FPGA real-time processing. The optical spectrum of the downstream PS-OFDM WDM-PON over 25-km SSMF transmission is shown in Fig. 2(g). The DSP algorithms of the FPGA receiver include symbol synchronization based on SS, CP removal, 128-point FFT, TS-aided and ISFA enhanced channel estimation and equalization, PS-decoding and QAM de-mapping. Subsequently, PRBS data error counts are implemented after demodulation. By using a Xilinx Integrated Logic Analyzer (ILA), the captured OFDM samples and the number of error bits are sent to the personal computer (PC) via the Joint Test Action Group (JTAG) interface. The offline BER will be measured with discrete OFDM samples. The FPGA chip planner views for OFDM and PS-OFDM with k=4 transceivers are illustrated in Figs. 2(c) and (d), respectively.

4. FPGA experiment results and discussion

Table 1 compares the on-chip resource usage of Intra-SBWDM and three other reported distributed matchers. It can be seen that the Intra-SBDWM requires only a few CLB LUTs and CLB registers compared to other three reported distributed matchers. The Intra-SBWDM can save CLB LUTs by 88.6% and does not require Block RAM, compared with the HiDM.

Table 1. Resource Utilization Comparison

Resource	HiDM [10]	PCDM (n=300, w=32) [11]	DM/inDM [12]	Intra-SBWDM
CLB LUT	5458	21253	292546	621
CLB Register	4910	5455	544424	5248
Block RAM	31	0	98	0

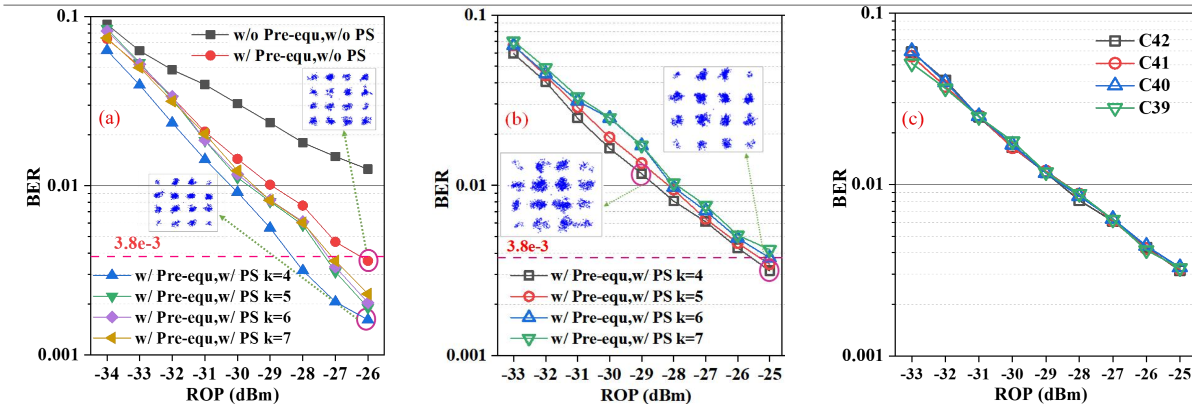

Fig. 3. BER versus ROP: (a) OBTB (b) 25-km SSMF (c) four carrier over 25-km SSMF with k=4.

Figs. 3(a), (b) and (c) shows the BER of PS-16QAM-OFDM in the case of OBTB, 25-km SSMF and 25-km SSMF for four carriers with k=4 under different received optical power, respectively. We can see that, in the OBTB case, about 2.2-dB receiver power sensitivity improvement can evidently be achieved for the PS-16QAM-OFDM with pre-equalization under HD-FEC (3.8×10^{-3}) threshold and k=4, compared to 16QAM-OFDM without pre-equalization. The constellations of 16QAM-OFDM and PS-16QAM-OFDM with the ROP of -26 dBm are shown in the insets of Fig. 3(a), respectively. The BER of PS-16QAM-OFDM with k=4 is still under the HD-FEC threshold after 25-km transmission. The constellations after 25-km SSMF transmission with the ROPs of -25 and -29 dBm are shown in the insets of Fig. 3(b), respectively. Four-carrier BER performance of PS-OFDM with k=4 with different ROP after the 25-km transmission is shown in Fig. 3(c). The BER performance of the four-carrier is almost the same.

5. Conclusions

In this paper, we experimentally demonstrated a low-complexity PS scheme for 16QAM-OFDM in a four-carrier-based real-time WDM-PON. The FPGA experimental results show that the Intra-SBWDM-based PS scheme with k=4 can save CLB LUTs by 88.6% and does not require Block RAM compared to the HiDM. *This work was partially supported by Chinese National key R&D projects under grant number 2018YFB1801703, and the National Nature Science Foundation of China (NSFC) under grant No 62127802.*

6. References

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