Inverse-Designed Grating Arrays for High-Sensitivity Plenoptic Time-of-Flight Pixels

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Abstract: We present a plenoptic time-of-flight pixel design using grating arrays with inverse-designed passive photonic power combining to achieve scalable signal-to-noise ratio. Experimental results are presented as a proof-of-principle demonstration of the pixel architecture. © 2022 The Author(s)

1. Introduction

Short-range LiDAR sensors are being adopted for a multitude of 3D imaging applications such as augmented reality, pose estimation, occupancy sensing, indoor mapping, and industrial automation. Achieving adequate sensing range and resolution in a small-footprint, low-cost, and low-power package remains one of the central challenges of designing such LiDAR systems. Angular-resolved sensing is commonly achieved through either solid-state beamsteering (e.g. optical phased arrays) [1] or structured illumination of the field-of-view [2]. However, these architectures typically have either package size and cost limitations, due to the use of lenses or diffractive optics, or power limitations, due to the requirement for high source power.

The plenoptic time-of-flight (ToF) sensor is an alternative approach to realizing short-range LiDAR sensors, wherein the ToF pixel utilizes a grating coupler to enable angular-resolved detection (Fig. 1(a)) [3]. Commercial foundry silicon photonic processes, offering the integration of passive and active photonic devices alongside CMOS readout electronics, present a competitive platform for realizing monolithic plenoptic ToF sensors. Silicon-on-insulator (SOI) processes additionally offer an attractive platform for low-power, high-speed, and high-sensitivity electronic-photonic integrated circuits (EPIC's) enabled by the low parasitics and leakage current of the SOI substrate [4]. Combining such a receiver with a low-cost, high-power 940nm VCSEL transmitter can enable short-range LiDAR in a low-cost and small form factor package.

However, the coupling of free-space optical signals to SOI EPIC's remains a challenge. The thin SOI substrate results in low absorption at infrared wavelengths, rendering frontside illumination impractical. Most SOI EPIC sensors rely on fiber coupling, either through edge couplers or grating couplers (e.g. [5]). Thus, the optical signal must be coupled to the photodetector either via edge- or waveguide-coupling in order to maintain efficient detection (Fig. 1(b-c)). Further, design rules and density limitations in a standard fabrication process can present challenges for creation of large, continuous collection areas.

In this work, we propose an architecture for realizing a plenoptic pixel using an array of grating couplers coupling to a single Ge-on-Si avalanche photodetector (APD). The proposed design utilizes inverse-designed passive photonic devices to achieve an efficient and compact power combining network. This architecture, implemented in Global Foundries 45nm silicon photonic process (45SPCLO) [4], allows for a scalable collection area while maintaining a fixed minimum noise floor, low detector capacitance, and meeting commercial foundry density limitations.

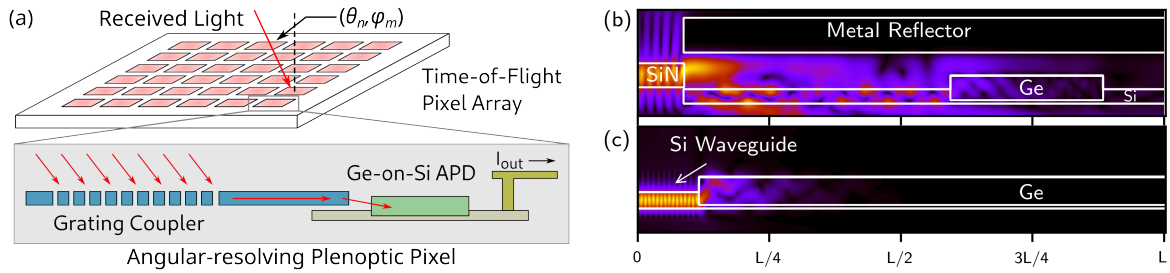

Fig. 1: (a) Operating principle of a plenoptic ToF sensor. A grating coupler acts as an angular-selective filter to separate light by the angle of incidence. An array of such pixels can be used to create a small form factor, short-range LiDAR sensor. (b-c) Comparison of (b) edge-coupling with minimum SiN-Ge space and (c) waveguide-coupling coupling efficiency. In the edge-coupling case, only ∼30% of the light is absorbed in the Ge absorption region vs. >95% for waveguide-coupling.

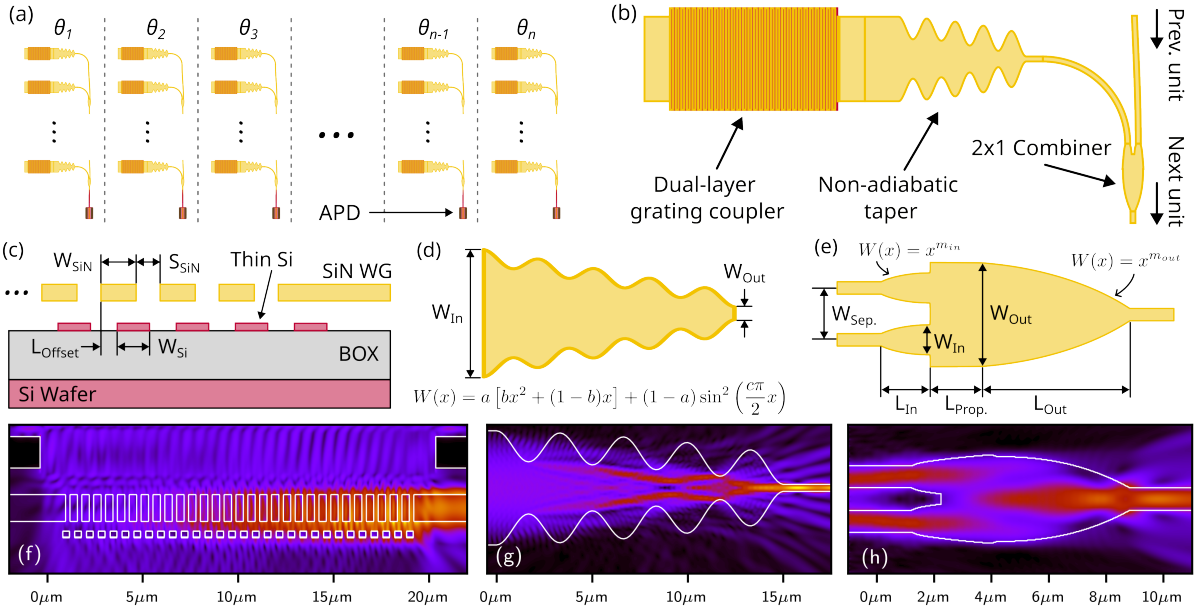

Fig. 2: (a) The grating array pixel concept, where the gratings of each column are tuned to a different angle θ_i. (b) A single unit of a grating array utilizing inverse-designed passive photonics. (c-e) Design parameters for shape optimization of the grating coupler, taper, and power combiner. (f-h) FDTD simulations of optimized components. The grating coupler, taper, and power combiner exhibit coupling efficiencies of 41% (IL=3.87 dB), 78% (IL=1.08 dB), and 80% (IL=0.97 dB), respectively.

2. Design Considerations

One architecture for realizing a plenoptic pixel is a large-area uniform grating coupler where the output slab waveguide is edge-coupled to a Ge-on-Si APD (Fig. 1(b)). While this approach is simple to implement, it suffers from low coupling efficiency and poor sensitivity scaling. Since the length of the following photodetector must be matched to the collection length of the grating coupler, the noise current of the APD scales as the square root of the collection length. The photodetector capacitance will scale linearly with the collection length, adversely affecting the readout transimpedance amplifier bandwidth and noise floor [6]. Edge-coupling from a silicon nitride waveguide to a Ge-on-Si photodetector presents a fabrication challenge, as a relatively large minimum space between the SiN and Ge layers must be maintained for manufacturing reliability, reducing the photodetector coupling efficiency. Critically, SOI CMOS processes must enforce density limitations to ensure process uniformity. These density limitations place a maximum continuous area constraint on the photonic layers in the design process, thus limiting the maximum continuous collection area. While the total collection area could be scaled by placing multiple large-area grating couplers with APD's connected electrically in parallel, the noise and capacitance scaling issues remain.

Waveguide-coupling to the photodetector can address many of these limitations. Coupling from a SiN waveguide to a Ge-on-Si photodetector allows for significantly improved coupling efficiency compared to edge-coupling (Fig. 1(c)). Stacking multiple collection areas (i.e. grating couplers) together results in a linear scaling of the effective collection area. By combining these collection areas together using a passive photonic power combining network, the effective collection area and signal-to-noise ratio at the photodetector can be scaled linearly (assuming lossless components) (Fig. 2(a)). However, this combining network must be relatively compact to maintain a low photonic layer density and high fill-factor. To achieve a high grating coupler collection efficiency and compact combining network with relatively low insertion loss, we employed shape optimization using the adjoint method (see [7]) in Lumerical FDTD for all critical components.

All components are optimized for λ=940nm. Fig. 2(b) shows an individual unit of the array with inverse-designed passives. The parameters sets for each component are defined in Fig. 2(c-e). The grating coupler uses a dual-layer geometry consisting of a primary SiN grating layer and a secondary thin-silicon bottom reflector. The taper consists of a non-adiabatic, sinusoidally-varying sidewall profile. The 2x1 power combiner geometry consists of two exponential input tapers, a propagation region, and an exponential output taper. Similar geometries have been demonstrated in [8–10]. For all components geometries, the bounds of the model parameters are set such that the foundry minimum width-space rules are respected for all possible designs. The simulated electric transmission of each optimized component is shown in Fig. 2(f-h). While higher transmission efficiencies have been demonstrated in the literature for Si passives, the low index contrast of the SiN-SiO_2 core-cladding makes it difficult to achieve higher efficiency in a compact area, and small component size was prioritized.

To meet the layer density rules in a standard fabrication process, the grating-to-grating pitch, Λ, of a column of

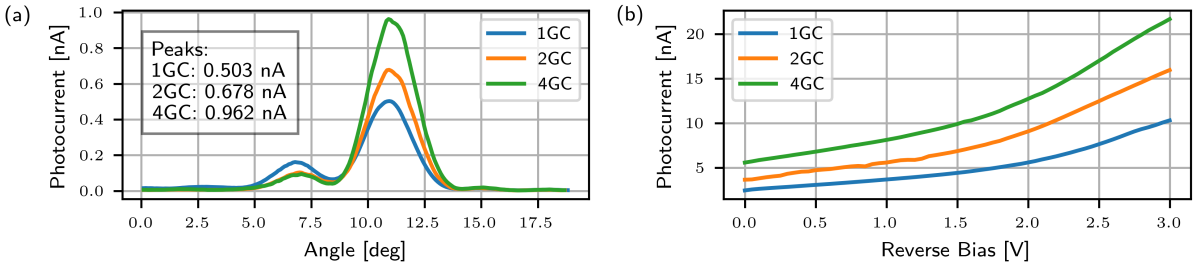

Fig. 3: Experimental results demonstrating photocurrent scaling for 1, 2 and 4 grating couplers. (a) Photodetector response vs. incident angle, demonstrating the angular selectivity of the arrays. (b) Photocurrent vs. reverse bias voltage at the peak coupling angle. V_R for these devices was restricted to 3V due to reliability limitations.

grating couplers is tuned. The typical minimum metal layer density is approx. 10%, so Λ is tuned such that the total area of the SiN and associated layers is <75% of the total design area. The remaining 25% is then used for metal fill to achieve the minimum density. Further, because the grating array acts similarly to an optical phased array (without active phase tuning), Λ must be tuned such that the phases at the two inputs of the combiner are matched in order to maintain maximum coupling efficiency. This matching is achieved by simulating the phase delays of the waveguide bend, combiner, and s-bend between the combiners and tuning the length of the s-bend ($L_{sbend} = \Lambda$) such that the total optical path length is equal to an integer multiple of the wavelength ($OPL = \frac{m\lambda}{n_{eff}}$).

3. Preliminary Experimental Results

To demonstrate SNR scaling for increasing numbers of grating couplers, test structures are fabricated using the optimized dual-layer grating coupler and sinusoidal taper. The grating couplers are combined using a tree-style configuration with simple 2x1 MMI couplers (rather than the folded-style combining network shown in Fig. 2(a)) to eliminate any potential phase mismatch issues. The grating couplers are designed for a 10° coupling angle. Fig. 3(a-b) demonstrates the increasing photocurrent with increasing number of grating couplers. Because each combination of grating couplers connects to the same minimally-sized, waveguide-coupled photodetector, the noise floor of the receiver remains fixed and the SNR scales directly with the number of grating couplers. The measured peak coupling angle of the grating couplers is $\sim 11°$. This discrepancy in designed vs. measured coupling angle may be due to slight process variations or variation in the wavelength of the laser used in measurement. The photocurrent scaling is limited primarily by the losses of the un-optimized MMI couplers and the waveguide losses of the s-bends between the combiners. More efficient scaling would be enabled by the folded-style power combining network illustrated in Fig. 2(a) providing that phase matching is achieved. Fig. 3(b) demonstrates the avalanche operation of the Ge-on-Si photodetector at the peak coupling angle, providing current gain.

4. Conclusion

We present a scheme for creating angular-selective pixels with scalable collection area and fixed minimum noise floor in a commercial SOI silicon photonic platform for a ToF receiver. An inverse-designed passive combining network allows for combining collected power from multiple grating couplers while maintaining low insertion loss, compact size, and respecting process design rules. Experimental results provide a proof-of-concept demonstration of the SNR scaling. Investigation of alternative geometries or inverse-design methods such a topological optimization may provide further reduction of the insertion loss of the combining network. While these pixels are designed for a plenoptic ToF receiver, they may be applicable to other EPIC's which require receiving free-space or near-field light, such as multi-input visible light communication receivers or photonic biometric sensors.

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