A 200Gb/s Low Power DSP-Based Optical Receiver and Transmitter with Integrated TIA and Laser Drivers

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Abstract: Fully integrated low power 200Gb/s DSP based optical transmitter and receiver ICs with transmitter chip incorporating fully integrated laser drivers and receiver chip with fully integrated Transimpedance amplifier (TIA) in 16nm FinFet using wirebond technology

1. Introduction

The continued growth of Internet traffic and the accelerated rise of hyperscale data centers as well as the emerging 5G fronthaul results in high demands for cost-effective, high-speed optical IC's. The current optical module products employ multiple IC's to perform the needed E-O and equalization functions. These IC achievements have been published over the past decade [1-3]. In this paper, we present 4x56Gb/s PAM4 transmitter and receiver DSP ICs with fully integrated Laser drivers and Transimpedance amplifiers (TIA) using wirebond technology reducing costly package supply chain dependency while further simplifying the assembly process, component count on the optical modules and maintaining superior system performance. The highly configurable DSP engine is designed to achieve performance levels for single-mode and multi-mode optical interconnects for IEEE Ethernet and Fibre Channel standards including 100G-xR2, 200G-xR4, 400G-xR8, 32GFC and 64GFC suitable for OSFP, QSFP56, QSFP-DD form factors suitable for PSM or CWDM transceivers.

2. Transmitter and Receiver ICs

2.1. Top Level

The transmitter IC shown in Figure 1 consists of four 28Gbaud lanes incorporating integrated laser drivers that supports both single-mode and multi-mode interconnect application from SR to LR reach ranging from <100m using VCSEL laser driver and up to 10km using EML/SiPho laser driver. The host receiver in transmitter chip is analog based CDR and contains adaptive CTLE and AGC that can equalize up to 12dB loss in the host channel and is compliant to OIF-CEI-56G VSR, GAUI-4 (PAM4), CAUI-4 (NRZ) and CPRI. Independent CDR in the host receiver and PLL in the line transmitter allows the chip to work in breakout mode enabling connectivity between network devices with difference speed ports

2.2. VCSEL Array Driver

VCSELs pave the way to short-reach, low-cost parallel-optical links due their ease of integration with MMF systems. The common-cathode VCSEL array at 250-um pitch is lowest cost platform which requires singe-ended dc-coupled current-mode driver design with integrated bias circuit. The single-ended nature and the tight pitch requires careful design and modeling of the return current and local on-chip decoupling to prevent crosstalk. Finally, the VCSEL at this speed has a bias-dependent non-linearity in its electro-optic (E-to-O) transfer function, which was overcome with the use of nonlinear pre-compensation from the TX DSP to counteract the non-linear characteristics.

2.3. EML/SiPho Driver

EML and SiPho MZM modulator technologies can support longer distance transmissions since it is a single-mode source with lower chromatic dispersion and chirp. The integrated EML/SiPho driver shown in Figure 2 uses 7-bit segmented DAC and supports up to $1V_{PP,\ SE}$ swing driving an EML laser, $2V_{PP,\ DIFF}$ into a 60-ohm SiPho load and $0.8V_{PP,\ DIFF}$ swing into a 100-ohm differential load. The cascode structure is needed to avoid electrical-overstress (EOS) on the transconductance devices. Bleeder current sources across the resistive termination are used to raise the common-mode level further improving the driver's SNDR at the cost of capacitive loading. The use of the T-coil the driver enables the design to achieve a bandwidth of 17GHz over worst case PVT conditions.

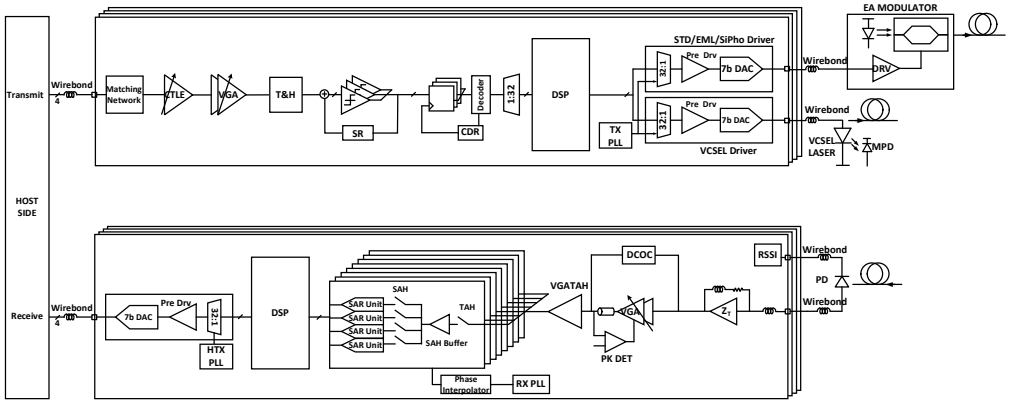


Fig. 1: 200Gb/s Transmitter and Receiver ICs

2.4. DML Laser Driver

The increasing demand for the emerging 5G technology led to rapid adoption of the next generation optical fronthaul technology covering distance up to 10km. To meet the market needs for high output power and low cost, another variant of driver is needed which can directly modulate a DML Laser that resides inside a TOSA. The DML laser driver block diagram is shown in Figure 3. The driver features a 7-bit DAC based driver, control circuitry for the laser current bias and a bias/control block for an external monitor photodiode used as optical-power loop feedback element. The board, and flex have been co-designed with the driver IC core and large signal coupled differential rate equation laser model to optimize for electro-optical performance. The DML driver can provide modulation current up to 60mAp-p and data-rates up to 28.9Gbaud PAM4, while guaranteeing a bit error rate better than 1×10^{-7}. The DML driver provides up to 125mA DC current for production burn-in test.

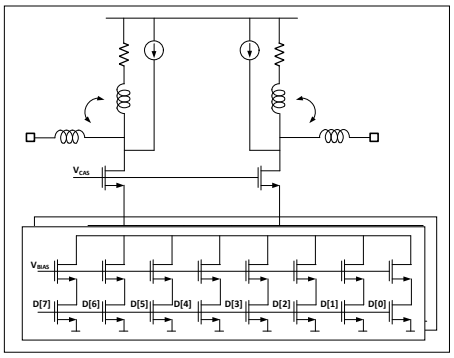


Fig. 2: EML/SiPho/STD Driver

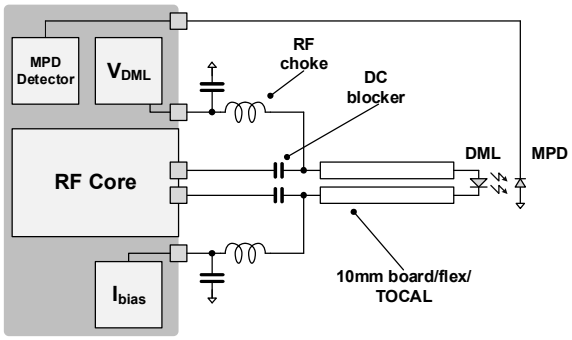


Fig. 3: DML Laser Driver

2.5. Transimpedance Amplifier and Time-Interleaved SAR ADC

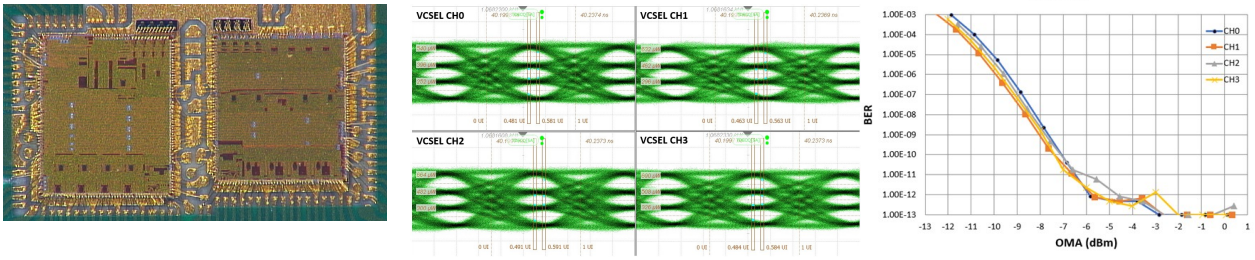
The block diagram of the receiver is shown in Figure 1. The input current from the photodiode (PD) is first passed through a transimpedance stage (ZT). The signal is then adjusted through variable gain amplifiers to full-scale of the ADC. This voltage level is controlled by an analog loop which sets the gain of ZT/VGA1/VGA2 & a DSP gain control loop which sets the gain of VGATAH. The TIA can accommodate an input dynamic range of over 30dB from sensitivity to overload. The TIA/AGC achieves a total noise <15pA/sqrt-Hz which is similar to a previously published 56Gbps PAM4 TIA in SiGe [4]. The ADC consists of 32 interleaved unit SARs arranged in a two-level hierarchical interleaving scheme. A single-ended 14GHz clock from the phase interpolator (PI) is used to generate 8 clock phases to provide 3.5GHz 25% duty cycle sampling clock for the track and hold switch (TAH). The timing mismatch (per TAH), offset and gain calibration (per unit SAR) are detected by the DSP and corrected using analog circuitry.

3. Optical Performance

The optical assembly for 200G SR using SW optics is shown in Figure 4(a). The RX and TX channel pitch is 250-um and separated by 1mm to match with the optical pitch defined by the MPO connector. Achieving this pitch simplifies the optical alignment and assembly process and reduces passive optical component cost significantly.

However, this tight pitch comes with the difficult task of mitigating crosstalk to maintain the required high performance. The wirebond interconnects are carefully modeled using 3-D EM simulation to minimize all crosstalk sources (RX-RX, TX-TX and TX-RX). In addition, the adverse effects of the wirebond solution are supply IR drop and voltage ripple due to the DSP dynamic current's peaks to average ratio. In addition, supply IR drop and voltage ripple introduce intra-chip and inter-chip crosstalk which also needs to be minimized with rigorous design optimization of on-chip and off-chip decoupling component selection and placement.

Measurement results show negligible crosstalk in both RX sensitivity and BER floor based on IEEE defined methodology as shown in Figure 4(c). The VCSEL driver converts a 7-b digital code serialized from 32-lane 875Mb/s data from the DSP core with pre-compensation where the electrical current for VCSEL is forward-tilted so that the optical output eye has reduced skew from VCSEL relaxation oscillation, Figure 4(b). With outer optical OMA ($TXOMA_{outer}$) of 1.9dBm, TDECQ <0.7dB with ER >4dB and BER $<1\times10^{-12}$ were achieved. The IC's combined power consumption of 2.8W meets the strict power requirements of QSFP56 and QSFP-DD form factors.



(a) (b) (c)

Fig. 4: (a) Chip, VCSEL and PD assembly, (b) VCSEL array TX eye diagram, and (c) 4-ch SW RX waterfall curve

Receiver Performance

Item	Lab Measurements
Receive Sensitivity[1] (OMA)	< -11dBm
Input Referred Noise	< 15pA/sqrt-Hz
Min. SNDR	30dB

[1] BER<1×10^{-4} without FEC

Transmitter OMA_{OUTER}

OMA	Lab Measurements
VCSEL Driver[1] ($8mA_{DC}/8mA_{MOD}$)	1.9dBm
SiPho Driver[1] ($2V_{PP\_DIFF}$)	4.2dBm
EML Driver[1] ($1V_{PP\_SE}$)	3.4dBm

[1] Optical OMA Depends on Module Vendor's Lasers

4. Conclusion

We present fully integrated low power transmitter with VCSEL/EML/SiPho laser drivers and integrated-TIA DSP-based receiver using four 50Gb/s lanes that support rates up to 400Gb/s in xR4 reaches with sensitivity better than required by IEEE and Fibre Channel Standards and with BER below the KP4-FEC threshold of 2.4×10^{-4}. The integration of PMD and DSP enables a low-cost, packageless and wirebond solution with competitive power dissipation (2.8W) while maintaining state-of-the-art optical TX parameters and RX sensitivity and overload performance This proven methodology and architecture can be established on rates of 100Gb/s per lane and beyond achieving higher throughput at lower power and cost.

5. References

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