

Speedy and Cost-efficient Optical Network Modernization through Quantum-inspired Computing

Masahiko Sugimura¹, Mohammad Javad-Kalbasi², Hidetoshi Matsumura³, Xi Wang⁴, Paparao Palacharla⁴, and Shahrokh Valaei²

¹Fujitsu Limited, Shiodome City Center, 1-5-2 Higashi-Shimbashi, Minato-ku, Tokyo 105-7123, Japan

²The University of Toronto, ³Fujitsu Consulting (Canada) Inc., ⁴Fujitsu Network Communications Inc. masahiko.sugimura@fujitsu.com

Abstract: We present a migration plan optimization solution to accelerate the removal of legacy devices and minimize travel costs in network modernization utilizing Fujitsu Digital Annealer. Our method found more cost-efficient plans by up to 70%. © 2023 The Author(s)

1. Introduction

In recent years, an increasing number of telecom operators are experiencing difficulties in managing their decades-old SONET/SDH-based optical transport networks. For many, these legacy infrastructures have reached or long past their intended lifespan, resulting in higher risk of hardware failure and service outage. Meanwhile, the end-of-life equipment has become increasingly costly to maintain, due to multiple factors including lack of vendor support and diminishing pool of qualified personnel. To tackle these challenges, many operators have initiated network modernization (NetMod), with the aim of replacing their aging networks with modern platforms such as packet-optical employing OTN and circuit emulation.

Modernizing a legacy network that carries live circuits, however, is a time-consuming and labor-intensive endeavor. It involves engineers visiting each circuit terminating site, setting up a new device, migrating all circuits from the legacy device to the new device, and removing the legacy device. Depending on the circuit count, size and complexity of the network, this process may take months or even years to complete [1].

Consequently, a well-designed circuit migration plan, which determines an optimized network-wide circuit migration/site visit sequence, plays a crucial role in the speedy and cost-efficient NetMod execution. Because a legacy device removal yields most prominent immediate benefits in terms of reduced OPEX/operational risk and increased revenue opportunity (e.g., vacated site space for new services), it is desirable to remove legacy devices from sites in a most speedy way. A legacy device, such as a SONET/SDH multiplexer or a Digital Cross-connect system (DCS), becomes ‘zero-fill’ after all its carried circuits have been migrated away. Such a zero-fill device can be safely disconnected from the network with no service impact. Thus, to accelerate the removal of legacy devices, it is essential to design an optimized circuit migration sequence that achieves as many zero-fill devices as early as possible. Meanwhile, since remote configuration is either not supported by these devices or has been disabled due to security concern, the engineers need to travel to every circuit terminating site. More specifically, a pair of engineers would visit the two terminating sites of a circuit to perform manual migration, and then travel to another pair of sites for next circuit migration. For a large-scale network (e.g., statewide, regional, or national) with many sites and longer spans, the labor cost/operational delay associated with traveling from site to site can add up quickly. Thus, optimizing the sequence of site visits throughout circuit migration, with the aim of minimizing the total travel distance, helps reduce the overall travel cost and labor expenses.

This is a combinatorial optimization problem, which can be addressed as a Binary Quadratic Problem (BQP). BQPs are NP-hard in general. Furthermore, a typical NetMod project may require migrating several hundred circuits, which leads to a large scale BQP with more than 10,000 decision variables. Although existing Mixed Integer Programming (MIP) solvers work with BQPs, their performance tends to degrade with the increase of problem size. On the other hand, there are emerging technologies for solving large scale BQPs, including quantum annealer, CMOS annealers, etc. In a related work addressing a similar problem [2], the authors leverage Fujitsu Digital Annealer (DA), which is a recent quantum-inspired computer architecture capable of solving large scale BQPs [3], and demonstrate that it can find efficient circuit migration plans. However, it does not consider the travel cost for site visits.

In this paper, we present a new BQP formulation for DA capable of both accelerating the removal of legacy devices and minimizing the travel distance of site visits, and demonstrate that the new method finds more optimal migration plans by up to 31% in legacy device removal speed and 70% in travel cost compared to a commercially available MIP solver.

2. Problem Statement

As a metric for how early all devices in a legacy network become zero-fill overall, we employ Time to Zero-fill (TTZ), which is the summation of devices in-service time across all circuit migration steps. For simplicity, we assume that

one circuit is migrated per migration step, and one non-zero-fill device accrues one unit of in-service time in one migration step. The other metric is the Total Travel Distance (TTD) required for engineers to migrate all circuits, which indicates the travel cost for all site visits. For simplicity, we assume only two engineers in this study. Thus, to migrate each circuit, the two engineers visit the two terminating sites of the circuit and work jointly, then travel to the terminating sites of the next circuit. Fig. 1 shows an example of TTZ and TTD calculation in a network with 5 devices and 3 circuits (A-C). With migration sequence of B-A-C, TTZ adds up as 5 (step 1/circuit B) + 5 (step 2/circuit A) = 10, and TTD is summed up to 300 km. On the other hand, with sequence of C-B-A, TTZ is only 5, and TTD becomes 400 km. Our goal is to find a circuit migration sequence that minimizes both TTZ and TTD with adjustable trade-off.

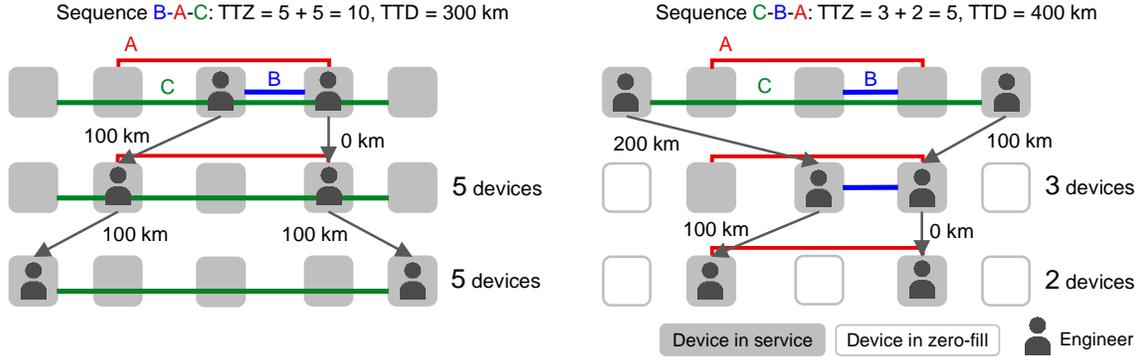


Fig. 1. An example of TTZ and TTD calculation in a network with 5 devices and 3 circuits (A-C).

3. Proposed Approach

First, we developed High Order Binary Optimization (HOBO) formulations for the TTZ minimization.

$$\min_{x_{c,t}} - \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} \prod_{c \in P_d} x_{c,t} \quad (1a)$$

$$\text{s. t. } x_{c,t} \leq x_{c,t+1}, \forall c = 1, \dots, N_C, \forall t = 1, \dots, N_C - 1 \quad (1b)$$

$$\sum_{c=1}^{N_C} x_{c,t+1} - \sum_{c=1}^{N_C} x_{c,t} = 1, \forall t = 1, \dots, N_C - 1 \quad (1c)$$

N_C and N_D are constants denote the total number of circuits to be migrated and the total number of devices to be zero-fill respectively. Each circuit has an index $c \in \{1, \dots, N_C\}$. Each device has an index $d \in \{1, \dots, N_D\}$. P_d is a set of circuits carried on device d . If device 1 carries circuits 2 and 5 then $P_1 = \{2, 5\}$. $x_{c,t}$ is a binary decision variable that denotes the status of circuit c at migration step t , which takes 0 if it is in service and 1 if it has been migrated. The status of device d at migration step t is calculate by $\prod_{c \in P_d} x_{c,t}$, which takes 0 if it is in service and 1 if it is zero-fill. TTZ is calculated by $N_C \times N_D - \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} \prod_{c \in P_d} x_{c,t}$. Since we can ignore the constant part $N_C \times N_D$ while minimizing TTZ, we have Eq. (1a) as an objective function. Eq. (1b) are constraints that a circuit will never be recovered once it has been migrated. Eq. (1c) are constraints that only one circuit can be migrated at a time.

DA and general MIP solvers process linear or quadratic functions. Therefore, we transformed the HOBO formulation to a BQP formulation with the following techniques. In [4], the authors show that the high order objective function $\min_{x_i} - \prod_{i=1}^N x_i$ is equivalent to the quadratic objective function $\min_{x_i} v(\sum_{i=1}^N 1 - \sum_{i=1}^N x_i - 1)$. v is a binary auxiliary variable to ensure that both functions take the same value for all possible combinations of x_i . By introducing this transformation, we have the following BQP objective function.

$$\min_{x_{c,t}} \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} v_{d,t} \left(\sum_{c \in P_d} 1 - \sum_{c \in P_d} x_{c,t} - 1 \right) \quad (2a)$$

In preparation for combining the objective function for TTD minimization, we introduced a binary decision variable $z_{c,t}$ that denotes the timing of migrating circuit c , which takes 1 only if the circuit c is migrated at migration step t . We transformed the objective function Eq. (2a) with $x_{c,t} = \sum_{r=1}^t z_{c,r}$ to have the following objective function.

$$\min_{z_{c,r}} \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} v_{d,t} \left(\sum_{c \in P_d} 1 - \sum_{c \in P_d} \sum_{r=1}^t z_{c,r} - 1 \right) \quad (3a)$$

The formulation for TTD minimization is basically a BQP formulation for traveling salesman problem (TSP) [5], where engineers travel from one circuit to another. However, unlike conventional TSP, this problem requires two engineers travel simultaneously. Thus, we modified some parts of TSP to fit to this problem. We defined the distance

between circuits as the summation of distance that two engineers travel from the end points of the first circuit to the ones of the second. There are two cases in how two engineers travel from one circuit to another, and the distance may differ. Accordingly, we pre-calculated the distance between circuits i and j for both cases and defined the shorter one as the distance between circuits $d_{i,j}$. We have the following objective function including TTZ and TTD.

$$\min_{z_{c,r}} w_1 \left\{ \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} v_{d,t} \left(\sum_{c \in P_d} 1 - \sum_{c \in P_d} \sum_{r=1}^t z_{c,r} - 1 \right) \right\} + w_2 \left\{ \sum_{i=1}^{N_C} \sum_{j=1}^{N_C} d_{i,j} \sum_{r=1}^{N_C-1} z_{i,r} z_{j,r+1} + \sum_{i=1}^{N_C} d_{0,i} (z_{i,1} + z_{i,N_C}) \right\} \quad (4a)$$

$$\text{s. t. } \sum_{t=1}^{N_C} z_{c,t} = 1, \forall c = 1, \dots, N_C, \quad \sum_{c=1}^{N_C} z_{c,t} = 1, \forall t = 1, \dots, N_C \quad (4b)$$

We assume that engineers depart their office to the first circuit and return to the office from the last one. $d_{0,i}$ denotes the distance between the office and circuit i . w_1 and w_2 are the weight values to control the trade-off between TTZ and TTD. By using $z_{c,t}$ we can replace the constraints Eq. (1b) and (1c) with constraints Eq. (4b).

4. Evaluation

We solved the BQP with 3rd generation DA in an environment exclusive for research purpose [3], and with Gurobi V9.1.1 using 32 cores on Intel (R) Xeon (R) Platinum 8176 CPU@2.10GHz. Gurobi is one of the state-of-the-art commercially available MIP solvers. The solutions were evaluated in terms of TTZ and TTD. We used three topologies (France, India, Pioro) from SNDlib datasets as legacy networks [6], which have 25, 35, and 40 nodes respectively. We assumed that each node corresponds to a site hosting a legacy device, and used the shortest paths consist of nodes between pairs of source and destination nodes in the datasets as circuits targeted for migration. We selected 100 and 290 circuits randomly from the datasets.

Fig. 2 and Fig. 3 show TTZ and TTD for France with 100 and 290 circuits minimized by DA with 0.5 hours of computation time and Gurobi with 6 hours. The results were obtained for 9 cases of weight values (99:1, 97:3, 95:5, 93:7, 91:9, 7:3, 5:5, 3:7, 1:9) representing varying trade-offs between TTZ and TTD. Each case is an average of three trials for DA since DA solves a problem stochastically. DA achieves 7% to 31% lower TTZ and over 50% lower TTD than Gurobi for 100 circuits and 4% to 28% lower TTZ and over 70% lower TTD for 290 circuits with 1/12 of computation time. Gurobi yields single solution regardless of weight values for 290 circuits. In contrast, DA is able to continue reflecting weight values to its solutions in terms of trade-offs between TTZ and TTD. India and Pioro results exhibit similar trend and are not shown due to space limit.

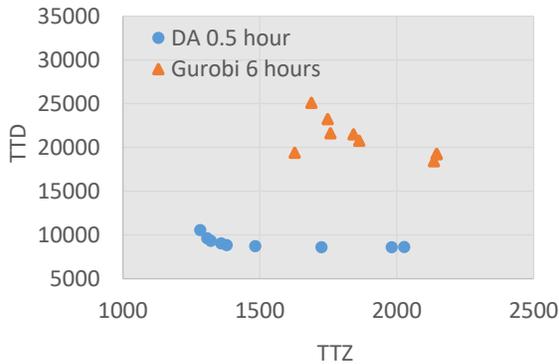


Fig 2. TTZ and TTD for France 100 circuits.

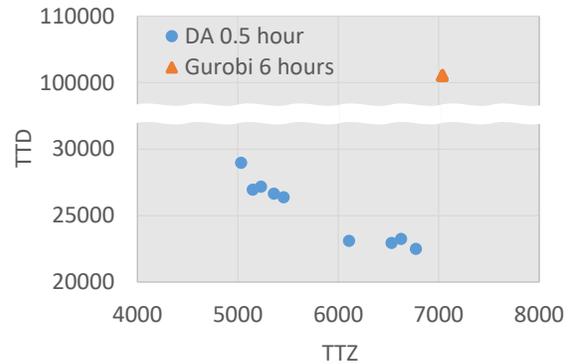


Fig. 3. TTZ and TTD for France 290 circuits.

5. Conclusions

In this paper, we developed a new BQP formulation to utilize Fujitsu Digital Annealer for generating optimized NetMod solutions. Compared to a commercial MIP solver, the Digital Annealer approach achieves up to 31% in speed and up to 70% in cost improvement. These results suggest the new approach effectively contributes to a speedy and cost-efficient execution of worldwide optical network modernization.

6. References

- [1] Cisco, "How Cisco IT Migrated TDM Local Access from SONET to OC-192 Infrastructure," (2017).
- [2] M. Sugimura et al. "Accelerate Optical Network Modernization through Quantum-inspired Digital Annealing," ECOC2022 (Basel, 2022).
- [3] H. Nakayama et al. "Description: Third Generation Digital Annealer Technology," https://www.fujitsu.com/jp/documents/digitalannealer/researcharticles/DA_WP_EN_20210922.pdf, accessed on 17 Oct. 2022.
- [4] V. Kolmogorov and R. Zabin, "What Energy Functions Can Be Minimized via Graph Cuts?," TPAMI, vol. 26, no. 2, pp. 147-159 (2004).
- [5] A. Lucas, "Using formulations of many NP problems," Frontiers in Physics 2, 5, (2014).
- [6] S. Orlowski et al. "SNDlib 1.0—Survivable Network Design Library," Networks, vol. 55, issue 3, pp. 276-286 (2009).