$In_{0.52}Al_{0.48}As$ Based Single Photon Avalanche Diodes with Multiple M-Layers for High-Efficiency and Fast Temporal Responses

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Abstract: Multiple multiplication-layers SPADs with excellent performances in terms of high-efficiency (>74%), neat impulse response time (101ps), and short hold-off time (83ns@<1% afterpulsing) can be achieved simultaneously with a simple passive quenching circuit under gated-mode operations.

OCIS codes: (230.5170) Photodiodes (230.0040) Detectors

I. Introduction

Semiconductor based single photon avalanche diodes (SPADs) play important roles in several different applications, such as time-of-flight (ToF) lidar [1], single-photon communications, and quantum computing. Compared with the Silicon (Si) based SPADs at short-infrared (IR; ~0.9 μm), the III-V (InP or $In_{0.52}Al_{0.48}As$) based ones usually has much more serious afterpulsing effect and lower single photon detection efficiency (SPDE) due to that their material quality of multiplication (M-) region is not as good as Si ones. Nevertheless, the III-V SPADs can effectively extend the optical operation window to cover the long-IR wavelengths (1.31 to 1.55 μm), which permit higher optical power at eye-safety threshold than short-IR for ToF LiDAR applications. The silicon based Si/Ge SPAD operated at around 1.31 μm wavelength is an alternative solution for long-IR ToF application. However, the room-temperature operation for such technology still remains a challenge [1]. In this work, we demonstrate a novel $In_{0.52}Al_{0.48}As$ based SPAD with a unique multiple M-layers design, which can fundamentally overcome the trade-offs between SPDE, response time (jitter), and hold-off time (afterpusling). Excellent performances in terms of record-high SPDE (74%), tailless impulse response time (101 ps), and short hold-off time (83 ns @<1% afterpulsing) can be achieved simultaneously with a simple passive quenching circuit under gated-mode operations at 1.31 μm optical wavelength.

II. Device Structure

Figures 1 (a) depicts the conceptual cross-sectional views of the demonstrated APD structure. Note that, for simplicity, Figure 1 is not drawn to scale. The top-view of the fabricated device with an active window (mesa) diameter of 60 (110) μm is shown in the inset to Figure 1 (a). The main difference between our proposed device structure and traditional APD is that we insert additional charge layers inside the multiplication regions [2]. As can be seen, the 600 nm thick multiplication (M-) layer in our APD is subdivided into three parts, 100, 100, and 400 nm in thickness. Due to the stepped electric field profile inside, the electrons will be energized by the first two M-layer with a thickness of 100 nm, respectively, where the electric field strength may not be high enough to trigger significant impact ionization, and then transit to the third 400 nm thick M-layer to initiate successive impact ionization. This design provides better localization of impact ionization than can be achieved in a uniform 600 nm thick M-layer, therefore it can greatly shorten both the impulse response (jitter) and hold-off time (afterpulsing). Furthermore, as compared to directly shrinking the thickness of the single M-layer in the traditional APD to 400 nm, the two additional M-layers in our structure can avoid an increase in the tunneling dark current and dark count rate (DCR) under Geiger mode operation. In order to suppress the edge breakdown at the edge of the bottommost M-layer, which has the strongest E-field, a composite charge layer ($In_{0.52}Al_{0.48}As$/InP) design is adopted [3] to precisely etching stop above the M-layer by use of selective chemical etching process and zero the E-field in the edge of M-layers.

III. Measurement Result:

Figure 1(b) shows the measured bias-dependent dark current, photocurrent, and operation gain of the demonstrated APDs, subject to different optical pumping powers (1 to 100 μW) at an optical wavelength of 1.55 μm. As can be seen, the measured breakdown voltage (V_{br}) and punch through voltage (V_{pt}) are around -45 and -30 V, respectively. With a 2 μm-thick $In_{0.53}Ga_{0.47}As$ absorption layer, the theoretical maximum unit gain responsivity will be around 1 A/W at the 1.55 μm wavelength. Figure 1(c) shows the bias-dependent O-E frequency responses measured under a 1 μW optical pumping power at the 1.55 μm wavelength. The measured 3-dB O-E bandwidths decreases with the increase of reverse bias voltages as expected, nevertheless, under V_{br} operation (-45 V), there is no dramatic degradation in speed and the 3-dB bandwidth can pin at 1.5 GHz. Such nearly invariant high-speed performance under Geiger mode operation implies a short jitter response time, which will be discussed in detail latter. Figure 2 shows our measurement setup and the inset shows the schematic diagram of our APD mounted on the circuit board for single photon measurement. The SPAD is operated under gated-mode with a passive quenching circuit. The gated signal is composed of a dc voltage, which is slightly below V_{br}, and a ac electrical pulse with a repetition rate at 10 kHz and a 1.5 ns pulse-width. All the characterizations are carried out in a LN2 open-cycle cryostat (Optistat CF, Oxford

Instruments) which can cool the device down to 77K. The values of excess bias voltage (V_{ex}) specified in the following figures are normalized to the measured V_{br} at each different temperature. A pulse laser at 1310 nm optical wavelength, which has a 50 ps pulse-width and a repetition rate of 10 kHz synchronized with the gated electrical pulse, is adopted as light source for our static and dynamic measurements. During experiment, the laser outputs are attenuated to about 0.1 photons per pulse. The timing jitter is determined by a time-correlated single photon counting module (TCSPC) with a timing resolution of 4 ps. Figure 3 shows the measured dark count rate (DCR) density versus V_{ex} at different ambient temperatures. Here, the measured DCR values of each device is normalized to its active area (110 μm diameter, as shown in Figure 1 (a)). We can clearly see that the DCR density values gradually increase with the V_{ex} and saturate when it is over at around 5.6 %. Besides, under such high V_{ex} (> 5.6%) regime, the DCR values can't be significantly reduced by decreasing ambient temperatures. This implies that under high V_{ex}, the measured DCR is dominant by the tunneling current from M-layers instead of from thermal generation process. Figure 4 (a) and (b) shows the measured SPED and corresponding DCR density versus V_{ex} under room-temperature (RT) and 225 K operation, respectively. Table 1 shows the benchmark of reported InP and $In_{0.52}Al_{0.48}As$ based SPADs. As can be seen, the achieved SPDE (up to 74 % at 225K) performance of demonstrated SPAD is the highest ever reported in SAPDs at telecommunication wavelengths (1.31 to 1.55 μm). During dynamic operation, the maximum operation speed of SPAD is usually limited by the afterpulsing effect. Here, this phenomenon of our device is characterized via the double pulse method [2]. Fig. 5 shows the afterpulsing probability as a function of hold-off time for the gate width of 1.5 ns under different ambient temperatures. During these measurements, the chosen V_{ex} is for highest SPDE at each temperature. We can clearly see that the hold-off time required to reduce the afterpulsing probability below 1 % at 225 K and 300 K is 83 and 55.6 ns, respectively. This corresponds to the maximum operation speed at 12 and 18 MHz, respectively. Figure 6 (a) shows the measured full-width half maximum (FWHM) of jitter performance of our device at different ambient temperatures. As can be seen, the measured jitter responses broaden seriously with the increase of ambient temperatures. This phenomenon is usually observed in the InP based SPADs [4] and can be attributed to the increase of thermal noise in our measurement system. Figure 6 (b) and (c) shows the corresponding temporal waveforms at RT and 225K, respectively. As can be seen, the neat, tailless, and Gaussian-like temporal responses can be achieved in both temperatures. According to the above-mentioned dynamic and static results and benchmark as shown in Table 1, we can conclude that our novel SPAD with multiple M-layer design can attain the record-high SPDE (74 %) ever reported in the InP or $In_{0.52}Al_{0.48}As$ based SPADs. Furthermore, our device can attain the excellent dynamic performances in terms of tailless and fast temporal (jitter) response and short hold-off time. Compared with the SPAD with dual M-layer design reported in our previous work [2], by increasing the number of M-layer in this newly demonstrated device, the DCR density can be further reduced due to the suppression of tunneling leakage current. This leads to the enhancement of SPDE (74 vs. 61 %) but degradations in jitter (101 vs. 65 ps) and hold-off time (83 vs. 30 ns). This result verifies that in our demonstrated novel SPAD structure, the number and thickness of each M-layer can be further optimized to get the desired efficiency and speed performances of SPADs operated at telecommunication optical windows.

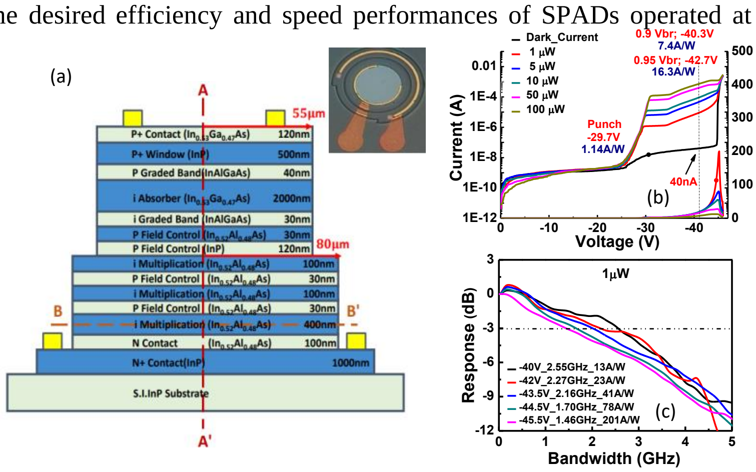

Fig. 1(a) and its inset show conceptual cross-sectional and top views of the demonstrated APDs. (b) shows IV characteristics under different input power. (c) depicts the bias-dependent O-E frequency responses measured under a low input power (1 μW).

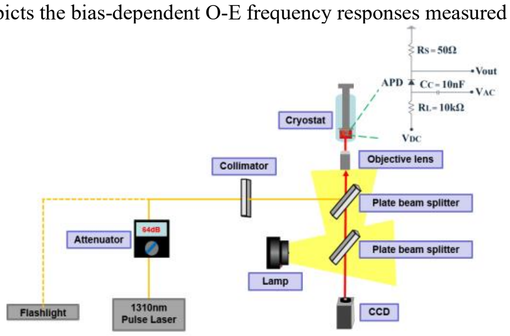

Fig. 2. The conceptual diagram of our measurement setup

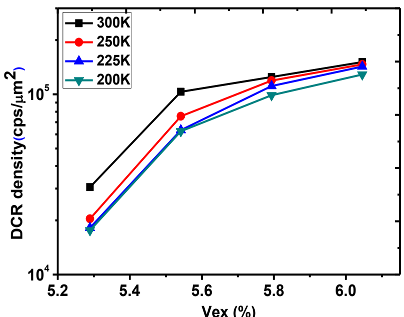

Fig. 3. The measured DCR desnity versus V_{ex} under different ambient temperatures

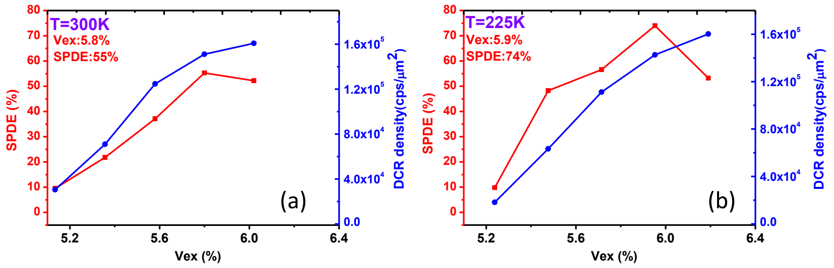

Fig. 4. The measured DCR density and SPDE versus V_{ex} at (a) 300 K and (b) 225 K

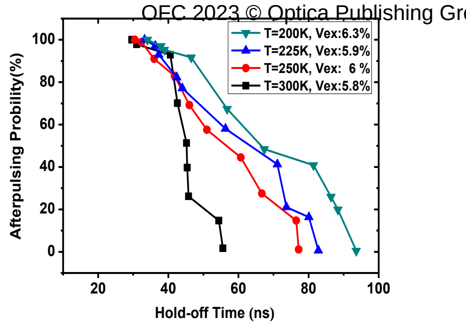

Fig. 5. Afterpulsing probability versus the hold-off time at various temperatures and excess biases.

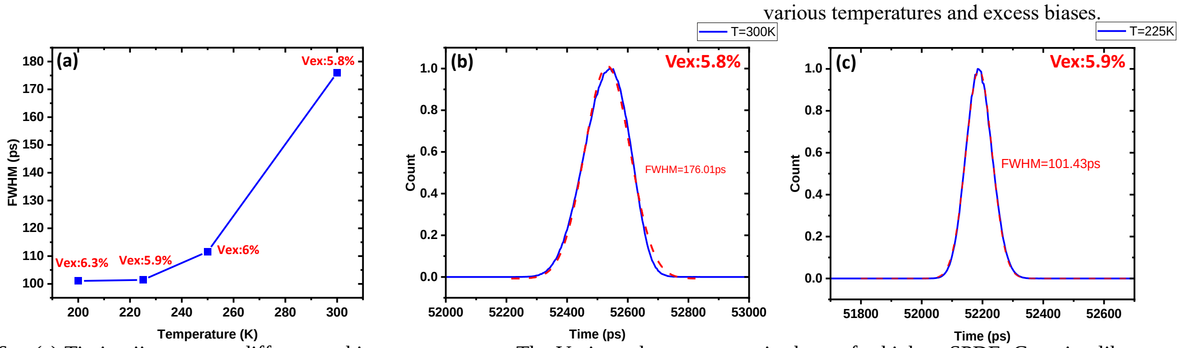

Fig. 6. (a) Timing jitter versus different ambient temperatures. The V_{ex} in each temperature is chosen for highest SPDE. Gaussian-like temporal responses measured at T= 300 K (b) and T= 225 K (c).

TABLE 1

FIGURE OF MERITS OF OUR AND OTHER SPADS

	Material	Diameter (μm)	V_{ex} / V_{BD} (%)	SPDE (%)	DCR (cps/μm²)	P_{AP} (%) @HO time	Jitter (ps)	Diffusion tail (ps)	Temperature (K)
Tosi [5]	InGaAs/InP	25	15	37	24	--	57	360	225
Liu [6]	InGaAs/InP	40	6.4	45	7.5	--	140	400	200
Comandar [7]	InGaAs/InP	--	14	55	--	10.2 @10ns	91	--	293
Fang [8]	InGaAs/InP	25	20.7	60	544	15 @3μs	--	--	300
Signorelli [9]	InGaAs/InP	25	9	30	10.4	5.9 @1μs	119	--	225
Zhang [10]	InGaAs/InAlAs	25	3	35	5.3×10^4	--	--	--	240
Our previous work[2]	InGaAs/InAlAs	60	8.3	61	1.8×10^5	<1 @30ns	65	N/A	200
This work	InGaAs/InAlAs	60	5.8	55	1.6×10^5	<1 @55ns	176	N/A	300
This work	InGaAs/InAlAs	60	6	74	1.4×10^5	<1 @83ns	101	N/A	225

IV. Summary:

In conclusion, we demonstrate novel structure of SPAD with state-of-the-art SPDE and speed performances with a typical passive quenching circuit and under gated mode operation. As compared to the traditional SPAD, the demonstrated novel SPAD structure with additional charge layers inserted into the multiplication region opens the new possibilities to further improve the SPDE, DCR, jitter, and hold-off time performances of SPAD by optimizing the thickness of each M-layer, its E-field inside, and total number of cascaded M-layer.

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