Promising DSP Techniques to Increase Long Haul Transmission Capacity

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Abstract: The state-of-the-art in realtime DSP for long haul coherent optical communication systems is described. We discuss how emerging applications for coherent transceivers may influence DSP design choices.

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1. Introduction

In long haul optical communication systems, how can one design digital signal processing (DSP) algorithms for capacity approaching performance? Fortunately, there are many published descriptions of DSP algorithms that are optimised for coherent transmission systems; some providing a level of detail sufficient to implement an entire software-based DSP chain (e.g., [1,2]). Indeed, there are examples of open source [3] and off-the-shelf commercial libraries providing ready-to-use DSP implementations, which implement near-ideal linear channel equalization.

Efficient use of any communication channel also requires optimizations in coded modulation. Recent developments in bit interleaved coded modulation (BICM)[1] guide us in how to approach this problem. Probabilistic constellation shaping (PCS) – and specifically probabilistic amplitude shaping – has re-emerged as a relatively simple method to approach capacity in linear additive white Gaussian noise (AWGN) channels when paired with ideal forward error correction codes (FEC). Regarding FEC, codecs are known which can arbitrarily approach the AWGN channel capacity [4].

In short, DSP algorithms exist which almost perfectly equalize the (deterministic) linear transmission impairments, modulation can be judicially chosen for spectral efficiency, and it is possible to implement FEC with a negligible gap to capacity. Yet, despite this, realtime DSP implementations have practical constraints which preclude such an ideal implementation for application specific integrated circuits (ASIC). Specifically, ASICs have a limited chip area (finite number of logic gates) and a maximum thermal design power (a limit on the maximum power consumption).

Here, we examine how DSP design can be altered to optimize throughput in long haul fiber transmission links under these design constraints. Three case studies are used: 1) transmission environments where increased spectral efficiency is paramount, 2) pluggables, where ASIC power consumption is strictly limited, and 3) 'high fiber count' subsea cables.

2. Increasing spectral efficiency in bandwidth-constrained transmission systems

The increased performance of optical transceivers over the last two decades can be attributed in equal parts to engineering developments in the field of optical devices and the capability of DSP. CMOS scaling (from the 90 nm process in 2008 to 7 nm in 2020) has increased available digital logic gates for DSP by 20x [5], allowing increased symbol rates, greater chip throughput, and a more powerful and flexible DSP chain. In bandwidth-constrained transmission systems, what are the candidate DSP techniques that can exploit this improved ASIC capability for increased spectral efficiency?

It should be assumed that tighter spectral shaping (reduced pulse shaping roll off) and more advanced FEC can, and will, be used to improve spectral efficiency, as has historically been the case. State-of-the-art ASICs can achieve pulse shapes with just 6.25% excess bandwidth [1], and FEC within approximately 1 dB of the Shannon limit. Further, increased block length PCS can also close the gap to capacity.

For transmission in the weakly nonlinear regime (where interference due to linear and nonlinear effects are approximately equal), algorithms for nonlinearity mitigation do exist [6] which are hardware implementable. Further, modulation schemes can be designed which inherently mitigate fiber nonlinearity [7, 8]. Machine learning algorithms have

[1]BICM is the separation of modulation into two components: the modulation format (e.g., quadrature amplitude modulation) and the binary FEC.

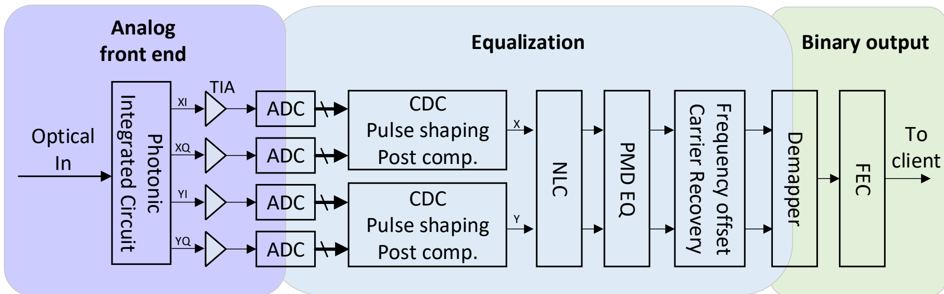

Fig. 1. An example Rx DSP chain (a more complete description can be found in [1]). Note some blocks can be positioned elsewhere in the DSP chain (or at the Tx) depending on the specific algorithm used.

also been proposed which can compensate fiber nonlinearity, along with other, unknown, channel impairments. In the case of [9], the objective is to use machine learning to reduce the complexity of an existing NLC algorithm, which is an approach particularly amenable to hardware implementation.

Machine learning algorithms have also been demonstrated which attempt to replace multiple DSP operations with a blind approach. An advanced example of this is end-to-end learning, which exchanges information between the transmitter and receiver to simultaneously optimise both the encoding and decoding (e.g., [10]). This is attractive because the channel conditions do not need to be known *a priori*, although there are many challenges to be overcome in order to develop a practical implementation, not least to do with realtime adaptation to changes in channel conditions and the requirement of a back channel.

3. DSP for long haul pluggables

For ultra-long haul (e.g., transoceanic) systems, there is no technology that can compete with the performance of high specification optical transceivers. However, recent developments in pluggable coherent technologies (e.g., ZR+, XR [11]) have made low power, high volume modules a viable alternative for a range of shorter, but still long haul, routes.

Pluggable modules are constrained by power consumption, thereby also constraining DSP capabilities. A 400G quad small form factor – double density (QSFP-DD) module has theoretical maximum power consumption in the range of just 38 mW/(Gb/s), decreasing to 31 mW/(Gb/s) for 800G modules [12]. To achieve this, sacrifices must be made in DSP capability, but overall data density may be improved due to the use of compact modules and low power consumption.

Considering Fig. 1, there are some natural areas where the DSP can be optimised for power consumption. First, the chromatic dispersion compensation (CDC) range can be reduced to allow transmission over only a restricted long haul (e.g., <2000 km) or dispersion managed links; implemented as a shortened CDC filter. All but the simplest NLC algorithms would also be unfeasible for low power modules so, again, this is a likely area to scale back the complexity. Finally, the roll-off of pulse shaping filters can be relaxed to reduce filter length; at a cost of spectral efficiency.

In high specification modules, many transmission modes are supported [5]. For example, a range of modulation formats (QPSK, 16QAM, 64QAM, uniform or PCS, etc.) can be paired with a range of FEC rates and implementations. There may also be a range of symbol rates and client protocols to support. Each mode must be implemented in an ASIC and, even when a mode is not being used, the circuits may draw power due to leakage current. Although methods exist to mitigate this issue, restricting the number of operating modes still has the effect of reducing ASIC power and area.

Finally, although there may appear to be some power difference when comparing the requirements single and multi-carrier systems, in practice there are pros and cons to both approaches. Although single carrier pluggables are more prevalent, high-performance multi-carrier systems have also been developed which meet the stringent power limits of QSFP-DD modules [11].

4. Submarine spatial division multiplexing (SDM) cables

SDM can increase submarine cable capacity through optimized use of a cable's limited electrical power feed (PFE) [13–15]. In subsea cables, the power available for signal amplification must be shared between fibers so, while an increased number of fibers per cable results in an increased transmission bandwidth, each will have a lower optical power available and, therefore, a lower SNR for each fiber. However, as capacity scales linearly with bandwidth but only logarithmically with SNR, the overall capacity of the cable increases.

One upshot of lower SNRs is that the optimum modulation order will be reduced. For example, a link which previously had an SNR supporting PS-64QAM in a conventional cable may now only support 16QAM, or even QPSK. The impact on the DSP is that the throughput of the chip is now reduced, meaning that the ASIC may no longer be operating at its electrical power limits. If the ASIC was designed to accommodate this change, then the lower throughput could allow for, e.g., many more FEC iterations, or otherwise increased FEC complexity.

Table 1. OFEC performance, relative complexity, and the impact on SDM cable capacity

Iterations	Decoder Test Patterns	Q [dB] at BER = 10^{-15}	Relative Complexity	Cable Capacity [Tbit/s]
3 SD 2 HD	32	6.45	1.0	528.7
3 SD 2 HD	128	6.30	2.0	547.2
4 SD 2 HD	128	6.27	2.7	551.0

Consider a hypothetical SDM system described in [14] with 220×50 km SSMF spans but with QPSK modulation and OFEC [16] (3 soft + 2 hard iterations, 32 Chase decoder test patterns). Also assume that the ASIC is now operating at roughly a third of its maximum throughput due to the reduction in modulation order to QPSK. The same OFEC with 128 test patterns has approximately double the implementation complexity, but is 0.15 dB closer to capacity. (Note that similar trade-offs in performance and complexity are observed in practical LDPC codes, as noted in [1], section IV-B.) Applying the methodology from [14] to our example system, this leads to a capacity increase of $\sim$3%; see Table 1.

Although individually less significant, other areas of the DSP chain can be adjusted to save power in SDM cabled systems. For example, the lower optical powers result in operation in the (quasi-) linear regime, so we can save power by disabling NLC. If fibers with lower core areas are used, which typically have higher nonlinear coefficients, but lower chromatic dispersion, then power can also be saved in the CDC. Any such power savings could also be used to increase the number of FEC iterations, thus achieving a performance that is closer to capacity.

Note that the intention, here, is not to advocate for a particular fiber type or design choice. Rather, it is to show that the link and DSP design choices are inherently connected. DSP designers should therefore accommodate forthcoming changes to link design in next generation ASICs to be able to exploit advantages that are intrinsic to these systems.

5. Conclusions

Emerging applications of digital coherent transceivers require us to revisit DSP design to optimise performance under new constraints. The recent move towards coherent pluggables for long haul presents a particular challenge for coherent ASICs due to the module power limitations. Having a restricted set of operating modes, limited transmission reach, and single carrier operation are all candidate power saving methods. We also showed how the change in operating SNR when moving from conventional to SDM subsea systems can allow for an overall improvement in DSP performance; provided the capability to exploit this change is incorporated in the ASIC design.

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