System-on-Chip Photonic Integrated Circuits in Silicon Photonics and the Role of Plasmonics

Claudia Hoessbacher[1*], Benedikt Baeuerle[1], Eva De Leo[1], Wolfgang Heni[1], Stephan Koch[1], Juerg Leuthold[2]
[1]*Polariton Technologies AG, 8803 Rueschlikon, Switzerland*
[2]*ETH Zurich, Institute of Electromagnetic Fields (IEF), 8092 Zurich, Switzerland*
**Author e-mail address: claudia@polariton.ch*

Abstract: This paper reviews photonic integrated circuits on silicon photonics. We focus on system on chips in applications for optical communications, sensing, and quantum technologies, and outline the role of plasmonics in silicon photonics. © 2022 The Author(s)

1. Introduction

A photonic integrated circuit (PIC) is a chip that contains optical functions, the optical equivalent of an electronic IC. From data communications [1], through sensing [2], to quantum technologies [3], PICs are central to the current and future digital economy. Just as it is possible to produce a chip with millions of transistors on it, it is possible to produce a chip with millions of photonic devices to manipulate light. Fitted with the right building blocks (BBs), such chips can efficiently realize complex photonic system on chips (SoCs). Integrated photonics was first proposed by Miller in 1969 [4] and, since then, made significant progress on various technology platforms. However, while there have been lots of research efforts for various applications, the main commercial driver of PICs today is optical communications.

In this paper, we review the progress of technology and processes from individual BBs towards fully integrated SoCs. The focus lies on silicon photonics that leverages the capabilities of fabrication tools of the semiconductor industry. We examine state-of-the-art PICs deployed in optical communications and future generations of PICs with a focus on plasmonics and complex applications that will enable PIC scaling and a more ubiquitous use of PICs.

2. Challenges of today's PICs

In practice, PICs face significant challenges (see also [5, 6]):

1. PICs are based on demanding manufacturing processes. While fabrication processes are similar to those used in electronic ICs, active photonic devices require a much more diverse set of semiconductor materials that are harder to control and manufacture. Therefore, they do not yet reach acceptable scale and costs.
2. Today's PICs cannot yet deliver the performance (speed, size, and efficiency) required for upcoming applications. Fundamentally, photonics devices are significantly larger than electronic devices. They are limited by the optical wavelength which is much larger than the electron size limit in electronics and hence are not subject to the same level of dimensional scaling.
3. Besides optical communications, few applications that require large-scale integration have been identified. Many BBs are still rather basic, so that photonic circuit design requires specific photonics know-how and is not accessible for a broader audience of circuit designers.

After the conceptual proposal in 1969, it took time to develop the necessary materials and integration techniques. PIC technologies have matured rapidly in recent years, driven by the cost-effective manufacturability offered by international foundries and applications in optical communications. Multiple material platforms operating at telecom wavelengths have enabled transceiver products. Recent advances (germanium on silicon, silicon nitride) are now allowing to move to other wavelengths which is important for new applications. However, the community has to rapidly scale complexity and develop new BBs to realize practical photonic SoCs.

3. The demand for Building Blocks

A set of building blocks is required to construct complex PICs. A simple optical communication system, for example, requires lasers, phase-shifters, modulators, waveguides, and photodetectors. Additional functionality (polarization diversity, multiplexers…) is needed for complex systems such as coherent communications. The BBs are the toolkit for the development of PICs and are the result of many iterations. PIC designers can choose various functions from so-called process design kits (PDKs) provided by the foundries to build integrated circuits by optical routing. A PDK is typically compatible with specific design tools and provides a parametric design environment. Comprehensive reviews on silicon photonics building blocks can be found in [7, 8].

Disclaimer: Preliminary paper, subject to publisher revision

4. Current PICs for Optical Communications

The transformation of silicon photonics from a promising research field to commercial success was accompanied by various major milestones fueled by the potential for lower cost and size due to high-volume production and semiconductor integration technology [8]. First volume-manufactured silicon photonics products were transceivers for datacenters, developed by Luxtera and launched in 2007. In 2014, Acacia Communications brought silicon photonics into the telecommunications market for longer communication ranges, launching the first coherent modules. In 2016, Intel, which has been developing their own silicon photonics platform for more than 10 years, launched 100 Gbit/s parallel single-mode (PSM) transceivers for cloud and data center applications. Inphi (now Marvell) announced 100G PAM-4 dense wavelength division multiplexing (DWDM) products for inter-datacenter communications in 2017. Cisco acquired Luxtera in 2018 and Acacia in 2021 gaining access to silicon photonics technology. These are just a few examples of the many milestones accomplished in the field. Currently, typical data rates are 100…400 Gbit/s (symbol rates: 25…50 GBd) with 800 Gbit/s (100 GBd) under development. An overview of optical coherent systems in silicon photonics can be found in [1].

5. The Evolution of High-End PICs and Plasmonics

5.1. Brief Introduction to Plasmonic PICs

The complexity of PICs will grow over the years but shrinking of photonic components is not possible due the diffraction limit of light. Fundamentally, the size of the photonic components cannot be much smaller than the wavelength of light (~1500 nm). As a comparison, today's silicon transistors feature size are smaller than 10 nm. Since PICs are comparably large and do not require the expensive wafer area of advanced CMOS nodes, they are mostly realized in 45 nm nodes or higher, compared to the 7 nm nodes used for electronic ICs [9]. With increasing complexity, PIC chip sizes are in risk of increasing drastically, along with exploding costs since chip designers pay per wafer area.

Therefore, our efforts focus on the development of plasmonic PICs that are fundamentally smaller (µm scale) than conventional PICs and enable complex optical functionality on a most compact footprint. Plasmonic devices use metal for guiding light which has the advantage that they serve as their own electrical contacts. Due to small RC time constants and since there is no walk-off between electrical and optical waves, switching speeds up to 500 GHz were demonstrated [10]. Under the right conditions, optical signals can be converted to plasmonic ones and vice versa. Therefore, plasmonic PICs can be seamlessly integrated into the existing silicon photonics platform, enabling a broad range of applications, see Fig. 1.

5.2. Sensing Applications

Applications in sensing were among the first conceived for silicon photonics [8]. Examples are fiber gyroscopes, bio sensors (e.g. for viral infection diagnosis), gas sensors (e.g. CO sensors), 3D imaging (LiDAR, optical coherence tomography) and water pollutant monitoring. With diabetes being a major health challenge in the 21st century, glucose monitoring is an important application. However, the transmissivity change of merely 0.5% poses a major challenge for absorption spectroscopy methods [2]. Startups such as Indigo and Rockley Photonics employ silicon photonics to enable non-invasive, continuous glucose monitoring. In 2021, Intel announced to bring its expertise and manufacturing capability in silicon photonics to develop a LiDAR SoC for use in autonomous vehicles starting in 2025 [11].

Research activities that reconcile PICs with plasmonic structures are ongoing, potentially paving the way towards disposable, mass-produced sensors. Plasmonics provides a strong field enhancement over small volumes enabling strong light-matter interaction. Examples for its use in sensing applications include on-chip surface-enhanced Raman spectroscopy (SERS), a technique that uses plasmonic enhancement to probe analytes in small volumes, such as the one reported in [12]. Given the compactness of these sensor, one can foresee a chip, capable of containing dozens or

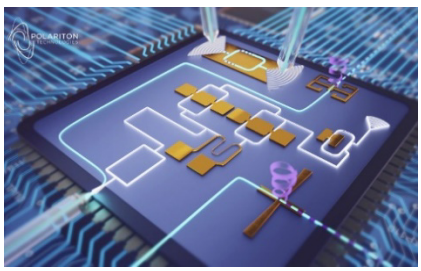

Fig.1: Vision of Plasmonic PICs that enable complex optical functionality on a compact footprint.

hundreds of them. We consider that sensing applications will benefit from plasmonic enhancement and the small size of the PIC. In the future, electronic intelligence might be included to create intelligent sensor networks.

5.3. Quantum Technologies

The current boom in quantum technologies demands for devices that provide higher performance and have some potential for scaling. The run for higher qubit count in quantum computing drives the development for specialized high-end components to carry, manipulate, and store light. In this regard, photonic quantum computing already demands for specialized PICs [13] and the trend is going to increase clearly, supported by start-ups such as Xanadu, PsiQ, and QuiX. On the other hand, quantum sensing already has a well-established industry with the laser-based nitrogen vacancy sensors in diamonds for microscopy or sensing of other physical characteristics with for instance quantum dots. By using quantum effects, measurement sensitivity and precision can be efficiently increased, but also size, energy efficiency and weight can be optimized [3]. For this, efficient field-sensors, detectors, and single photon detectors will be integrated on a PIC platform in the near term.

To allow for efficient scaling of quantum computers, photonic communication links are of particular interest. Controlling and interfacing superconducting (quantum) logic, energy-efficient and scalable interfaces are needed. Recently, our team has demonstrated cryogenic operation of a plasmonic modulator as an energy-efficient (449 aJ) and scalable interface for quantum systems [14]. This is the first demonstration in this domain, and there are new ideas of using plasmonics for quantum technologies e.g. in quantum key distribution [15].

5.4. Hybrid/Heterogenous/Monolithic Integration

The question of whether electronic ICs and PICs should be on the same wafer is primarily a question of costs and time to market. The feature size mismatch between electronic ICs and PICs drives the use of different nodes and thus hybrid integration (adjacent chips) of known good dies, while there are only few attempts of monolithically integrating both ICs on the same wafer [16, 17].

Similarly, most PICs today use disaggregated lasers due to reliability and integration challenges [9]. This means that the laser is on a separate III-V chip fiber-coupled to the silicon PIC. However, PICs with integrated lasers have been commercialized (Juniper, Intel) and promise reduced complexity of connecting and cooling remote lasers. III-V material may be bonded (heterogeneous integration) or epitaxially grown (monolithic integration). To reduce the failure rate of the system, a redundant laser per optical channel was added to such structures [18].

Whether plasmonic functionality is hybrid, heterogeneous, or monolithically integrated with the PIC depends on many questions, mainly reliability, process integration, and costs. Regarding process integration, plasmonic components currently rely on materials that are not CMOS compatible. However, they can be monolithically processed on top of another chip as the last step and this way does not affect the standard process flow [19]. Further, being CMOS compatible only translates into low costs if the product has a high-volume market and costs are dictated by efficient use of wafer real estate which requires photonic device sizes to shrink significantly.

6. Conclusion

In conclusion, silicon photonics is growing rapidly, with plasmonics playing an important role. Manufacturing processes and performance will continue to improve and allow for complex SoCs to be used in more and more applications.

References

[1] C. Doerr, and L. Chen, Proc. IEEE **106**, 2291-2301 (2018).
[2] R. Baets, in *2021 Optical Fiber Communications Conference and Exhibition (OFC)*, (2021), pp. 1-42.
[3] E. Pelucchi, et al., Nature Reviews Physics **4**, 194-208 (2022).
[4] S. E. Miller, The Bell System Technical Journal **48**, 2059-2069 (1969).
[5] I. P. Kaminow, J. Lightwave Technol. **26**, 994-1004 (2008).
[6] F. Kish, et al., IEEE J. Sel. Top. Quantum Electron. **24**, 1-20 (2018).
[7] B. Jalali, and S. Fathpour, J. Lightwave Technol. **24**, 4600-4615 (2006).
[8] A. Rahim, et al., Proc. IEEE **106**, 2313-2330 (2018).
[9] N. Margalit, et al., Appl. Phys. Lett. **118**, 220501 (2021).
[10] M. Burla, et al., Apl Photonics **4**, 056106 (2019).
[11] B. Barrett, "Mobileye Puts Lidar on a Chip—and Helps Map Intel's Future," (2021), https://www.wired.com/story/mobileye-lidar-on-a-chip-intel/2022.
[12] A. Raza, et al., APL Photonics **3**, 116105 (2018).
[13] D. Llewellyn, et al., Nature Physics **16**, 148-153 (2020).
[14] P. Habegger, et al., "Plasmonic 100-GHz Electro-Optic Modulators for Cryogenic Applications," in *ECOC 2022, 48th European Conference on Optical Communication* (2022).
[15] M. Cherchi, et al., in *Integrated Optics: Devices, Materials, and Technologies XXVI*, (SPIE, 2022), pp. 46-62.
[16] L. Zimmermann, et al., in *Optical Fiber Communication Conference*, (Optical Society of America, Los Angeles, California, 2015), p. Th4E.5.
[17] A. H. Atabaki, et al., Nature **556**, 349-354 (2018).
[18] S. Fathololoumi, et al., J. Lightwave Technol. **39**, 1155-1161 (2021).
[19] U. Koch, et al., Nature Electronics **3**, 338-345 (2020).