Advancements in heterogeneously integrated silicon photonics for IMDD and coherent data transmission

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Abstract: Explosive growth of datacenter traffic drives rapid scaling of optical interconnects architectures and technologies. We summarize the advancements in Intel's heterogeneously integrated silicon photonics manufacturing platform enabling throughput scaling for IMDD and high-efficiency coherent links.

1. Introduction

Continuous growth in data analytics, AI and machine learning applications are driving rapid growth of network traffic in the datacenters and require scaling of the switch capacity, optimization of the network architectures, and data throughput of the optical transceivers. Scaling of optical interconnect bandwidth can be accomplished thorough increase in the baud rate, number of lanes (including number of fibers, wavelengths), implementing polarization division multiplexing and higher order modulation formats. Each of these technologies has advantages and constraints especially when viewed through the requirements of different optical interconnects applications.

Several generations of Ethernet transceivers deployed in the data center in the last decade utilize intensity-modulated direct detection (IMDD) with Pulse Amplitude Modulation (PAM) 2-level or PAM4 modulation and one to eight lanes architectures. IMDD transceiver architectures can continue to scale in data throughput, for example, scaling the baud rate from 53 to 106Gbaud for PAM4 modulation enables 1.6Tb/s solutions while preserving transceiver architectures developed for 800Gb/s pluggable modules (800G DR8 and 800G 2xFR4), radix, and backward compatibility. Such pluggable transceivers and co-packaged solutions can be directly deployed in the established datacenter networks topologies and can further scale in throughput to 6.4Tb/s by increasing the number of lanes. However, due to the impact of chromatic dispersion at higher baud rates, the longer reach links (10km) currently serviced by 400G LR4 transceivers are challenging using Coarse Wavelength Division Multiplexing (CWDM) grid and will require narrower wavelength channel spacing.

Alternatively, coherent detection has significant advantages over direct detection in terms of receiver power sensitivity, bandwidth efficiency, and tolerance to optical impairments. Furthermore, the higher sensitivity offered by coherent detection can be used to enable novel network architectures that incorporate all-optical routing/switching without requiring additional amplification. However, deployment of coherent transceivers for short reach applications is impeded by power consumption, cost and complexity of optical components and digital signal processor (DSP). Although analysis presented in [1] concludes that with optimization for data center links, the power consumption of coherent DSP could approach the level of direct detection PAM systems, the power efficiency and manufacturability of optical coherent transceivers needs to be addressed through advancements in photonic integration.

Further reduction in power consumption in coherent transceivers has been proposed and demonstrated using analog coherent detection [2]. In this implementation, optical phase locked loops lock and track the phase and frequency of the receiver local oscillator (LO) to the incoming signal eliminating the need for DSP-based carrier recovery. Analog coherent systems implemented using chip-scale integration of the tunable LO lasers enable low feedback loop delay and therefore high loop bandwidth with relaxed requirements for laser linewidth.

Finally, new Optical-IO interfaces are being defined to meet compute node scaling for data intensive computations requiring distributed computing and disaggregated memory banks. These include architectures with a floating dense wavelength division multiplexing and NRZ modulation format to meet the requirements of throughput per fiber, latency, and power efficiency [3].

Scalability in throughput, density, and power efficiency of all optical interconnect technologies listed above relies on high density photonic integrated circuits that combine laser arrays with high-bandwidth modulators, detectors, and a multiplicity of passive components. In this paper, we review Intel heterogeneous Silicon photonics (SiP) manufacturing platform focusing on advancements in lasers and semiconductor optical amplifiers (SOAs) that

enable development of SiP integrated circuits for multiplicity of optical interconnects applications including scaling of IMDD and coherent.

2. Heterogeneous silicon photonics platform and key enabling capabilities for scaling transmission throughput

Heterogeneous SiP integration platform has been used for manufacturing of high functionality photonic integrated circuits (PICs) with multi-channel (4-32) laser arrays and operating temperature range in excess of 80ºC. The fabrication process is schematically illustrated in Fig. 1a) and detailed in [4]. Several features of the fabrication flow make this platform especially attractive for manufacturing high-density and efficiency PICs: (1) low loss adiabatic coupling between the gain sections and underlying Si waveguide, (2) high accuracy of laser array wavelength targeting using CMOS manufacturing tools for the grating and/or other laser cavity elements, (3) flexibility in the IIIV gain material, which can be optimized for the desired functionally since different epitaxial material can be used in different parts of the PICs, (4) flexibility of using optical amplification to offset loss in increasingly more complex/larger PICs, (5) compatibility with passive fiber attach techniques, and (6) on chip high-density integration of all required photonics functional elements including high-speed modulators, photodetectors, and all required passives components for full (C)WDM IMDD or dual polarization in-phase quadrature modulation and coherent detection optical transceiver functions.

In addition to enhancing functionality, density, and performance, the heterogeneous integration platform reduces the manufacturing cost of PICs and final products. On-wafer test of full optical PIC functionality and wafer-level burn-in for lasers and SOAs dramatically reduce cost and increase manufacturing throughput. Furthermore, high degree of photonics integration drives drastic reduction in the number of photonics and micro-optics components, eliminating multiple high-precision alignment steps, and reducing overall packaging complexity allowing for improved module assembly yield and cost. Excellent laser reliability has also been validated through stringent accelerated life tests and product field data demonstrating the maturity of this heterogeneous manufacturing platform [5].

Figure 1b-d) presents some examples of heterogeneously integrated laser performance including on wafer wavelength distribution for 800Gb/s 2xFR4 PICs (b), spectral characteristics of a tunable laser integrated into coherent PIC (c), and SOA gain vs output power (d).

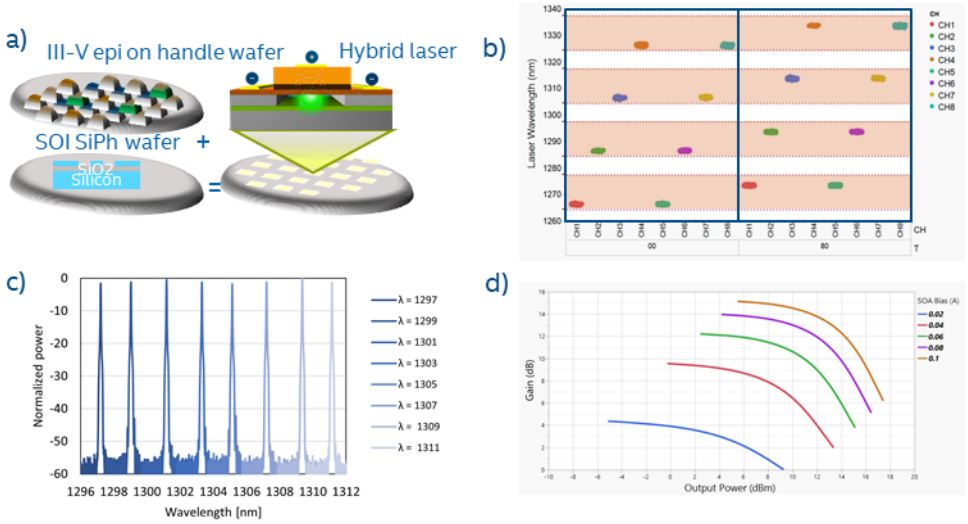

Figure 1: a) Manufacturing flow for heterogeneously integrated lasers, b) Wavelengths of 8-channel laser array measured across 300mm wafers for 800Gb/s 2xFP4 PICs at 0ºC and 80ºC, c) Spectra of a tunable laser integrated into coherent SiP PIC, d) SOA gain vs output optical power at several SOA bias currents.

Intel's heterogeneous SiP platform has enabled rapid product development and high-volume manufacturing ramps for several generations of IMDD pluggable Ethernet transceivers delivering an eightfold increase of throughput from 100Gb/s to 800Gb/s in the last years [6-8]. Furthermore, high bandwidth density and power efficient 1.6Tb/s photonics engines co-packaged with the switch ASIC demonstrated full compliance with Ethernet standards [9]. Heterogeneous SiP platform also enables new PIC architectures for Optical Compute Interconnects, for example, PICs with 4 Tbps bidirectional IO bandwidth have been demonstrated by integrating eight channel

laser arrays on a floating DWDM grid with tandem arrays of micro-ring modulators used as filters and modulators [10]. Such architecture can continue to scale to 10's of Tb/s by increasing the number of wavelengths, baud rate, number of fibers, and employing polarization division multiplexing.

3. Summary

In summary, we have reviewed the vectors of transmission capacity scaling for 1.6Tb/s and beyond and the scalability of Intel heterogeneous SiP platform to deliver performance, high density, power efficiency, and manufacturability for IMDD and coherent optical links.

4. Acknowledgements

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5. References

[1] X. Zhou, R. Urata, and H. Liu, "Beyond 1Tb/s Datacenter Interconnect Technology: Challenges and Solutions", OFC 2019.

[2] T. Hirokawa, "Analog Coherent Detection for Energy Efficient Intra-Data Center Links at 200 Gbps Per Wavelength", Journal of Lightwave Technology, Vol. 39, No. 2, 2021, pp. 520-531.

[3] L. Liao, "High Density Silicon Photonics for Co-packaged Ethernet Switches and XPUs", Tutorial W4H.3, OFC 2022.

[4] R. Jones et al., "Heterogeneously integrated Photonics," IEEE Nanotechnology. Mag., vol. 13, no. 2, pp. 17-26, 2019.

[5] R. Jones, "Overview and Future Challenges on III-V Integration Technologies in Silicon Photonics Platform", OFC 2021.

[6] H. Yu et al., "100Gbps CWDM4 Silicon Photonics Transmitter for 5G applications", W3E.4, OFC *2020*.

[7] H. Yu et al., "400Gbps fully integrated DR4 silicon photonics transmitter for data center applications", T3H.6, OFC 2020.

[8] H. Yu et al., "800 Gbps Fully Integrated Silicon Photonics Transmitter for Data Center Applications", M2D.7, OFC 2022.

[9] S. Fathololoumi et al., "1.6 Tbps Silicon Photonics Integrated Circuit and 800 Gbps Photonic Engine for Switch Co-Packaging Demonstration", Journal of Lightwave Technology Vol. 39, Issue: 4, 2021.

[10] S. Fathololoumi et al., "Highly Integrated 4 Tbps Silicon Photonic IC for Compute Fabric Connectivity", Hot Chip, 2022.