Silicon Photonics for Next-Generation Optical Connectivity

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Abstract: We review advancements in silicon photonic (SiPh) devices and integrated circuits (SiPICs) to enable high density, low power, multi-Tb/s optical solutions for next-generation Ethernet networking and compute connectivity.

1. Introduction

Technologies such as video streaming, social networking, artificial intelligence (AI), and machine learning (ML) are driving exponential growth in data center traffic and accelerating demand for compute capacity. They have led to the buildout of hyperscale data centers that increased networking bandwidth (BW) 80X since 2010 [1]. At every bandwidth transition, however, the growth of networking power outpaced that of server and IT power, leaving less and less of the total power to "value-add" compute [2]. One promising approach to save networking power is to improve the BW density of optics and co-package them with the switch ASICs. This new architecture would reduce the length and RF loss of the electrical channels between the optics and the switch dies to drastically reduce SerDes power. Meanwhile, compute intensive AI/ML workloads are driving the need for distributed computing and memory disaggregation. The resulting scaled-up and scaled-out systems with compute nodes and resources located beyond the board-level will challenge the capability of electrical I/O currently deployed. Like above, co-packaging optics in close proximity of host compute dies, in the form of optical compute interconnect (OCI), can address this I/O challenge and offer superior density, power efficiency, and reach.

Co-packaged optics for both Ethernet and compute connectivity require scaling in size, BW, and power. We review below advancements in key devices fabricated using Intel's 300 mm SiPh platform [3]. They include on-die lasers, semiconductor optical amplifiers (SOAs), modulators, photodetectors, and passive optical components such as de-interleavers, demultiplexers (DeMUXs), and spot size converters (SSCs). We also share the architecture and performance of two highly integrated, high BW SiPICs. The first is a 1.6 Tb/s transmitter (Tx) targeting Ethernet switch co-packaging, and the second is a 4 Tb/s transceiver (TRx) for OCI applications. They are two examples of many possible SiPIC designs using Intel's SiPh device portfolio and fabrication process.

2. SiPh Devices

On-die lasers and SOAs are integrated by bonding III-V gain chips to the SiPh wafer and then using CMOS processes to form the needed device structure. Their wafer-level integration offers 1) highly integrated, high channel count architectures, 2) ultra-low loss coupling to SiPh waveguides, 3) high device reliability with CMOS dielectric films protecting all facets, 4) option for device redundancy to further improve reliability, 5) wafer-level PIC SORT and burn-in, and 6) low cost by eliminating need for laser packaging. Using this integration capability, DFB laser arrays have been qualified for PSM4, CWDM4, FR4, DR4, and LR4 pluggable products. Laser arrays have also been demonstrated for CWDM 20 nm wavelength spacing spanning >140 nm as well as for DWDM wavelengths with 200 GHz spacing. Fig. 1 is an example of measured performance of a 1310 nm laser showing 20 mW optical power in the silicon (Si) waveguide at 80 °C with ~110 mA bias current and <1.55 V bias voltage. The lasers have >45 dB side mode suppression ratio (SMSR) and <-150 dB/Hz relative intensity noise (RIN). Also, accelerated aging tests as well as product field data show high laser reliability with >10 year lifetime and <2 failure in time (FIT) rate.

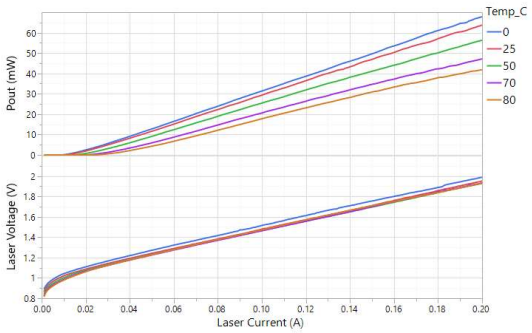

Fig. 1: DFB laser LI and IV from 0°C to 80°C.

SOA integration enhances link performance and enables architectures that are not possible otherwise. For example, it allows for the use of low power lasers for 1xN splitting to improve energy efficiency while also reduce four wave mixing risk that is common in laser sharing designs. It can also simultaneously amplify multiple wavelength-multiplexed data streams to improve energy efficiency by amortizing SOA power consumption over large amounts of aggregate data. Fig. 2 is an example of SOA performance at different bias currents. It offers >12 dBm of saturation power and 12 dB of gain at 80 mA.

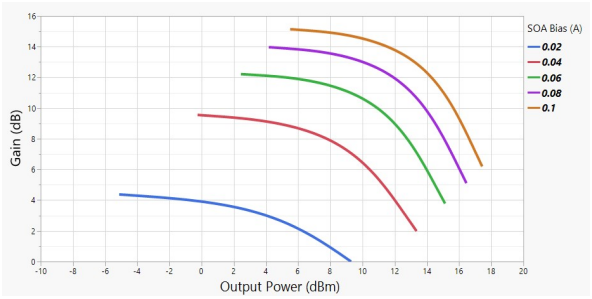

Fig. 2: SOA gain vs. output power at different bias currents.

For high-speed modulation, micro-ring modulators (MRMs) offer compact size for BW density scaling. Using MRMs with reverse-biased Si PN diodes, 106.25 Gb/s PAM4 modulation has been demonstrated with <0.7 dB TDECQ and -0.32 dB C_{eq} with <2 V_{pp} drive [4]. Path to 128 Gb/s NRZ and 240 Gb/s PAM4 has also been demonstrated [5]. MRMs are sensitive to even minor temperature variations, so they require dynamic control during operation. A feedback control loop using monitor photodetectors (PDs) before and after the MRM has ensured zero post-FEC BER for 106 Gb/s PAM4 operation, over both fast thermal transients of 45 °C/min as well as large temperature range of 85 °C, as shown in Fig. 3. For high-speed detection, vertical germanium on Si waveguide PDs (Ge-PDs) offer <100 nA dark current, ~60 GHz BW, and ~0.9 A/W responsivity for both TE and TM polarizations.

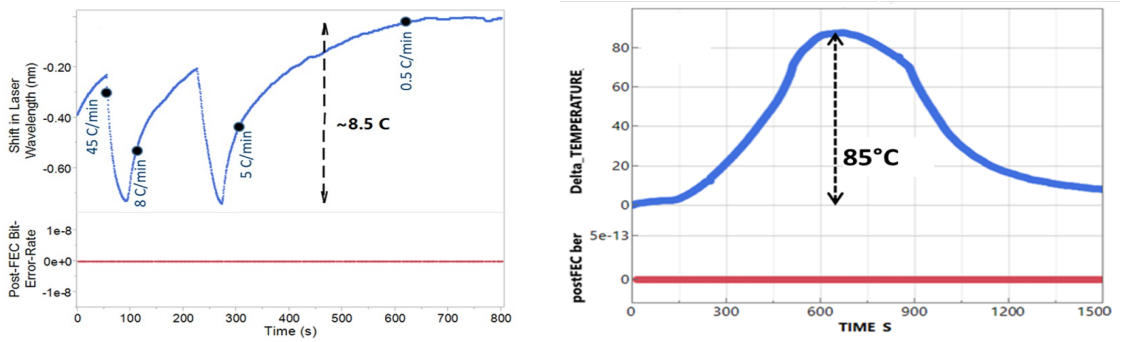

Fig. 3: Dynamic feedback control loop ensured error free operation over large thermal transients and range.

Numerous passive optical devices have also been developed, including Mach Zehnder interferometer (MZI) based switch to support laser redundancy designs, multi-mode interference (MMI) device as wavelength multiplexer and power splitter, MZI de-interleaver to improve optical crosstalk, micro-ring drop-filter as compact DeMUX, polarization splitter-rotator-combiner (PSRC) to manage receiver polarization, and inverse-taper SSC to mode-match Si waveguide and single-mode fiber (SMF). Some notable performance results are 1) de-interleaver has 20 dB adjacent channel crosstalk and <0.5 dB propagation loss, 2) ring drop filter has ~0.55 nm 3-dB BW and <1 dB loss, and 3) SSC has low polarization dependence with ~0.8 dB taper loss and ~0.5 dB active alignment coupling loss. Passive optical alignment using SSC and integrated V-groove shows mean coupling loss of ~1.2 dB.

3. SiPICs

For Ethernet switch co-packaging, SiPICs have been demonstrated supporting IEEE standards compliant DR4 optical interface. They include 1.6 Tb/s Tx PICs, Rx PICs, and 800 Gb/s TRx PICs. Their Tx and Rx channel architectures are shown in Fig. 4. For the 1.6 Tb/s Tx, 32 on-chip lasers support a pair of redundant lasers for each of the 16 optical channels. This full laser redundancy design greatly improves FIT rate of laser arrays. For example, for a 51.2 Tb/s switch where 512 lasers are needed to support 512 channels of 106.25 Gb/s PAM4, laser redundancy can improve laser related system FIT to ~0.1 even for lasers with individual FIT rate of 10. Following the 32 Si lasers on the SiPIC are MZI switches with phase tuners to select the operating laser from each redundant laser pair. The laser light is then modulated using MRM, with integrated heater and Ge-PDs as part of a dynamic control loop to optimize and maintain the MRM bias point insertion loss. Modulated light is then expanded using integrated SSCs. V-grooves are formed on-die to allow for low-cost passive alignment to SMF. Fig. 5 shows 106.25 Gb/s eye diagrams of eight of the 16 channels. Performance is in good agreement with simulations and shows repeatable performance, with TDECQ of 1.7-2.1 dB. This SiPIC has edge BW density of >300 Gb/s/mm.

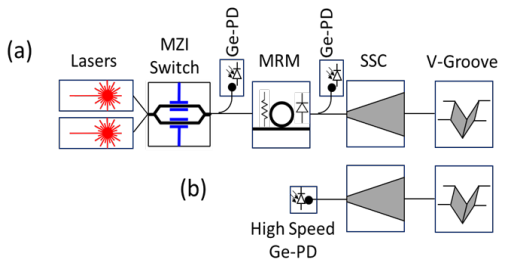

Fig. 4. SiPIC architecture for a) Tx and b) Rx channels.

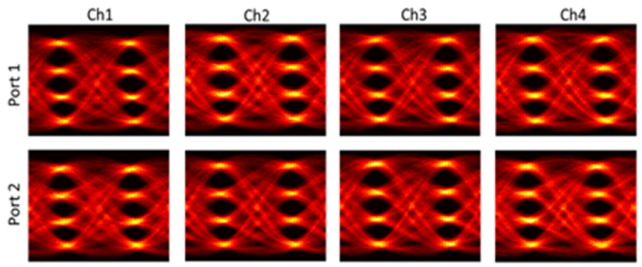

Fig. 5. Measured 106.25 Gb/s PAM4 Tx eye diagrams.

For OCI, a SiPIC capable of 4 Tb/s is designed to aggressively scale BW density, energy efficiency, and latency. Its architecture is shown in Fig. 6. The Tx path includes an array of 8 integrated DWDM lasers with 200 GHz spacing. The outputs of the 8 lasers are multiplexed together and split evenly across 8 bus waveguides using a passive WDM MUX/splitter, such that the 8 bus waveguides on the output of this component all carry the 8 wavelengths. Each bus waveguide then feeds an array of 8 cascaded MRMs that each encodes high speed data onto one of the 8 multiplexed wavelengths. After modulation, an integrated optical switch directs the light either to the Rx path for internal Tx-to-Rx self-test or to a booster SOA. SSCs and V-grooves are integrated for low-cost passive alignment. The Rx design targets compatibility with a SMF fiber plant, so it integrates polarization insensitive SSCs as well as PSRCs to manage polarization. Depending on application requirements, an optional Rx SOA can be integrated before demultiplexing the 8 data streams of each Rx bus waveguide. The DeMUX includes a de-interleaver that separates the odd and even optical channels and 8 micro-ring drop filters that direct each channel to a high-speed Ge-PD.

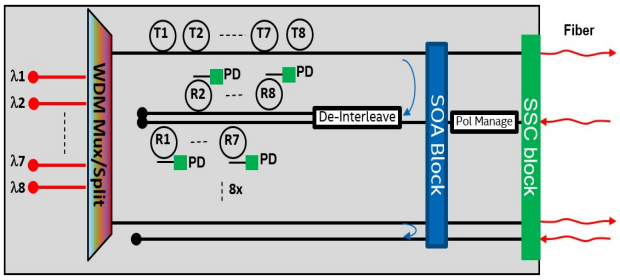

Fig.6: Block diagram of the 4 Tb/s OCI SiPIC architecture.

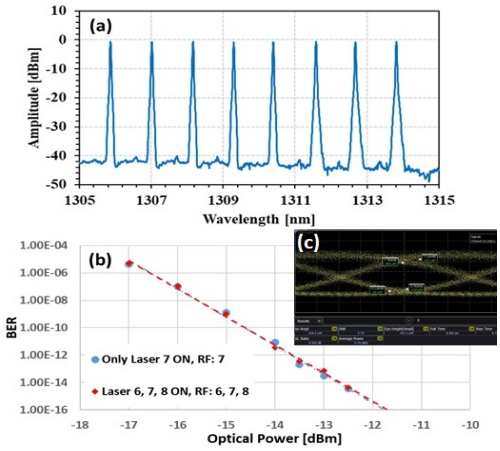

Fig.7: a) Tx output spectrum, b) BER performance at 32 Gb/s, c) Tx eye diagram at 64 Gb/s.

Fig. 7a is the normalized spectrum of the SiPIC Tx output. It shows the targeted 200 GHz channel spacing and >43 dB optical signal-to-noise ratio (OSNR). BER measurement is performed at 32 Gb/s NRZ using a reference PD and TIA. NRZ modulation is of interest because it offers low power and latency. Two test cases are studied: 1) one laser and one MRM are turned on so input power to the SOA is well below its power saturation (Fig. 7b blue), and 2) three lasers and three MRMs are turned on, and laser and SOA biases are increased so the SOA output power is equivalent to that of intended SiPIC operation (Fig. 7b red). Data shows no penalty from having higher power in the SOA and having it amplify multiple modulated data streams at the same time. It confirms minimal four wave mixing and cross-gain modulation effects and shows no observable BER floor. Testing is also performed at 64 Gb/s, and a sample Tx eye diagram is shown in Fig. 7c. This SiPIC has bi-directional edge BW density of >800 Gb/s/mm.

4. Summary

Using Intel's 300 mm SiPh platform, a large portfolio of optical devices has been demonstrated to drive scaling of BW density and power efficiency. They have enabled multi-Tb/s SiPICs with integrated lasers for both Ethernet switch and compute co-packaging.

5. References

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