# Polarization mode dispersion in CMOS-integrated monolithic SiPh components: simulations and experiments

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**Abstract:** We simulated and experimentally characterized the differential group delay induced from polarization mode dispersion (PMD) of key components on a monolithic SiPh platform. Strategy for compensating PMD was introduced for high-speed applications beyond 100 Gbit/s. © 2023

## 1. Introduction

As the datacom and telecom industries transition from electrical to optical interconnects, there is a growing demand to improve the scalability, power consumption, and cost efficiency of photonic interconnection schemes. Monolithic SiPh technologies, among others, have been recognized as a highly attractive solution for meeting these challenging requirements by enabling the large-scale manufacturing of state-of-the art photonics and CMOS devices and circuitries on the same chip [1-2]. With the potential to offer ultra-low parasitic integration, a monolithic approach allows to build faster, and more energy efficient transceivers as compared to the conventional hybrid integrated solutions using 2.5D- or 3D-packaging, while opening avenues for a variety of other emerging applications.

To enable an optimized process and allow full realization of the system benefit, the waveguide (WG) layers incorporated in the monolithic technology are typically thinner than those in the hybrid SiPh solutions [3-4]. However, this results in non-negligible birefringence and PMD for various WGs and functional devices. Due to PMD, the TE and TM modes typically propagate at different speeds, which then results in a polarization-dependent time difference $\Delta\tau$, also known as differential group delay (DGD) [5]. DGD can cause inter-symbol interference (ISI) and eye diagram distortion for high-speed and wideband applications. Here, we report comprehensive simulations and characterizations of the DGDs associated with monolithically integrated SiPh components. Both wafer- and module-level measurements were conducted to characterize the aggregated DGDs in representative testing structures. Finally, we investigated the system-level impact of DGD for high-data-rate applications. Our simulations showed successful signal recovery for a typical receiver (RX) link after DGD compensation using an optimized WG delay line.

## 2. Polarization mode dispersion in monolithic SiPh components: numerical simulations

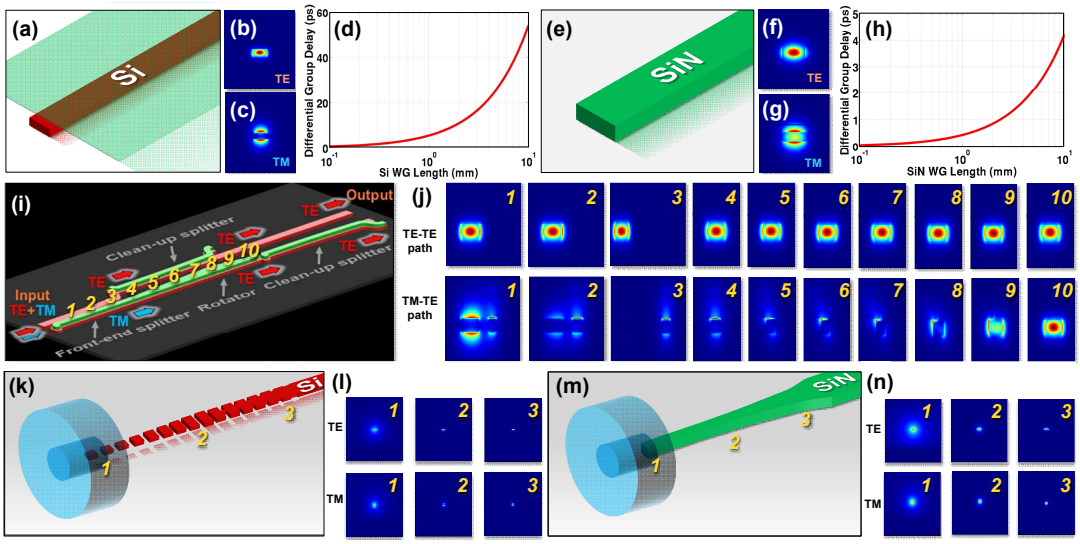


**Fig. 1**. Schematic, TE/TM mode profiles and calculated DGD: (a)-(d) Single-mode Si waveguide. (e)-(h) Single-mode SiN waveguide. Schematic of the PSR (i) and mode profiles (j) at various locations (marked in the 3D perspective view) for the TE->TE and TM->TE paths. Schematics and

mode profiles of edge couplers at various locations for TE and TM polarizations: (k)-(l) Edge coupler (fiber attach) incorporating a Si metamaterial spot size converter (SSC); (m)-(n) Edge coupler based on a multi-stage nonlinear SiN SSC. All the simulations are performed at 1310 nm.

**Table 1.** Summary of the calculated DGDs for representative monolithic SiPh components at 1310 nm

| Device | Si WG | SiN WG | PSR | Si Edge Coupler | SiN Edge Coupler |
|---|---|---|---|---|---|
| **Differential group delay** | 5.4 ps/mm | 0.42 ps/mm | 5.2 ps/device | 0.69 ps/device | 0.06 ps/device |

To gain deeper insight into the PMDs of monolithic SiPh components, we started from the 2D eigenmode simulations of single-mode (SM) Si and SiN WGs [3-4], the essential building blocks for most other photonic devices on the platform. Figs.1(b)-(c) and (e)-(f) show the field profiles of the fundamental modes, which indicates that the TE modes are better confined than their TM counterparts for both WG types. Quantitative analysis revealed that the mode effective index ($n_{eff}$) and group index ($n_g$) of the TE modes are higher than TM. This was a clear indication that higher group velocities ($v_g$) are achievable in the TM path. The calculated DGD as a function of the WG length are shown in Figs. 1(d) and 1(h), respectively, and summarized in Table 1. Compared to SiN WG with the same length (e.g. 1 mm), Si WG exhibits more than one order of magnitude larger DGD (e.g. 5.4 ps vs 0.42 ps).

For more complex functional components such as polarization splitter rotator (PSR) (Fig.1(i)) and edge coupler (Figs.1(k) and 1(m)), we took advantage of the adiabatic nature of the designs and divided the structure into smaller sections that can be approximated as uniform WGs. Then, we calculated the DGD in each section using mode simulations and obtained the total DGD by summing up the time delays in all sections, which was later validated by 3D FDTD calculations. The electric field profiles at representative locations for the PSR and Si and SiN edge couplers are illustrated in Figs.1(j), (l) and (n), whereas the corresponding DGD is summarized in Table 1. Due to greater PMD in well-confined geometries, the PSR suffered from remarkably greater DGD than the edge couplers, while demonstrating smaller group delay than a pure Si WG of the same length due to the presence of hybrid Si-SiN structures and the varying Si widths in the TM-TE path [4], which largely contributed to the PMD recovery. Moreover, the DGD in the Si edge coupler [6] was found to be smaller than its SiN counterpart, consistent with the trend in the SM WG case. Finally, process corner case studies were performed for these functional components. They revealed that tight distributions in the PMD can be reasonably achieved within the current process capabilities for typical components that are used in the RX link for optical interconnect applications.

## 3. Polarization mode dispersion in monolithic SiPh components: experimental characterization

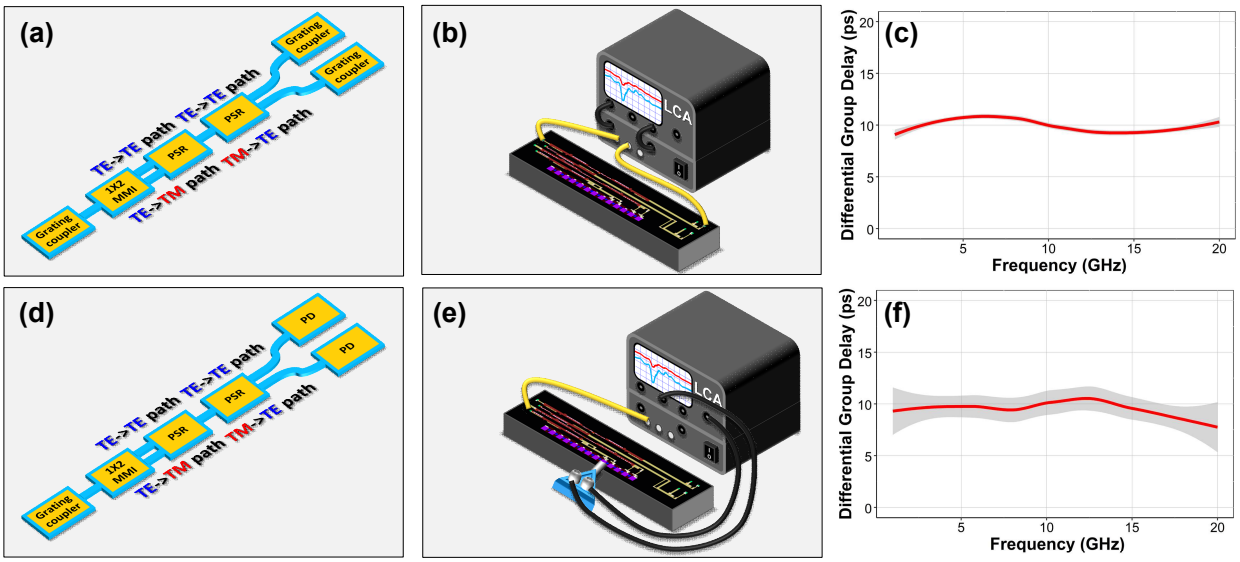


**Fig. 2**. (a)-(c) Wafer-level optic-optic (O-O) measurement of back-to-back connected PSRs with input and output grating couplers: schematic, test setup and measured DGD. (d)-(f) Wafer-level electric-optic (E-O) measurement of back-to-back connected PSR with input grating couplers and output photodetectors: schematic, test setup and measured DGD. To ensure only PSR contributes to the DGD, the waveguides for the TM and TE paths are balanced in both test structures. The operating wavelength is 1310 nm with 2dBm input optical power.

To experimentally characterize the PMD, several test structures and measurement techniques were designed and adopted to enable both wafer- and module-level extraction of the DGD in monolithic SiPh components. Figs.2(a)-(b) and (d)-(e) illustrate the layout schematics and test setups for wafer-level measurement of the PSR group delays using a lightwave component analyzer (LCA) in O-O and E-O configurations. After completing the initial calibration and optical/electrical probe set-up, the S-parameters and the group delays were recorded for both TE and TM polarizations. The DGD can then be calculated by subtracting the two delay values. The corresponding results shown in Figs.2(c) and 2(f) indicate that the aggregated DGD from two PSRs are around 10 ps for both O-O and E-O cases at 1310 nm,

agreeing well with the simulated differential delay shown in Table 1. In addition to the frequency domain measurement, one can also use time domain techniques to measure the differential delay with the assistance of a pattern generator, reference transmitter and optical oscilloscope. From a square wave-modulated optical signal, the measured DGD from the same O-O structure shown in Fig.2 (d) was found to be ~ 9.7 ps, which is consistent with the measurement results using the LCA.

In addition to the wafer-level testing, a V-groove-based loop-back structure was designed to enable module-level characterization of the DGD in Si WGs and edge couplers. As illustrated in the test setup (Fig.3(a)), an optical vector analyzer (OVA) was used to measure the PMD of the photonic chip in the transmission mode. The DGD as a function of the operational wavelength is plotted in Fig.3(b), which shows a ~6.5 ps aggregated DGD for the loop-back structure consisting of Si WGs and two Si edge couplers. Based on the simulated delay values for these individual components (Table 1), the calculated total DGD was estimated to be 6.35 ps at 1310 nm, which matches reasonably well with the OVA measurement.

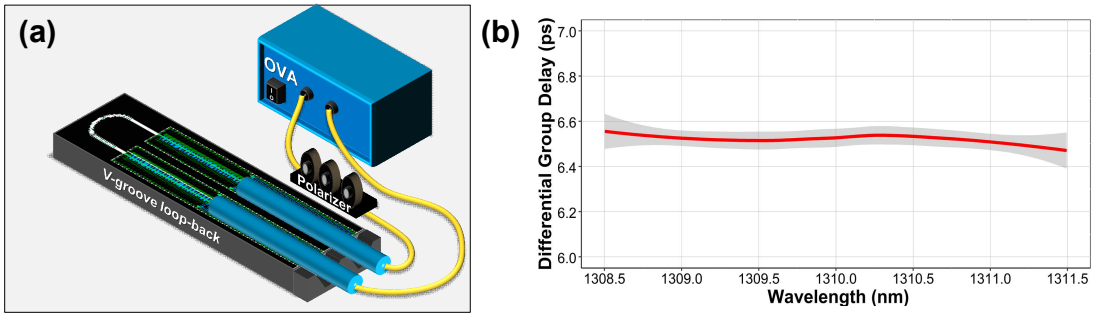


**Fig. 3**. Module-level DGD characterization: (a) Test setup for V-groove based loop-back structure. (b) Measured DGD for a fiber LB showing ~6.5 ps aggregated DGD in the loopback containing two Si-based edge couplers and ~0.92-mm long Si waveguide path.

## 4. PMD compensation for high-speed transceiver applications

PMD and the associated DGD can potentially cause major problems for high-speed coherent optical communication systems [7-8]. This is well-studied for fiber optics [9] but not yet extensively for SiPh. Here, we took a typical RX circuit built using monolithic SiPh components (Fig.4(a)) and studied the system level impact of the DGD effect. Fig.4 (b) shows the impact of a 6 ps DGD on a 100 Gbps PAM-4 signal (20 ps symbol interval) eye diagram seen at the photodetector (PD). The ISI introduced in the received signal closed the PAM4 eye. In Fig.4(c), we incorporated a waveguide delay line in the TM-TE path to compensate for the longer delay of the optical signal in the TE path, the result of which is depicted in Fig. 4(d) which shows an open eye of the PAM-4 signal after the differential delay compensation between the TE and TM paths feeding the dual input PD. Any residual differential delay at the PD (e.g., less than 10% of the symbol interval) can be compensated by the adaptive equalizer in the RX.

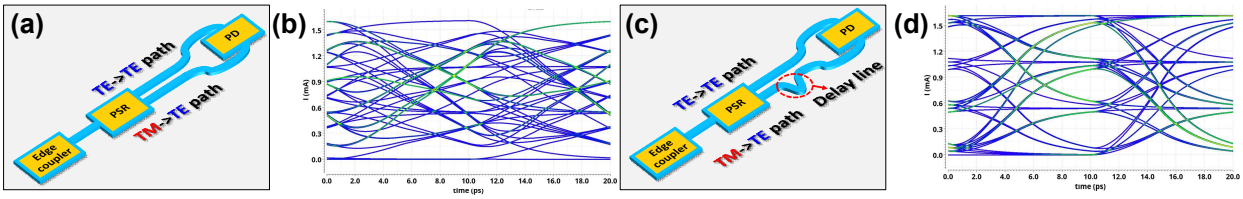


**Fig. 4**. (a) Schematic of a typical RX link. (b) Simulated eye diagram of the 100 Gbs RX path with 6 ps DGD between TE and TM paths (assuming a RX path comprising Si edge coupler, PSR and a short Si WG). (c) Simulated eye diagram of the 100 Gbps RX path with DGD compensation.

## 5. Summary

In conclusion, we have simulated and experimentally characterized the DGDs in several key SiPh components on the monolithic SiPh platform. Additionally, we evaluated the system-level impact of the DGD for high-data-rate applications (e.g. 100 Gbps) and proposed PMD compensation methods to recover the distorted eye diagram.

## 6. References

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