First Monolithically-Integrated Silicon CMOS Coherent Optical Receiver

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Abstract: An O-band coherent optical receiver (CORX) is integrated in a 45-nm monolithic CMOS SOI process. The CORX operates to 80 Gbps with FEC-acceptable BER at 1.2 pJ/bit energy efficiency. To our knowledge, this is the first monolithically-integrated Silicon CMOS CORX.

1. Introduction

As data center traffic continues to grow, intra-data center interconnects require scaling baud rates while reducing power consumption through a transition from OOK to high-order modulation formats. Although intensity-modulation direct detection (IMDD) with high-order pulse amplitude modulation improves spectral efficiency, scaling beyond PAM-4 demands significant power consumption in the transmitter and receiver, resulting in low energy efficiency. Adaptation of the short-reach data center interconnect to quadrature modulation offers an energy-efficient alternative to IMDD links if highly-efficient operation is possible in the coherent optical receiver (CORX) [1].

Recent work has demonstrated coherent optical links above 100 Gbps/wavelength with heterogeneous integration between electronic and photonic ICs [2]. Nevertheless, parasitic components due to wirebond interconnects deteriorate the high-speed performance requiring more power hungry circuitry to compensate packaging effects. Silicon photonic technologies enable a high level of integration by incorporating electronic and photonic components on a single chip. The first fully-integrated coherent receiver at C-band using a photonic BiCMOS 0.25 μm SiGe technology is demonstrated in [3]. However, a survey on optical receivers shows energy efficiency improvements using CMOS technologies [4]. In this case, a high-performance 45-nm CMOS SOI technology ($f_T = 290GHz$) has been adapted to support a process development kit that includes complete optical structures for waveguides, photodetectors, fiber coupling, polarization control structres, as well as ring and Mach-Zehnder modulators [5].

In this paper, we present an O-band I-Q coherent optical receiver operating up to 40Gbaud with record energy efficiency of 1.2pJ/bit, 3.6 times improvement compared to prior O-band monolithic coherent design [6].

2. Circuit Design

Fig. 1 shows the schematic of the high-speed I/Q receiver with an on-chip 90° optical hybrid. The optical hybrid comprises thermal phase shifters and directional couplers used as splitters or optical combiners. A phase shifter

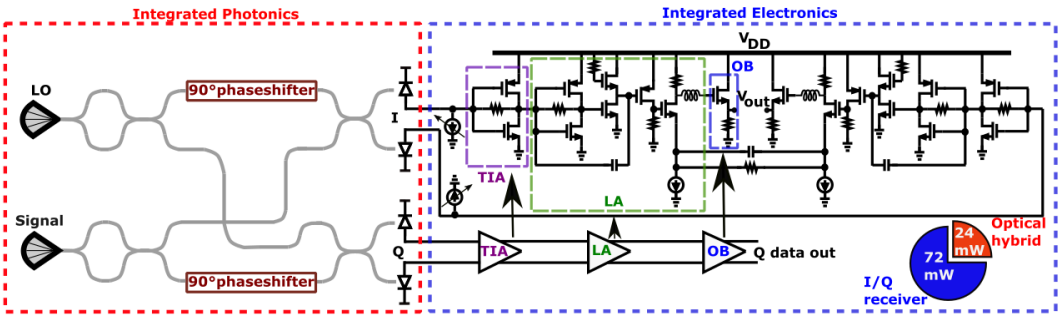

Fig. 1. Optical receiver implemented in 45-nm RF/photonic integrated circuit process consisting of an optical hybrid, a transimpedance amplifier, limiting amplifier and 50Ω output buffer

is placed in the quadrature path to provide a 90-degree phase shift. Two additional phase shifters enable path length matching between the in-phase and quadrature signals and shift the LO to be in-phase with the signal. Phase shifters were preferred over multimode interferometers (MMIs) due to their lower loss and tunability which increases optical efficiency and lowers ISI.

The optical hybrid produces differential optical signals and drives two integrated Germanium photodetectors (PDs). The differential PD current is then amplified through a low-power pseudo-differential push-pull shunt-feedback TIA followed by a second push-pull amplifier stage and a common-source amplifier with active peaking to increase the transimpedance gain. The pseudodifferential architecture avoids the excess power consumption of current-mode circuit techniques by eliminating the tail current source; however, the output buffer is fully differential to provide improved common mode rejection.

3. Measurement Result

The receiver was tested in a self-homodyne link configuration. The measurement setup as well as chip micrograph and assembly on a FR-4 PCB is shown in Fig. 2. A 1310-nm external cavity laser (ECL) splits into local oscillator (LO) and signal paths. In the signal path, an iXblue MXIQER-LN-30 I/Q modulator is driven with a 600-mV PRBS-15 signal from a bit pattern generator (BPG) (SHF 12105A). The signal path also includes an attenuator for sensitivity measurements. The receiver I/Q channels are connected to a real-time oscilloscope (RTO) (Keysight UXR0702A). with a 0.875 µs acquisition time at 256 GSa/s to detect the transmitted QPSK signal.

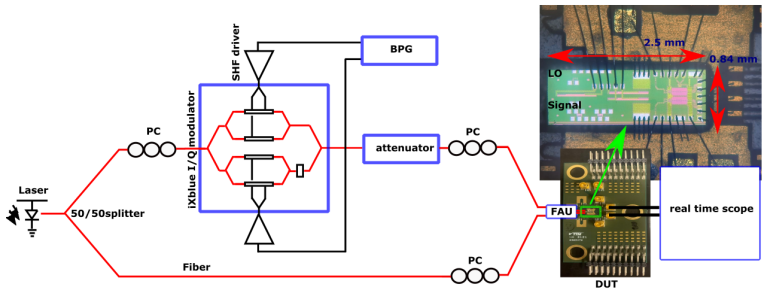

Fig. 2. Self-homodyne link configuration and microscopic view of the chip.

The ECL power is set to 13 dBm providing 10-dBm LO power and 10-dBm input power to the transmitter. The transmitter has a typical bandwidth of 25 GHz and 15 dB of loss at O-band. The 10-dBm LO power and -5.3-dBm signal power translate to 0.59-mA LO and 8-μA signal current per PD indicating 12.2 dB of coupling loss. The differential dual-channel electrical circuit draws 60-mA current from a 1.2-V supply and thermal phase-shifter inside the optical hybrid consumes 24-mW for quadrature bias corresponding to 96-mW dc power consumption for the CORX.

Fig. 3 shows the measured constellations at 20, 32, and 40 Gbaud and bit error rate (BER) as a function of signal power incident at signal grating coupler which is 23 dB larger than signal power at each PD. The single ended output voltage swing is 28 mV for 67-μA (calculated based on signal and LO power) input current per PD driving the TIA showing 415Ω (52.3dBΩ) transimpedance gain.

A performance summary for this design is shown in Table 1 and compared against recent work. FinFet CMOS has indicated excellent power; however, this process does not support silicon photonic integration. When compared with monolithic coherent design in O-band, we achieved a 3.6 times improvement in energy efficiency.

4. Conclusion

This paper describes the performance of a 1.2-pJ/bit coherent optical receiver fabricated in the 45CLO technology that supports both silicon photonic components as well as high speed electronics. Measured constellations and sensitivity curves show performance up to 40 Gbaud below FEC BER limit of 2.2×10^{-3}.

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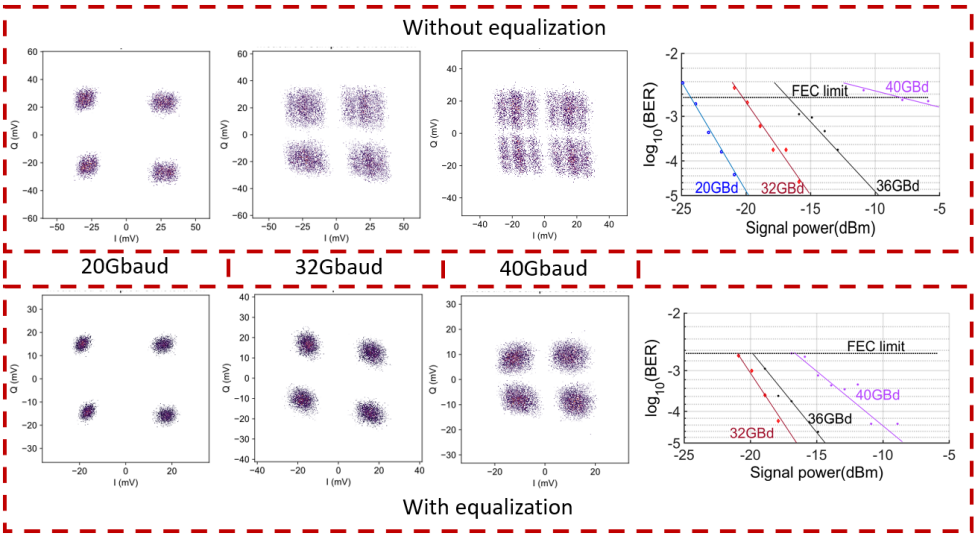

Fig. 3. Measured constellations at 20, 32, and 40 GBd and sensitivity curves. Equalized results use a post-processing script on raw data to apply a 7-tap feed-forward equalizer (FFE) to compensate for bandwidth limitations of TX and RX packaging losses. The equalization adds 6dB of peaking at 40GHz and reduces BER for a given signal power and data rate.

Table 1. State-of-the-Art Comparison

	Process	Modulation	Speed (Gb/s)	Energy efficiency(pJ/bit)	Chip area mm^2
[3]	0.25 μm SiGe-Photonic	QPSK*	128[1]	3.2	2.5×1.1
[6]	0.25 μm SiGe-Photonic	QPSK	112[1]	4.3	3.65×1.45
[7]	45-nm CMOS SOI EIC	QPSK	100[1]	0.98[2]	1.885×1.28 EIC
	90-nm Silicon Photonics PIC				65×1.1 PIC
[8]	22 nm FinFET CMOS[3]	PAM4	128[1]	0.098	0.23×0.11[4]
[9]	14 nm FinFET CMOS	OOK	32	1.4	0.046[4]
This work	45-nm CMOS SOI-Photonic	QPSK	80	1.2/0.9[2]	2.7×0.84

* C-band, [1] With post-processign equalization, [2] EIC only, [3] No integration with PIC, [4] EIC core area

References

1. T. Hirokawa et al., "Analog Coherent Detection for Energy Efficient Intra-Data Center Links at 200 Gbps Per Wavelength," in Journal of Lightwave Technology, vol. 39, no. 2, pp. 520-531, 15 Jan.15, 2021
2. A. Maharry et al., "First Demonstration of an O-Band Coherent Link for Intra-Data Center Applications," 2022 European Conference on Optical Communication (ECOC), 2022,
3. C. Kress et al., "64 GBd Monolithically Integrated Coherent QPSK Single Polarization Receiver in 0.25 μ m SiGe-Photonic Technology," 2018 Optical Fiber Communications Conference and Exposition (OFC), 2018, pp. 1-3.
4. https://rfic.ece.ucsb.edu/files/opticalrxsurveyv0xlsx
5. M. Rakowski, et al. "45nm CMOS - Silicon Photonics Monolithic Technology (45CLO) for next-generation, low power and high speed optical interconnects," in Optical Fiber Communication Conference (OFC) 2020, OSA Technical Digest (Optica Publishing Group, 2020), paper T3H.3.
6. P. M. Seiler et al., "56 GBaud O-Band Transmission using a Photonic BiCMOS Coherent Receiver," 2020 European Conference on Optical Communications (ECOC), 2020, pp. 1-4, doi: 10.1109/ECOC48923.2020.9333218.
7. H. Andrade, Y. Xia, A. Maharry, L. Valenzuela, J. F. Buckwalter and C. L. Schow, "50 GBaud QPSK 0.98 pJ/bit Receiver in 45 nm CMOS and 90 nm Silicon Photonics," 2021 European Conference on Optical Communication (ECOC), 2021, pp. 1-4.
8. S. Daneshgar, H. Li, T. Kim and G. Balamurugan, "A 128 Gb/s, 11.2 mW Single-Ended PAM4 Linear TIA With 2.7 Arms Input Noise in 22 nm FinFET CMOS," in IEEE Journal of Solid-State Circuits, vol. 57, no. 5, pp. 1397-1408, May 2022, doi: 10.1109/JSSC.2022.3147467
9. J. E. Proesel et al, "A 32 Gb/s, 4.7 pJ/bit Optical Link With 11.7 dBm Sensitivity in 14-nm FinFET CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 4, pp. 1214-1226, April 2018.