Developments of VCSEL-based transceivers for Co-Packaging

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Abstract: This paper covers recent industry developments in VCSEL-based transceivers that are designed for co-packaging on a first level package with ASICs, such as CPUs, GPUs, and data center switches. © 2023 The Author

1. Introduction

Packaging of optical transceivers with the primary data source IC on the same first level package (aka co-packaging) is a subject of current research and development. Recently there have been well attended major conference workshops on this subject [1][2]. The Optical Internetworking Forum (OIF) started a Co-Packaging Framework group which has so far completed a specification for a 3.2Tb/s co-packaged optical module based on silicon photonics and is currently working on specifications for the External Laser Source [3]. By over absorbing all the hype surrounding co-packaging, one may get the impression that co-packaging is a new optical packaging concept. But, in reality, it is not new. The first commercial system to use co-packaged optics was deployed in the field more than 10 years ago [4]. The optical transceivers used in this first system were 850nm VCSEL-based transceivers with 12 channels at 10Gb/s NRZ [5]. The commercial drawer compromised 224 transceivers co-packaged around 8 switch chips resulting in 22.4Tbps of throughput in 2010. Today, VCSEL-based co-packaging is still being developed and researched. This short-reach technology, up to 100m, has co-packaged applications such as xPU to xPU connections as well as switch to switch and switch to xPU within racks in data centers. VCSELs are an important workhorse in optical communications and continue to represent the lowest cost and lowest energy optical link solutions in the marketplace. This paper will report on recent industry efforts to bring VCSEL-based co-packaging to the market again.

2. Recent developments

Japan has recently funded the NICT B5G research project called BRIGHTEN [6] with the goal of creating co-packaged technology for 400G using 16 channels at 25G and consuming < 5W and an area of < 10mm^2 [6]. Two companies participating in this are Furukawa [7] and Fujitsu [8]. Furukawa has developed a single wavelength, 8 channel transceiver at 56Gbps PAM4 using 1060nm VCSELs. The VCSELs comprise a linear array of top emitters. The overall package footprint is 15.9 x 7.7mm^2 that includes a 0.3mm pitch LGA interface with a hexagonal arrangement of 231 pads. The channels in this transceiver have been operated to 56 Gbps PAM4 with a BER < 10^{-12} over 4.4m of MMF. Fujitsu has developed a 16 channel at 25Gb/s NRZ transceiver using sixteen 1060nm bottom emitting VCSELs arranged in a hexagonal pattern on a 40um pitch to directly match the cores of a 16 core multicore fiber. Their optical engine is 7 x 10mm^2 and fits inside a 7.8 x 16mm^2 package with a 231 pad, 0.3mm pitch, hexagonal LGA interface.

Hewlett Packard Enterprise (HPE) has been developing a multi-wavelength VCSEL-based co-packaged transceiver [9]. They arranged four linear VCSEL arrays of 6 devices, each under a special ferrule which also contained the optical mux and demux elements. By moving the optical mux and demux elements to the ferrule, they were able to create a reflow solderable technology and eliminate the LGA interface. The four wavelengths used are 990, 1015, 1040, and 1065nm. Reliability data for the 1065nm device showed 10Khrs at 170C, 8mA bias with no failures. An initial version of this technology was demonstrated at 600Gbps with the 24 VCSELs each operating at 25Gbps NRZ. A later version was extended to 1.2Tbps with each VCSEL operating at 56Gbps PAM4 and BER < 10^{-12} in a BTB link [10]. Using a special MMF with peak bandwidth centered on 1060nm, they were able to demonstrate 50Gbps PAM4 over 100m with BER < 10^{-12}. An impressive aspect of this work is the two system demos reported in [10]. The first was a bi-directional operation of the full link at 1.2Tbps over 10m with multiple connectors. The per channel data rate was 53.125Gbps and the average BER < $5x10^{-6}$ with over 10 modules tested. The second demonstration had 20 transceivers co-packaged around two 12.8 Tbps switches.

IBM and Coherent (formerly II-VI/Finisar) have collaborated for a number of years on a U.S. government project called MOTION (Multi-wavelength Optical Transceivers Integrated On Node) to create a VCSEL-based high speed co-packaged transceiver with an emphasis on very low energy per bit [11][12]. The project has two phases with phase 1 ending in 2020. In Phase 1, a single wavelength VCSEL-based 900 Gb/s transceiver was developed with 16 channels at 56 Gb/s/ch NRZ and 4 pJ/bit. The NRZ modulation format is preferred as this is still the dominant format used for xPUs, with the lowest latency due to no Forward Error Correction, and with the lowest energy per bit. Having used LGAs for co-packaging in the previous system [4], IBM is primarily focused on a

reflow solderable package, although an LGA option exists for other users. Directly soldering a co-packaged transceiver avoids all of the issues associated with LGAs, such as reduced signal integrity, higher cost, mechanical loading of the both the transceiver and laminate, compromised thermal path, and extra space taken up by the LGA loading mechanism. At the same time, a solderable part is no longer replaceable after underfill and thus requires the technology to have a higher level of reliability. (One can make the argument that LGA socketed modules are not field replaceable either). Since lasers tend to be the least reliable component within an optical transceiver, the MOTION approach has been to provide an additional spare VCSEL per channel. Reliability calculations have shown this 2:1 sparing approach to increase the reliability by almost 3 orders of magnitude [13]. The sparing does not require additional fibers as both the spare and primary VCSELs can be coupled into the same fiber using polarization multiplexing [13]. Another important aspect of this sparing scheme is that it has been shown to take ~100ns to deploy the spare, which is about 9 orders of magnitude faster than replacing a pluggable optic [14]. In phase 2 of MOTION, the data rate and channel count will double and the energy per bit will be halved [12]. Table 1 below compares the major specification differences be MOTION phases 1 and 2.

Table 1: Comparison of Specifications between MOTION Phases 1 and 2

Parameter	MOTION Phase 1	MOTION Phase 2
Electrical Interface	16 channels @ 56G NRZ	32 channels @ 112G PAM4
IC Technology	SiGe	CMOS
Optical Interface	16 channels @ 56 G NRZ	32 channels @ 112G PAM4
# of Wavelengths	1: 850nm	2: 850nm, 910nm
# of Fibers	16 Tx + 16 Rx	16 Tx + 16 Rx
Fiber Type	50/125 MMF	50/125 MMF
Supported Distance	30m	30m
Package I/O Pitch	400um	300um
Glass Carrier Size	13x13mm	13x13mm
Energy consumption	4 pJ/bit	2 pJ/bit
Laminate interface	Soldered or LGA	Soldered or LGA

Another aspect of the MOTION Phase 2 is a feasibility study performed by IBM's Server Packaging group [15]. Figure 1 shows images of the laminates used in this feasibility study. The left side show four MOTION modules soldered to the laminate prior to lid attach and the right side shows a 5-module version after lid attach and fiber ribbon insertion. Twenty laminates (80 MOTION modules) were subjected to 5 cycles of -40°C/ +60°C thermal shock before being divided into 4 groups of 5 to receive either Deep Thermal Cycling (DTC, -40°C/ +125°C, 1500 cycles), Accelerated Thermal Cycling (ATC, 0°C/ +100°C, 3000 cycles), High Temperature Storage (HTS, +125°C, 2000 hrs) or 85°C/85 %RH temperature and humidity (T&H, 1000 hrs) tests. These 20 modules did not show significant degradation in terms of thermal performance. Another group of 17 laminates have been subjected to 1500 cycles of DTC only. This group saw some laminate failures late in the DTC cycles (>1000 cycles), which does not pose a reliability risk for the field application.

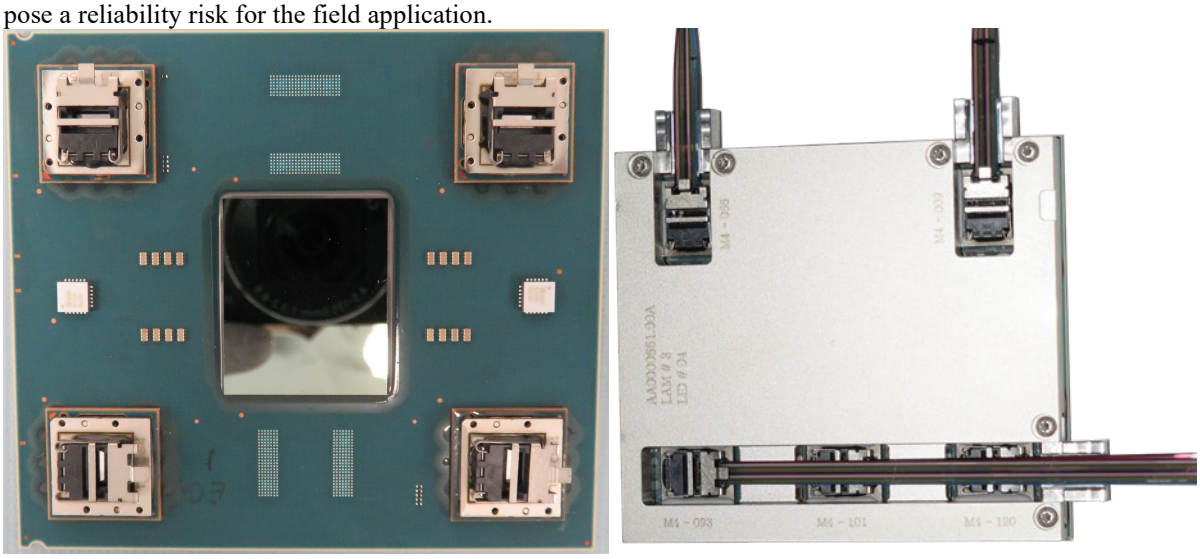

Figure 1 (left) Four MOTION1 transceivers on a processor laminate, (right) Laminate after lid and fiber insertion.

3. Closing Remarks

One of the touted advantages for co-packaging is a reduction in power consumption. VCSEL based solutions have the best chances of realizing this. The goal of the Japanese projects at 8pJ/bit and the MOTION project at < 4pJ/bit will demonstrate this. The vast major of links used in High Performance Computing systems and hyper scale data centers are less than 100m long. This is the distance for which the use of VCSELs is optimal and where they are deployed in very high volumes. Leveraging these volumes along with prior commercialization of parallel links using VCSELs puts the current industry focused VCSEL-based co-packaging developments in a good position for success.

4. Acknowledgements

The information, data, or work presented herein related to IBM's project MOTION, was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000846. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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