# 30-Gbps/ch x 4 ch Simultaneous Error-Free Transmission with A Low-Power Transmitter Flip-Chip-Bonded 1.3-µm LD-Array-on-Si

Toshiki Kishi<sup>1</sup>, Munehiko Nagatani<sup>1</sup>, Shigeru Kanazawa<sup>2</sup>, Kota Shikama<sup>1</sup>, Takuro Fujii<sup>1</sup>, Hidetaka Nishi<sup>1</sup>, Tadashi Minotani<sup>1</sup>, Norio Sato<sup>1</sup>, Toru Segawa<sup>1</sup>, and Shinji Matsuo<sup>1</sup>

<sup>1</sup>NTT Device Technology Labs., NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-0198, Japan <sup>2</sup>NTT Device Innovation Center, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-0198, Japan Author e-mail address: toshiki.kishi.ay@hco.ntt.co.jp

**Abstract:** 30-Gbps/ch NRZ PRBS-31 x 4 ch simultaneous error-free 1.6-km transmission was achieved with a low-power 4-ch transmitter consisting of 65-nm CMOS cascode shunt LD drivers and flip-chip-bonded LD-array-on-Si, resulting in power efficiency of 1.2 mW/Gbps. © 2023 The Author(s)

# 1. Introduction

With the expansion of social networking services, further rapid increases of transmission capacity in data centers are expected. To process large amounts of traffic, high-speed data communication in data center rack units is needed. For this purpose, low-power optical transceivers have been implemented on boards in data center racks, and multichannel co-packaged optical devices [1] and photonic chiplets [2] have been reported. To increase the bandwidth density of these multi-channel devices, supply voltage terminals common to all channels are needed, since the larger the channels of devices are, the larger the supply voltage terminals are. However, since the terminals common to all channels receive crosstalk noise from adjacent channels, the impedance of the terminals should be extremely low. In particular, decreasing the impedance for the low-frequency range is important because pseudo-random bit sequence (PRBS)-31 signals, which are used for 100GbE [3], have a lower frequency range than low-order PRBS signals, such as PRBS-7, 11, 15, and 23 [4]. To decrease the impedance for the low-frequency range, decoupling capacitors with huge capacitance values are needed between the supply voltage terminals and ground in the transceivers. However, these capacitors take up huge spaces, which makes it difficult to implement them in the transceiver IC. We have reported a 4-ch transmitter that achieved 25-Gbps/ch NRZ PRBS-7 x 4 ch simultaneous error-free transmission by increasing the capacitance value of the decoupling capacitors as much as possible to decrease the impedance of the supply voltage terminals [5]. The transmitter was able to transmit only up to NRZ PRBS-7 because the increase in the capacitance value was not enough to transmit NRZ PRBS-31 signals in 4-ch simultaneous error-free operation.

In this work, to decrease the impedance further, we have devised a new low-power 4-ch 65-nm CMOS cascode shunt LD driver, which has an improved connection of the decoupling capacitors to the supply voltage terminals. Compared with our previous one [5], crosstalk noise from adjacent channels is suppressed. In addition, the driver has an inductor peaking part to improve eye openings of optical output waveforms. With the improvements, a low-power 4-ch transmitter consisting of the new driver and flip-chip-bonded  $1.3-\mu m$  LD-array-on-Si achieves 30-Gbps/ch NRZ PRBS-31 x 4 ch simultaneous error-free 1.6-km transmission, resulting in power efficiency of 1.2 mW/Gbps.

#### 2. Structure of low-power 4-ch transmitter and simulation results

Fig. 1(a) and (b) show block diagrams of the 4-ch transmitter with our previous driver [5] and new driver, respectively. The dotted line outlines the 4-ch driver IC. In the new one, we incorporated two improved parts without increasing power consumption. One part is for suppressing crosstalk noise from adjacent channels inside the dashed lines. The other is the inductor peaking part inside the dashed-dotted lines. Inside the dashed lines, supply voltage terminals for the gate terminal of the PMOS transistor  $M_3$  and NMOS transistor  $M_2$  ( $V_2$  and  $V_3$ , respectively) of the previous driver have decoupling resistors and capacitors outside each channel. However,  $V_2$  and  $V_3$  of the new driver have decoupling resistors and capacitors outside each channel. However,  $V_2$  and  $V_3$  of the new driver can be set close to the gate terminal of  $M_3$  and  $M_2$ , respectively, crosstalk noise into the gate terminal can be prevented. In addition, all decoupling capacitors of  $V_2$ ,  $V_3$ , and  $V_4$  in the previous driver are connected to the ground. However, as shown in the new driver, since the impedances of  $V_2$ ,  $V_3$ , and  $V_4$  are connected in parallel with  $V_1$  by connecting all decoupling capacitors of  $V_2$ ,  $V_3$ , and  $V_4$  to  $V_1$ , the impedance of  $V_1$  can be decreased. The inductor peaking part can improve the electro-optic (EO) responses of the 4-ch transmitter. In





Fig. 3. Simulated 30-Gbps/ch NRZ PRBS-31 optical output waveform for 4-ch transmitter with (a) previous driver and (b) new driver under simultaneous operation.



Fig. 2. Simulated EO responses of 4-ch transmitter with previous driver and new driver. Dotted lines and dashed lines show EO responses of the 4-ch transmitter with previous driver and new driver, respectively.



Fig. 4. Microphotographs of 4-ch transmitter (left) and the 4-ch LD-array-on-Si and new 4-ch driver IC (right).

addition, the RC filter on  $M_3$  can suppress excessive overshoot and undershoot of optical waveforms due to the inductor peaking part.

The dotted and dashed lines in Fig. 2 show the simulated EO responses of the 4-ch transmitter with the previous driver and new driver, respectively. The EO responses were simulated with our photonic-electronic conversion system in SPICE [6]. As shown in Fig. 2, compared with the previous driver, the new one with suppressed crosstalk noise suppresses the resonance peak in the low-frequency range, which is caused by the parasitic inductance and resistances of the supply voltage terminals  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$ . In addition, the new driver improved the 3-dB bandwidth more than 2 GHz with the inductor peaking part. Fig. 3(a) and (b) show simulated 30-Gbps/ch NRZ PRBS-31 optical output waveforms for the 4-ch transmitter with the previous driver and new one under simultaneous operation, respectively. The functions of both suppressing crosstalk noise and inductor peaking improved the  $\Delta x$  and  $\Delta y$  values of the diamond eye mask pattern outlined by the dashed line.

Fig. 4 shows microphotographs of the 4-ch transmitter, 4-ch membrane LD-array-on-Si, integrated with a spotsize convertor (SSC) [7], and new 4-ch driver IC. The driver IC chip was fabricated in 65-nm CMOS technology. In the driver IC, dummy pads, which the dotted line outlines, are used to prevent the 4-ch LD-array-on-Si from leaning when the LD array is flip-chip bonded to the driver IC. The face-down LD array is stably connected to the driver IC by flip-chip bonding through Au bumps bonded to V<sub>outa</sub>, V<sub>outc</sub>, and the dummy pads. V<sub>outa</sub> and V<sub>outc</sub> of the driver are connected to the p and n terminals of the LD array, respectively. The dummy pads in the upper side of the driver IC are connected to the blank space between each SSC of the LD array. The flip-chip bonding interconnection technique minimizes the parasitic inductance between the LD array and driver IC. Therefore, the degradation of the group delay characteristics due to bonding interconnections is suppressed.

### 3. Measurement results

We measured 30-Gbps/ch NRZ optical waveforms for discrete and simultaneous operation of all four channels at 25°C. Lasing wavelengths were 1292–1300 nm. The 30-Gbps/ch NRZ PRBS-31 signals from the pulse pattern generator were input into  $V_{in}$  of the 4-ch driver with RF probes. The input signal amplitude was 0.45  $V_{pp}$ . The LD bias current of all four channels was set to 10.1 mA. The measurement was carried out via a single-mode high-numerical-aperture fiber that was butt-coupled with the SSC on the LD chip and spliced to standard single-mode fiber (SSMF) at the opposite side. As shown in Fig. 5, measured optical waveforms of all channels operating simultaneously have an extinction ratio (ER) of over 3 dB with clear eye-openings. The difference between each channel in the average optical power ( $P_{avg}$ ) is mainly caused by fiber coupling issues.

Next, we measured the bit error rate (BER) performance for discrete and simultaneous operation with 30-Gbps/ch NRZ PRBS-31 signal after 1.6-km transmission using SSMF. To measure the BER, we used a receiver (DSC-R409, Discovery Semiconductors, Inc.), consisting of a photodiode and transimpedance amplifier, and an



Table 1. Comparison of state-of-the-art low-power 4-ch transmitters for DFB-LD and VCSEL, showing the measured BER dependence of NRZ signals over 25 Gbps/ch with 4-ch simultaneous operation

|  | [8]                           | [9]                            |       | [10]                          | [11]                           | [5]                           | This work                      |
|--|-------------------------------|--------------------------------|-------|-------------------------------|--------------------------------|-------------------------------|--------------------------------|
| IC technology  | 130-nm SiGe BiCMOS            | 130-nm SiGe BiCMOS             |       | 65-nm CMOS                    | 65-nm CMOS                     | 65-nm CMOS                    | 65-nm CMOS                     |
| LD technology  | 850-nm VCSEL                  | 850-nm VCSEL                   |       | 850-nm VCSEL                  | 1.3-µm DFB-LD                  | 1.3-µm DFB-LD                 | 1.3-µm DFB-LD                  |
| Chip mounting technology                             | Flip-chip bonding             | Flip-chip bonding              |       | Flip-chip bonding             | -                              | Flip-chip bonding             | Flip-chip bonding              |
| Single data rate [Gbps]                              | 40                            | 25.8                           | 34    | 25                            | 25                             | 25                            | 30                             |
| Total data rate [Gbps]                               | 160                           | 103.2                          | 136   | 100                           | 100                            | 100                           | 120                            |
| Power consumption including<br>Driver and LD [mW/ch] | 327.5                         | 525                            | 650   | 257.5                         | 207.8                          | 66.8                          | 35.9                           |
| FOM [mW/Gbps/ch]                                     | 8.19                          | 20.35                          | 19.12 | 10.3                          | 8.31                           | 2.67                          | 1.2                            |
| Bit error rate                                       | <10 <sup>-12</sup><br>(PRBS7) | <10 <sup>-12</sup><br>(PRBS31) |       | <10 <sup>-12</sup><br>(PRBS9) | <10 <sup>-13</sup><br>(PRBS31) | <10 <sup>-12</sup><br>(PRBS7) | <10 <sup>-12</sup><br>(PRBS31) |
| Transmission length                                  | 8 m                           | -                              | -     | -                             | 100 m                          | 1.2 km                        | 1.6 km                         |

error analyzer. As shown in Fig. 6, for all channels, error-free transmission (BER  $< 10^{-12}$ ) for discrete and simultaneous operation over 1.6-km-long SSMF was achieved without an optical amplifier. In addition, the crosstalk penalties between discrete and simultaneous operation are below 2.2 dB in all channels. These results show that the electrical crosstalk was suppressed by the improved 4-ch driver. The total power consumption of the 4-ch transmitter, including the 4-ch driver and LD array, is only 144 mW at 30 Gbps/ch.

Table 1 compares our 4-ch transmitter with state-of-the-art low-power 4-ch transmitters designed for DFB-LD and VCSEL, showing the measured BER dependence of NRZ signals over 25 Gbps/ch with 4-ch simultaneous operation. The figure of merit (FOM) is defined as power consumption per channel, including the 4-ch driver and LD array, divided by the single data rate. The FOM of our 4-ch transmitter, 1.2 mW/Gbps, is the lowest in Table 1.

## 4. Conclusion

We have devised a low-power 4-ch transmitter consisting of a 4-ch 65-nm CMOS cascode shunt LD driver and flipchip-bonded 1.3-µm directly modulated LD-array-on-Si. The transmitter can operate simultaneously with 30-Gbps/ch NRZ PRBS-31 x 4 ch, resulting in power efficiency of 1.2 mW/Gbps. Clear 4-ch eye openings of 30-Gbps/ch NRZ optical output waveforms were achieved in simultaneous 4-ch operation. In addition, transmission of 30-Gbps/ch NRZ PRBS-31 x 4 ch operating simultaneously over 1.6-km-long SSMF was demonstrated with errorfree operation. To the best of our knowledge, our 4-ch transmitter achieves the best power efficiency among reported 4-ch transmitters with over 25-Gbps/ch NRZ signals. This transmitter could feasibly be further developed as a low-power high-speed multi-channel device with more than four channels such as 16 or more.

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