A Direct Bond Interconnect 3D Co-Integrated Silicon-Photonic Transceiver in 12nm FinFET with -20.3dBm OMA Sensitivity and 691fJ/bit

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Abstract: We present the first experimental demonstration of an electronic-photonic co-designed transceiver circuit heterogeneously 3D co-integrated with high-density, low-parasitic Direct Bond Interconnect (DBI®) featuring full SerDes that achieves -20.3dBm OMA sensitivity and 691fJ/bit link energy efficiency.

1. Introduction

Increasing demand for energy-efficient data transmission in future high-performance computing (HPC) systems and data centers results in power, bandwidth, and scalability bottlenecks [1]. Silicon photonic (SiPh) transceivers have the potential to address this, provided that the photonic integrated circuits (PICs) and electronic integrated circuits (EICs) are optimally co-designed and co-integrated with minimal parasitics [2]. In particular, minimizing parasitic capacitances at the receiver input can dramatically improve receiver sensitivity and at the transmitter output can improve bandwidth and energy efficiency [3]. While monolithic integration of electronic-photonic circuits [4] can minimize parasitic overheads, this compromises the flexibility and performance of both the EIC and PIC. Heterogeneous integration allows for independent EIC and PIC optimization with low parasitics.

While recent work has shown 3D integrated EIC-PIC assemblies [5], this was without integrated operational electronic circuitry and required an external high-speed data I/O interface to the photonic circuits. The presented work utilizes direct bond interconnect (DBI®), which is a state-of-the-art 3D integration solution [6] that offers bond pitch as small as 2 µm, and is the first demonstration of a 3D DBI® integrated, co-designed silicon photonic transceiver with a 12 nm FinFET EIC. This EIC features full 8:1 SerDes transceivers with drivers optimized to drive microring modulators and transimpedance amplifier (TIA) front-ends optimized to interface with low-capacitance waveguide photodetectors.

2. EIC-PIC Integrated System Architecture

Fig. 1 illustrates the integrated transceiver (TRX) platform consisting of the CMOS EIC die flip-chip bonded to the SiPh PIC with DBI®. The 1.5 mm ×1.5 mm TRX EIC is fabricated in GlobalFoundries 12 nm FinFET process and features 32 Tx and Rx pairs. These TRX pairs include 8:1 serializing transmitters with high-speed micro-ring modulator (MRM) drivers, 1:8 deserializing receivers with TIA front-ends and low-complexity timing recovery, and ring thermal tuning control circuitry. The optical transceiver circuits were carefully co-designed to fit within 20 μm vertically to match the DBI® bonding pad pitch for integration with the PIC. The EIC also includes 50Ω impedance-matched 4.125 Gb/s electrical transceivers to communicate with any external IC such as FPGA/ASIC/GPU/CPU.

The 5.5 mm × 7.5 mm SiPh PIC was implemented on a custom 300 mm wafer-scale AIM Photonics silicon photonics run with a number of custom-designed O-band microdisk modulators with integrated heaters, add-drop filters, and germanium photodetectors. The active photonic devices take up only ∼2 % of the PIC die area, with the rest utilized as a first-level optical interposer for the EIC, transitioning the signal and power nets to wirebond pads at the PIC periphery. The EIC die area is 5.45% of the PIC die and takes advantage of the more advanced CMOS process node. The EIC and PIC are integrated using DBI® at Nhanced Semiconductors. Simulation of the DBI pad array showed 5.5 fF capacitance [3], which represents substantially reduced parasitics relative to previously reported to Cu-pillar bonding capacitance of 80 fF [7]. The bonding pitch is 20 μm pad-to-pad for 6.6 μm bondpads. The signals are wirebonded to a secondary organic laminate interposer and assembled onto the test PCB on pogo pins. Polarization maintaining single-mode fibers are edge-coupled using v-grooves.

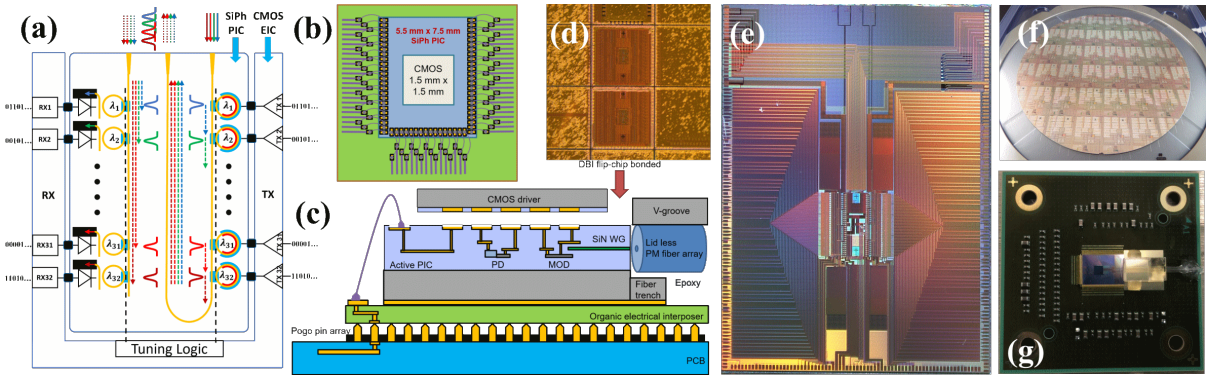

Fig. 1. (a), (b) and (c) illustrate the EIC-PIC architecture and integration scheme, (d) GF12LP wafer showing two CMOS die, (e) fabricated PIC, (f) DBI® bonded EIC dies on SiPh wafer, (g) EIC-PIC assembled onto a laminate interposer with wirebonding and co-packaged optics.

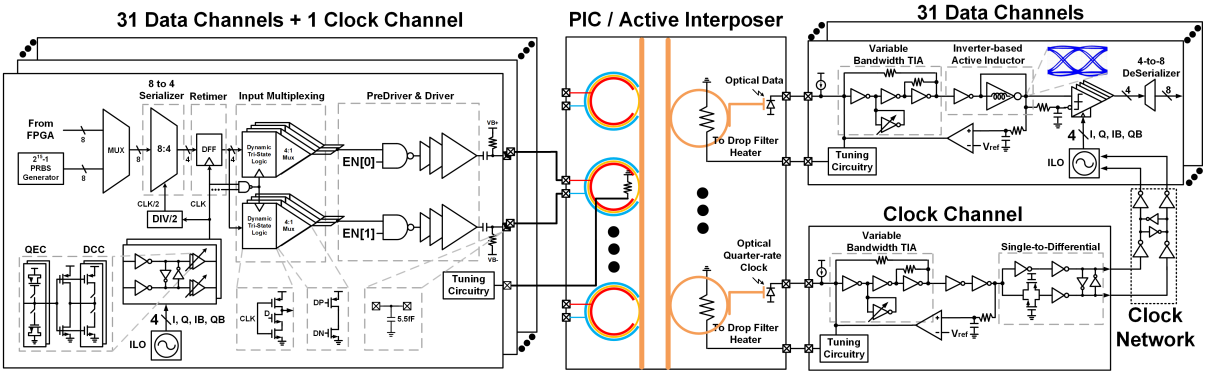

Fig. 2. 12nm optical transceiver circuitry with PIC/active interposer.

3. Transceiver Architecture

The optical transmitter architecture is shown on the left side of Fig. 2. Efficient global clock distribution is performed with a differential quarter-rate clock distributed to 4 injection-locked oscillators (ILOs) that each clock a group of 8 transmitters in a bundled manner. These ILOs generate 4-phase quarter-rate clocks that drive the final 4:1 serializer and, after passing through a divide-by-2 block, the initial 8:4 serializer. Per-channel buffers implement both clock phase quadrature error correction (QEC) and duty cycle correction (DCC). An on-chip PRBS-15 generator provides the 8-bit parallel input data to the initial 8:4 serializer. The data is then serialized to full rate in the final 4:1 mux with minimal transistor high-impedance slices driven by dynamic pulse gates. An inverter-based output driver with AC-coupling on-chip bias-tee is used. Powered by a 0.9 V supply, the driver outputs a 1.8 V_{ppd} electrical swing to the micro-ring modulator after AC coupling. A forwarded-clock transmitter, which is a replica of the data transmission channel with the 8-bit input programmed as quarter-rate clock pattern, forwards a clock signal to the receiver channels for low-complexity timing recovery.

The optical receiver architecture is shown on the right side of Fig. 2. A multi-stage high-transimpedance TIA front-end with tunable bandwidth is implemented to provide improved and consistent OMA sensitivity under variations of input capacitance and feedback resistance due to fabrication and packaging tolerances. Bandwidth tuning is achieved by a bank of programmable direct-feedback inverters that act as active inductance for bandwidth extension. An additional active inductor voltage amplifier stage then drives 4 parallel samplers that perform the initial 1:4 deserialization. These samplers are clocked with 4 ILO-generated quarter-rate clock phases, where tunability of the ILO center frequency is implemented to allow for a programmable phase shift and low-complexity timing recovery. This is then followed by the final 8:4 deserializing stage. The forward-clock receiver channel has a similar front-end design, but with no active inductance frequency peaking since the clock is a single-tone.

4. Experimental Results

Fig. 3(a and b) show the measured drop performance and high thermal tuning efficiency of 0.27 nm/mW of the custom add-drop filters. Fig. 3(c and d) shows the 10 Gb/s and 18 Gb/s eye diagrams from the transmitter testing

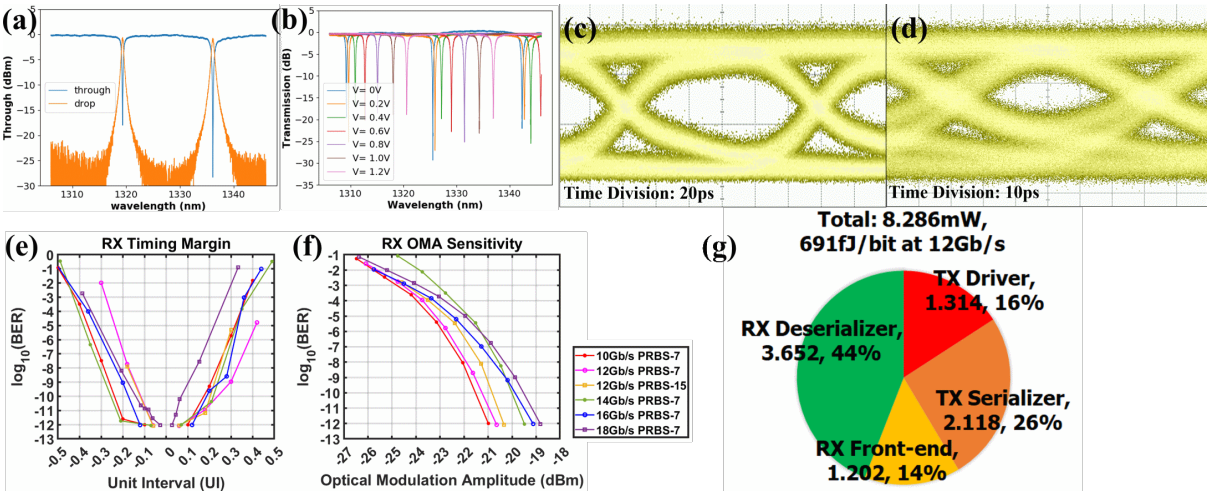

Fig. 3. (a) Through-Drop transmission spectra and (b) tuning efficiency of the PIC custom Add-Drop filters, (c)(d) transmitter eye diagrams at 10 Gb/s and 18 Gb/s, (e)(f) receiver timing margin and OMA sensitivity, (g) transceiver link energy efficiency.

with the EIC driving the PIC to modulate an external continuous wave (CW) 1310 nm laser input using PRBS-15 data from the on-chip PRBS generator. For receiver testing, the externally MZM modulated laser with PRBS data emulates optical data. An attenuator emulates any channel attenuation. An optical delay line (ODL) controls the sampling phase between the input optical signal and the receiver sampler circuit. The PIC add-drop filter is externally tuned to drop the modulated signal into a reverse-biased germanium photodetector (PD) and the output is sent to the TIA front-end on one of the RX channels. As Fig. 3(e and f) shows, the timing margin for error-free data sampling at 12 Gb/s optical input with 6.9dB extinction ratio (ER) and PD responsivity of 0.8 A/W was 0.12 UI and the optical modulation amplitude (OMA) sensitivity was -20.3 dBm. Crrently the RX is tested to operate up to 18 Gb/s with ∼2 dB OMA penalty. Fig. 3(g) power breakdown indicates the energy efficiency of a transceiver pair at 12 Gb/s is 691 fJ/bit.

5. Conclusion

We have demonstrated a co-designed electronic-photonic integrated transceiver with advanced 3D DBI® integration and co-packaged optics. The reduced parasitics of the DBI® packaging enabled OMA sensitivity of -20.3 dBm and energy efficiency of 691 fJ/bit at 12 Gb/s.

6. Acknowledgement

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