First 100 Gb/s monolithically integrated electronic-photonic coherent receiver with direct edge coupling to standard single mode fiber array

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Abstract: We report fabrication, assembly and testing of the first >100 Gb/s monolithic electronic-photonic coherent receiver chip and sub-assembly, edge coupled to standard single mode fiber array.

1. Introduction

Silicon photonics (SiPh) is becoming a mainstream technology platform for the realization of miniaturized coherent receiver (Coh-Rx) circuits deployed in network environments beyond long-haul, such as terrestrial intra-datacenter interconnects [1] as well as satellite laser communication links [2]. State-of-the-art Coh-Rx circuits demonstrated in various SiPh technologies, feature monolithic integration of passive waveguide components with Ge photodetectors (PDs) [3-5] and their assembly with electronics relies either on manual wire bonding [3] or flip-chip assembly [4, 5]. In the latter, coherent receivers were demonstrated to fit into small form factor BGA assemblies, validating module-level compactness, however the assembly complexity is driven by the use of multi-layer PCB substrates and the multiple bonding steps required for opto-electronic integration and interconnection. The integration of photonics with electronics in the same process and eventually on the same front-end would drastically mitigate complexities and further improve the assembly quality, performance and cost. Such monolithic co-integration of Coh-Rx circuits has been demonstrated at 100 Gb/s data rates [6,7], however these demonstrations were limited to probe testing, whereas fiber-to-chip coupling was realized vertically using conventional 1D grating couplers (GCs). The use of these structures would add to the assembly complexity since 1D GCs require non-standard coupling angles, angle polished fiber arrays and they exhibit polarization and wavelength dependence.

In this paper we demonstrate the first Coh-Rx electronic-photonic integrated circuit (ePIC) and sub-assembly which features optical edge coupling through on-chip integrated spot-size converters (SSC). The chip hosts >20 photonic and opto-electronic elements co-integrated with electronics into a silicon area of ~6 mm^2. The Coh-Rx was pigtailed and integrated in a receiver optical sub-assembly which was used to experimentally demonstrate coupling to a standard ribbon fiber array with <4 dB losses and coherent QPSK detection up to 108 Gb/s data rate on a single wavelength/polarization. The chip power consumption is 520 mW which corresponds to an energy efficiency of 5.2 pJ/bit. The Coh-Rx circuit was designed and manufactured in the IHP 0.25 um photonic-BiCMOS process.

2. Coherent receiver chip and sub-assembly

Fig. 1(a) shows the fabricated coherent receiver chip. Optical I/O is realized through edge coupling via inverse taper SSCs. There are four SSCs integrated on-chip; the two outer SSCs are connected back-to-back via an integrated waveguide loop that surrounds the receiver core. During packaging, these SSCs can be used to assist fiber alignment by monitoring the optical power that is launched through the integrated optical path. The other two SSCs are used for launching the input and local oscillator (LO) optical signals into the ePIC. The input and LO signals are mixed in a single 4x4 MMI coupler configured as an optical hybrid (OH). Photodetection is implemented in two pairs of Ge PDs which are coupled to a pair of 3-stage transimpedance (TIA) BiCMOS circuits described in [7]. The integrated optics design accommodates the connection of the MMI-OH outputs to the Ge PDs with equal and non-intersecting integrated waveguides [8], avoiding waveguide crossings and phase mismatching. Fig. 1(b) shows the Coh-Rx ePIC mounted and wire-bonded to a ceramic sub-mount with its DC pads positioned to the north/south side and the RF pads positioned to the east side of the chip. On the optical input end, a standard SMF array assembly (shown in the inset) is glued to the chip following active alignment. Fig. 1 (d) shows the finished Coh-Rx sub-assembly. Access to the differential RF outputs is provided through screw-on-PCB K-connectors. During test, one signal component per differential pair is used with the second signal pair terminated to 50 Ohm resistors.

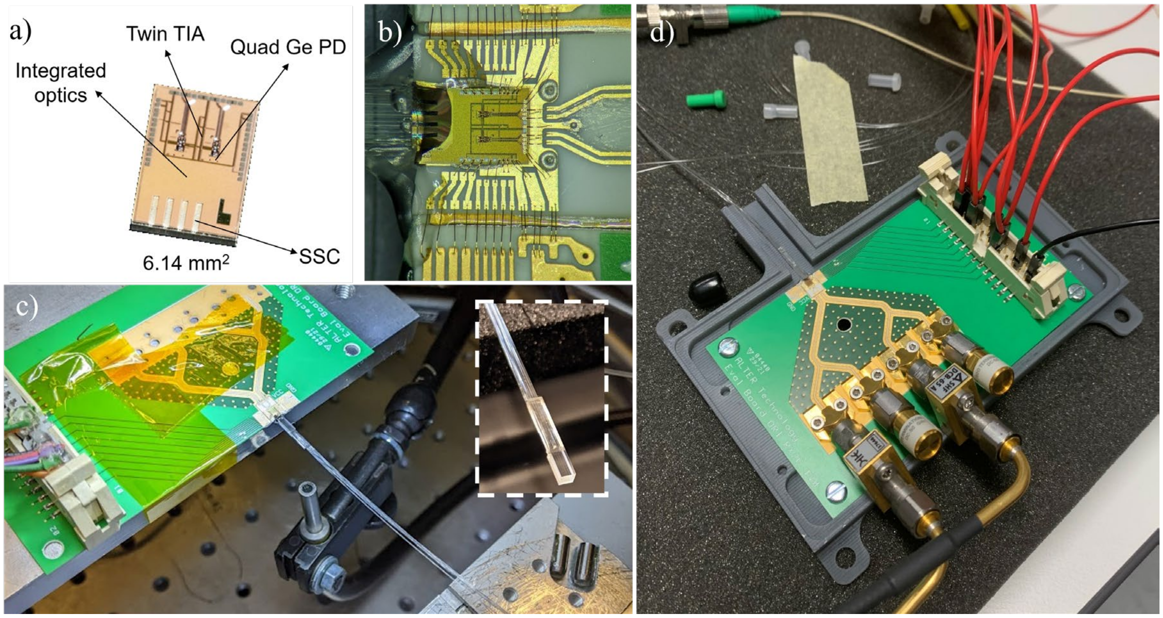

Fig. 1: (a) Fabricated Coh-Rx ePIC, (b) Coh-Rx ePIC assembled with ceramic tile and fiber array, c) alignment process and fiber array shown in the inset, d) complete Coh-Rx sub-assembly.

Fig. 1(c) shows the assembly set-up. The assembly was performed with active alignment by measuring the Ge PD photo-current. The fiber-to-chip coupling loss post-fiber fixing was estimated taking into account the typical responsivity of the Ge PD, the insertion losses of the MMI-OH and the insertion loss of the fiber array component. Using this method, the typical fiber-to-chip coupling was estimated at 4 dB.

3. Results

Fig. 2 shows the intradyne set-up used to evaluate the Coh-Rx sub-assembly performance. The set-up is similar to the one described in [7] and comprises a commercial-off-the-shelf multi-format transmitter, an arbitrary waveform generator, 2x external cavity lasers and test and measurement equipment. The modulated optical signal was launched to the Coh-Rx sub-assembly through a Variable Optical Attenuator (VOA), which has a built-in power meter (PM) to monitor the optical power. The receiver outputs were connected to two real-time oscilloscopes through DC blocking capacitors (see Fig. 1d)). For offline digital signal processing (DSP) and Bit-error-ratio (BER) measurement, a commercial analyzer tool was used. The DSP operations include clock recovery, phase estimation, RRC filtering and least-mean-square equalization based on the symbol decision and the constant modulus algorithm.

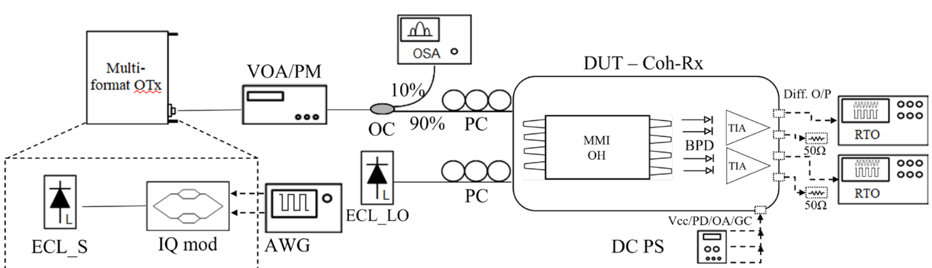

Fig. 2. Intradyne transmission test-bed for the Coh-Rx evaluation testing.

The Coh-Rx performance was evaluated by measuring the BER as a function of the received optical power (ROP) and recording the eye and constellation diagrams. The evaluation was performed for a 1550 nm, QPSK modulated optical signal at a symbol rate range of 32 up to 54 GBd (64 to 108 Gb/s data rate). The LO optical power injected in the Coh-Rx was 7.8 dBm. The OSNR of the QPSK signal was measured at >30dB. Fig. 3 shows the captured eye diagrams for both the I and Q signal components as a function of the data rate and at a received power of -9 dBm.

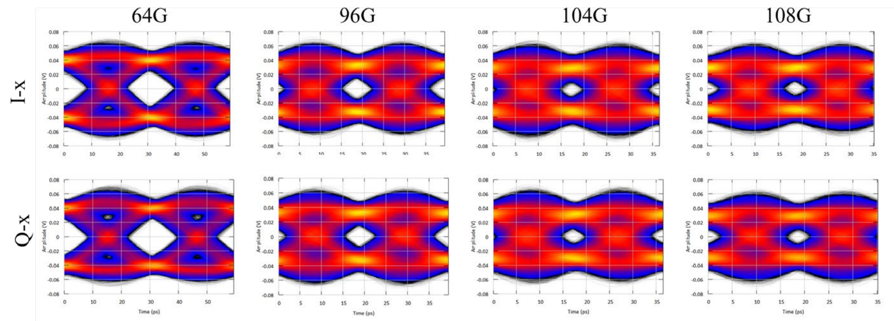

Fig. 3. Recovered eye diagrams for: (top) I-x signal and (bottom) Q-x signal at 64, 96, 104 and 108 Gb/s.

Fig. 4 shows the BER as a function of received optical power (ROP) as well as the constellation diagrams captured for -9 dBm received power at 64 to 108 Gb/s data rates. BER measurements show successful coherent detection up to 108 Gb/s below a pre-FEC limit of 10-3, which is shown in the dashed line. The receiver sensitivity (BER 10-3) at 108 Gb/s data rate was measured at -19 dBm.

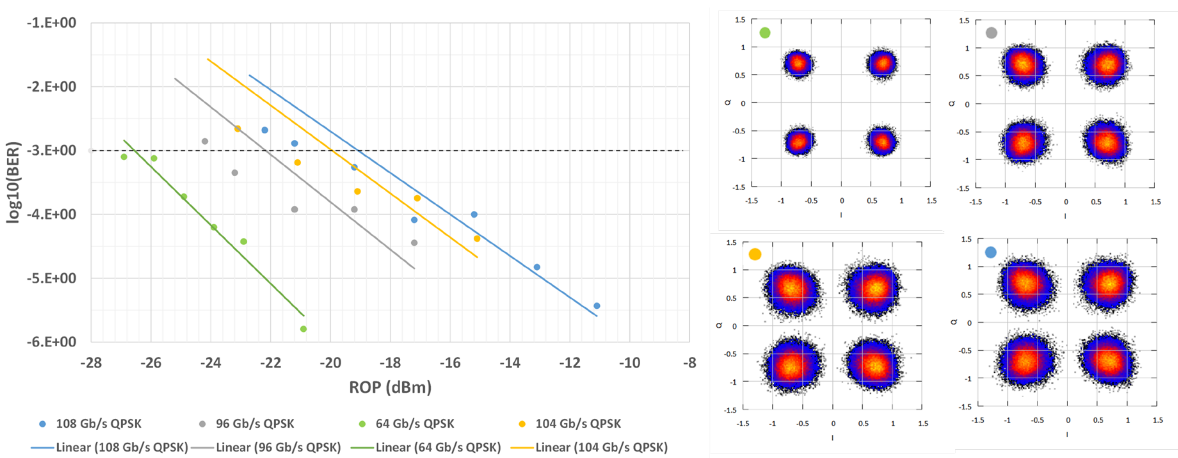

Fig. 4. (left) BER as a function of ROP and (right) constellation diagrams.

3. Conclusion

We presented the first monolithically integrated electronic-photonic coherent receiver chip and sub-assembly directly coupled to a standard SMF array. We demonstrated successful coherent detection of QPSK modulated signals at data rates up to 108 Gb/s.

Acknowledgement

This work was conducted within the framework of H2020-SPACE-ORIONAS and funding was received from the Horizon 2020 Research and Innovation Programme of the European Union under Grant Agreement No. 822002.

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