Monolithically Integrated Autonomous Demultiplexers with Near Zero Power Consumption for Beyond Tb/s Links

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Abstract: Integrated multiplexer/de-multiplexer systems based on capacitively tuned MZI and adiabatic ring resonators with sequential tuning and wavelength locking are presented.

1. Introduction

Wavelength division multiplexing (WDM) is a key enabler to achieve beyond Tb/s data-rates for next generation optical links. In the transmitter of such links, the output of a multi-carrier optical source (*e.g.* a frequency comb) is de-multiplexed into individual carriers using a DeMux block, individually modulated, and multiplexed back to a single output using a multiplexer (Mux). To achieve ultra-low energy and error-free operation for data-rates beyond 1 Tb/s, Mux and DeMux must provide a high level of channel-to-channel isolation and be immune to environment fluctuations and fabrication process variations while consuming a small amount of power and introduce negligible loss. Photonic Mux and DeMux systems using thermally tuned MZIs or ring resonators have been demonstrated [1][2]. However, thermal tuning, while achieving a large tuning range, does not offer the desired energy efficiency for tuning and control of Mux and DeMux components within a system with a large number of channels. Thermal cross-talk is another disadvantage of thermal tuning in such systems. Monolithic integration of photonic devices with CMOS electronics significantly reduces the packaging complexity and offers reduced parasitics due to the vicinity of photonic and electronic devices. In this paper, benefiting from semiconductor-insulator-semiconductor capacitor (SISCAP) [3] optical phase shifters, realized using the transistor gate structure of the photonic enabled GlobalFoundries GF9WG CMOS process, we report the demonstration of two fully integrated autonomous 8-channel Mux/DeMux systems; one based on capacitively tuned MZIs and another one based on capacitively tuned adiabatic ring resonators. Use of capacitive phase shifters and highly scalable on-chip sequential tuning and locking of Mux/DeMux systems results in near zero static power consumption. Demonstrated Mux/DeMux systems if used in an 8-channel 256Gb/s link can achieve an energy efficiency of under 10fJ/bit.

2. Principle of Operation

The first key concept in the design of the reported Mux and DeMux systems is the use of capacitive tuning to align the system to the input carriers (*e.g.* comb lines). Monolithic integration of the system on GloalFoundries 90nm CMOS process enables use of the thin gate oxide layer for implementation of SISCAP optical phase shifters. The

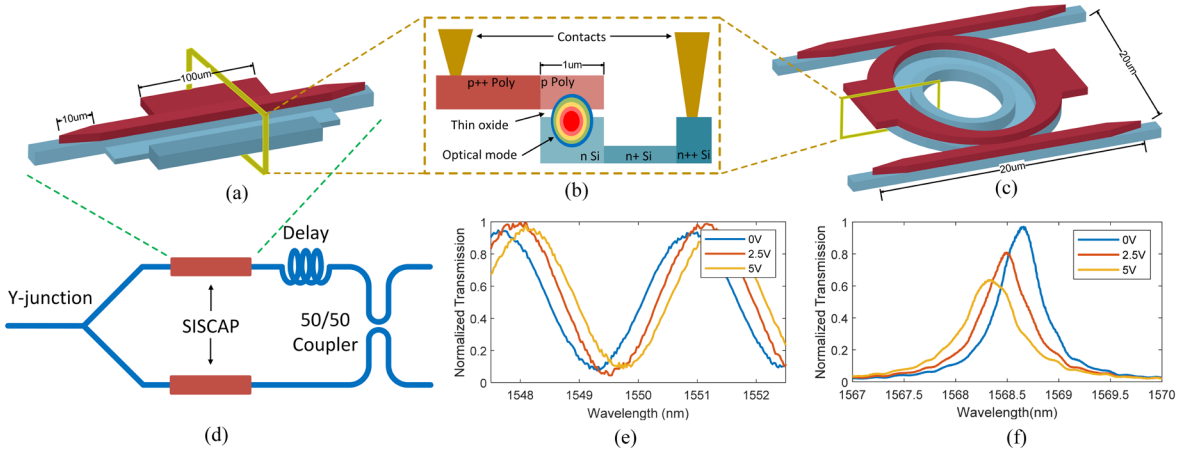

Figure 1. (a) Structure of a capacitive optical phase shifter. (b) Cross-section of a capacitive phase shifter. (c) Structure of a capacitively tuned adiabatic ring resonator. (d) Block diagram of a capacitvely tuned balanced MZI. (e) The tuning response of the MZI in (d). (f) The tuning response of the ring resonator in (c).

structure of the implemented SISCAP phase shifter is shown in Fig. 1(a), where a single mode Si waveguide is tapered to a multimode ridge waveguide with added gate polysilicon on top. The cross-section of this device is shown

in Fig. 1(b), where the optical mode is partially formed in the Si and polysilicon. Here, while the thin layer of oxide does not interfere with the optical mode, it blocks the DC current. In this case, by applying a DC voltage across the capacitor, the charge distribution within the optical mode is adjusted, changing the effective index of refraction of the medium. Figure 1(c) shows the implemented capacitively tuned adiabatic ring resonator, where a SISCAP is incorporated within a ring resonator. Note that adiabatic structure of the ring improves the quality factor and hence the channel-to-channel isolation within the ring based Mux/DeMux. We have also designed and implemented a balanced capacitively tuned MZI (Fig. 1(d)), which is used in the MZI based Mux/DeMux systems. Figure 1(e) shows the measured tuning response of the implemented capacitively tuned MZI, where a tuning slope of about 160 pm/V is achieved. Figure 1(f) shows the tuning response of the implemented capacitively tuned ring resonator, where a Q of about 3.6k and tuning slope of about 130 pm/V is achieved. The break-down of the gate oxide, limits the tuning range for the ring and MZI to about 0.65nm and 0.25FSR, respectively. Note that such zero-power capacitive tuning can also be utilized for ring/MZI modulators, regardless of whether they serve as a part of the DeMux and/or Mux. Another key feature of the implemented Mux/DeMux system is the on-chip sequential control of all blocks, where one on-chip control unit is used to sequentially tune and control all blocks of the system, which significantly reduces the energy consumption and chip area. In this work, as a proof of concept, two 8-channel Mux/DeMux systems one based on capacitively tuned balanced MZIs and another one based on capacitively tuned adiabatic ring resonators are implemented and characterized. Both systems are designed for carrier (comb line) spacing of 200GHz.

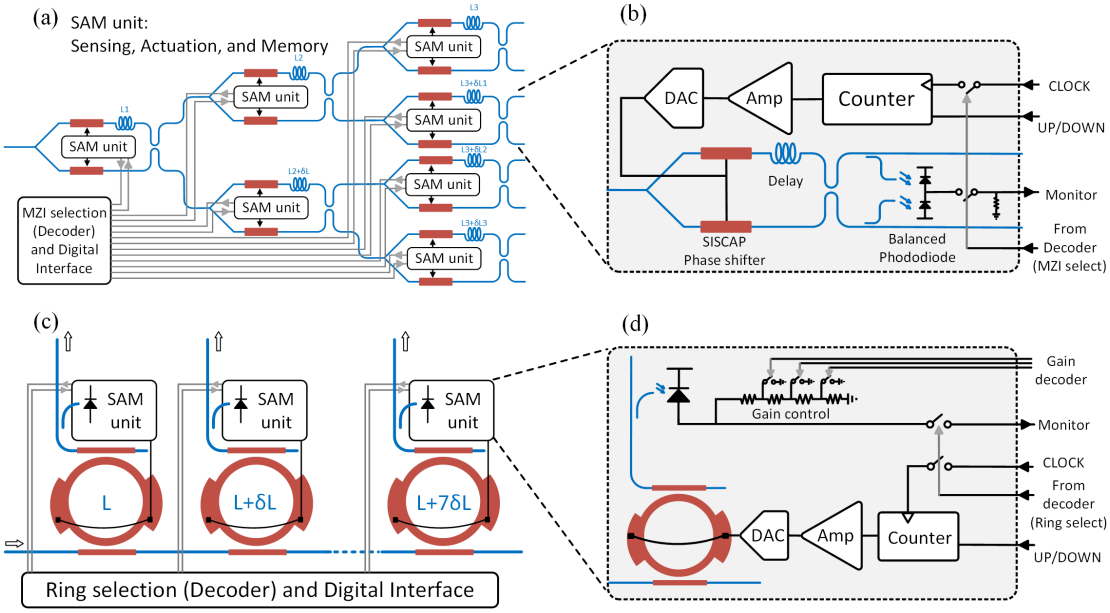

Figure 2. (a) Block diagram of the implemented 8-channel DeMux based on capacitively tuned MZIs. (b) Block diagram of the per-MZI sensing, actuation and memory (SAM) unit. (c) Block diagram of the implemented 8-channel DeMux based on capacitively tuned adiabatic ring resonators. (d) Block diagram of the SAM unit for the system in (c).

Figure 2(a) shows the block diagram of the 8-channel DeMux system formed using 7 capacitively tuned MZIs placed in 3 layers. Each balanced MZI consists of an input Y-junction followed by a delay line on one arm and SISCAP phase shifters on both arms. Two branches are combined using a 50/50 directional coupler. Once correctly tuned, every other carrier (comb) lines that appear at the input of an MZI is selected at its output. The delay difference between the arms of the MZI in each layer is designed to ensure that 8 input carries are separated and appear at the 8 outputs of the DeMux with a high degree of channel-to-channel isolation. A 100μm-long SISCAP phase shifter is placed on each MZI arm. A sensing, actuation, and memory (SAM) unit is placed within each MZI. The block diagram of the SAM unit is shown in Fig. 2(b). In the sequential control of the MZIs, one SAM unit at a time is selected using the decoder within the on-chip MZI selection and digital interface block. Once selected, the clock signal is connected to a 5 bit up/down counter and control system can increment or decrement the count at the edge of each clock cycle using the UP/DOWN signal. The counter output drives the balanced SISCAPs using a digital-to-analog converter followed by a driver. As the MZI is being tuned, a balanced photodiode output (monitoring 5% of each output of the MZI), also controlled by the decoder, is connected to the control system and is used to monitor the status of the MZI. Once the MZI is locked to the desired wavelength, the data is latched into the counter (serving as a memory) holding the MZI at the set point. In this case, the decoder of the MZI selection system selects the next

MZI within the sequence for wavelength locking and process is sequentially repeated. Note that when an MZI is de-selected, its clock is disconnected and the dynamic power consumption of the corresponding SAM unit drops to zero. Therefore, at any given time, only one SAM unit is functional, which significantly reduces the system power consumption. Also, note that, as an important advantage of the proposed sequential control scheme, the energy per bit of the Mux/DeMux decreases as the number of MZIs increases. In other words, sequential control enables use of only one control electronic block for a large number of channels. For example, for a 32 Gb/s per channel system, the power consumption of an 8-channel (256 Gb/s) and 32-channel (1 Tb/s) DeMux/Mux of 10fJ/bit and 2.5fJ/bit is expected which is orders of magnitude lower than the state-of-the-art thermally tuned Mux/DeMux systems. Regardless of the number of MZIs, the digital interface communicates with the off-chip microcontroller using only 7 pads, enabling scalability to a large number of channels. Figure 2(c) shows the block diagram of the proposed DeMux realized using capacitively tuned adiabatic ring resonators, where 8 capacitevly tuned ring resonators with different FSRs are placed in series, separating the 8 carriers at their drop ports. Similar to the system with MZIs, a SAM unit is used to control each ring resonator. The block diagram of the SAM unit for ring resonators is shown in Fig. 2(d), which is similar to that of the MZI. However, here, a single photodiode (PD) detects 5% of the output, and a switchable resistor (used to realize an adjustable gain) converts the PD current into a voltage. The PD voltage is then compared with a pre-programmed threshold value and the driving voltage of the phase shifter is adjusted accordingly. The ring is locked to the peak intensity of its output (drop port) response.

3. Measurement results

A wavelength adjustable laser is used to test the sequential tuning performance. A single-tone laser is coupled to the input grating coupler, MZI blocks are sequentially selected, and the monitor signal is read. The wavelength response of the implemented 8 channel MZI based DeMux before and after wavelength alignment are shown in Figs. 3(a) and 3(b), respectively, where an isolation of better than 15 dB (between adjacent channels) and an insertion loss of under 1.5dB per stage is measured. Total power consumption for tuning and control of 8-channel Mux or DeMux is under 2.5mW. The optical response of an 8 channel capacitively tuned ring based DeMux after automatic adjustment is shown in Fig. 3(c). Figure 3(d) shows the monitor voltage of time multiplexed SAM units demonstrating sequential locking of different channels. Here, once a channel is locked, the system automatically switches to the next channel and the process continues (2 channels shown here). Note that while the locking process typically takes under 10 µs, in this figure, the locking process is slowed down significantly to ease the presentation.

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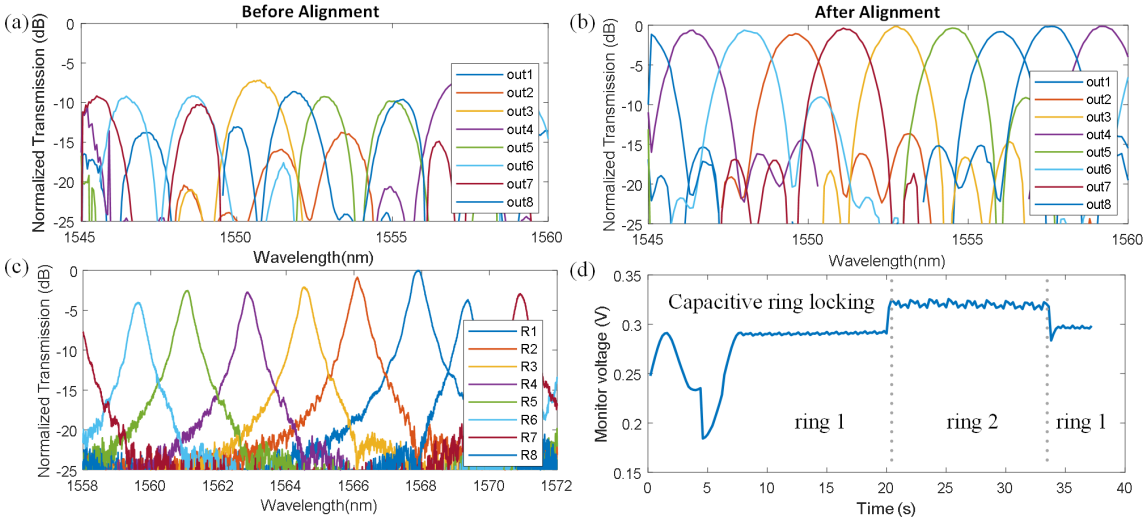

Figure 3. The output spectrum of the 8-channel MZI based DeMux before (a) and after (b) wavelength alignment. (c) Output spectrum of the 8-channel ring based DeMux after wavelength locking. (d) Sequential locking demonstration.

4. References

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