Ultra-dense 3D integrated 5.3 Tb/s/mm^2 80 micro-disk modulator transmitter

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Abstract: A large-scale array of 80 micro-disk modulators is densely bonded to an electronic chip and driven at 10 Gb/s/modulator for an unprecedented 5.3 Tb/s/mm^2 bandwidth density and 50 fJ/bit energy consumption. © 2023 The Author(s)

1. Introduction

Silicon photonics has the potential for extremely bandwidth-dense transceivers due to its high mode confinement waveguides and compact micro-resonators. However, the challenge of integrating photonics with electronics has impeded the realization of such dense transceivers. Monolithic integrations suffer from low transistor density and 3D integrations have been limited by connection pitches greater than 50 um with a maximum bandwidth density demonstrated at 2.6 Tb/s/mm^2 with four modulators [1]. Here, a successful 3D integration with a dramatic reduction in bump pitch to 25 um is demonstrated with an array of 80 micro-disk modulators. Each of the 80 modulators is driven by the bonded 28 nm complementary metal-oxide-semiconductor (CMOS) electronic chip at 10 Gbps with uniform data transmission. In addition, the device consumes a record low 50 fJ/bit at 10 Gb/s and transmits data error-free (BER $<$ 1E-12) down to -11.4 dBm received power. This work presents a clear solution to the communication bottleneck in modern computing with dense optical channels out of electronic chips.

2. Design and Experiment

The array of micro-disks is fabricated on a custom 300 mm photonic wafer through AIM Photonics. Inside the array are 20 buses with 4 modulators per bus, the spectrum of the bus is displayed in Fig. 1a. The modulator is a vertical p-n junction micro-disk that is ideal for CMOS drive voltages due to their high resonance (>80 pm/V) electro-optic response and compact radii (<5 um) [2]. These micro-disk resonance wavelengths are at 1543, 1549.5, 1555.5, and 1561.8 nm and are consistent across each bus in the array. Each bus is fanned out to silicon

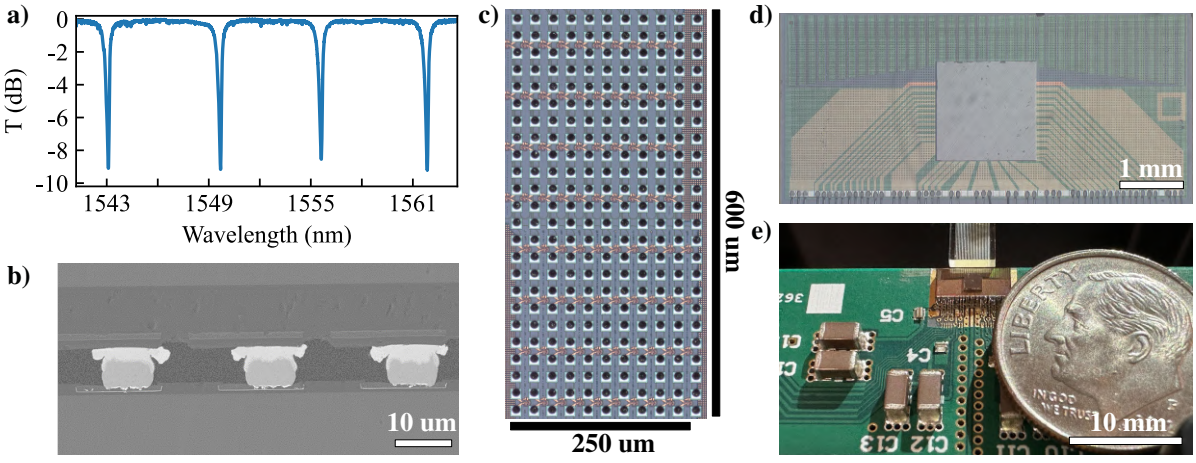

Fig. 1. (a) Spectrum of a four modulator transmitter bus. (b) Cross section SEM of bonded electronic (top) and photonic (bottom) chips. (c) Photonic chip with array of 80 micro-disk modulators after copper pillar bumping. (d) Flip-chip assembly. (e) Flip-chip assembly wirebonded to test PCB with coupled fiber array next to US dime.

nitride edge couplers on a side of the chip with input and output couplers spaced at 127 um for coupling with a standard SMF v-groove array.

The photonic wafer is bumped with tin tipped copper pillars after fabrication. Fig. 1c shows the bumped micro-disk array. Bump pads are 15 um x 15 um at a 25 um pitch with three pads per cell, and the bumps have a 10 um diameter and height. Electronic chips are fabricated through an multi-project wafer (MPW) in the TSMC 28 nm CMOS node. The singulated MPW electronic die are plated with electroless-nickel immersion-gold (ENIG). With both die ready for bonding, the bumped photonic chips were singulated and die-to-die thermo-compression bonded to the plated electronic chips. Cross section SEMs of the bonded dies are shown in Fig. 1b. Pads on one side of the larger photonic chip are wire-bonded to a printed circuit board (PCB). Fig. 1d shows the flip-chip module and Fig. 1e shows the complete assembly on the PCB and coupled to a fiber array on a micro-positioner. The electronic die is 1.6 mm x 1.6 mm and the photonic die is 6.5 mm x 3 mm.

Power supplies, ground, a high-speed clock signal, and SPI controls signals are fed through the wire-bonds to traces on the photonic chip and through bonds to the electronic chip. Each electronic transmitter cell has a 64 bit long register, a driver, and timing circuits with a 2:1 MUX to yield channel data rates at twice the supplied clock rate. The driver is designed for a range of output voltage amplitudes between 1 V and 1.5 V, controlled by the power supply of the driver. A micro-controller PCB is connected to the wire-bonded test PCB and programs each transmitter register to store a PRBS6 pattern. Then, a signal generator provides the chip with a 5 GHz clock and all data registers are cyclically transmitted by their respective modulators at 10 Gb/s. With 80 modulators transmitting data at 10 Gb/s, and the array in Fig. 1c occupying 0.15 mm^2, we show 5.3 $Tb/s/mm^2$.

3. Results

Fig. 2. shows eye diagrams from each modulator being driven at 1.5 V and 10 Gb/s . All transmitters are active at the same time and a tunable wavelength laser is tuned into each modulator resonance and out of the photonic chip for the eye diagrams. Laser power at the modulator is 1 dBm across all measurements and the resulting eyes are open at the receiver with a received average power at -9.5 dBm. No optical amplifiers are used in the

Fig. 2. Eye diagrams from each micro-disk being driven at 10 Gb/s by the 28nm CMOS chip. M 1, 2, 3, 4 correspond to each modulator on the bus.

measurements in this paper. Data transmission was stable and did not require any wavelength adjustment or active thermal control after tuning the laser into the resonance. The sampling oscilloscope receiver is a Tektronix 80C01 module with 8 uW input referred noise, this is the highest contributing factor to the noise in the eye diagrams. The open and uniform eyes from every modulator in the array demonstrates a 100% yield for the bonds between the electronic and photonic chip.

Next, a single modulator is characterized for insertion loss (IL) and extinction ratio (ER). Fig. 3a shows the impact of tuning the laser wavelength into the modulator resonance with 1.5 V driver modulation. Both IL and ER of the eye increase, and the optical modulation amplitude (OMA) at the oscilloscope receiver is maximized for a 2.5 dB IL and 4 dB ER. This performance is compared to lower driver voltage with lower power consumption in Fig. 3b. With OMA maximized, a lower driver voltages accrues more IL and has a lower ER. However, lowering driver voltage to 1 V reduces energy consumption down to 50 fJ/bit. This energy metric is recorded by reading the current and voltage of the driver power rail while every transmitter is modulating. To the best of the authors' knowledge, this is the lowest energy consumption to date for silicon photonic transmitters above 5 Gb/s/modulator.

A direct comparison between driver voltage and link performance is tested by feeding the transmitter output to a commercial receiver (Thorlabs RXM40AF) connected to a bit-error rate (BER) tester. IL is set to be the same for each trial at 2.5 dB and differences in BER curves are determined by ER. Fig. 3c shows the 1, 1.25, and 1.5 V driven data are received error free at -9, -10.4, and -11.4 dBm respectively. The error free data transmission and uniformity of eyes across the array show that all channels can transmit error free down to a received power determined by the receiver.

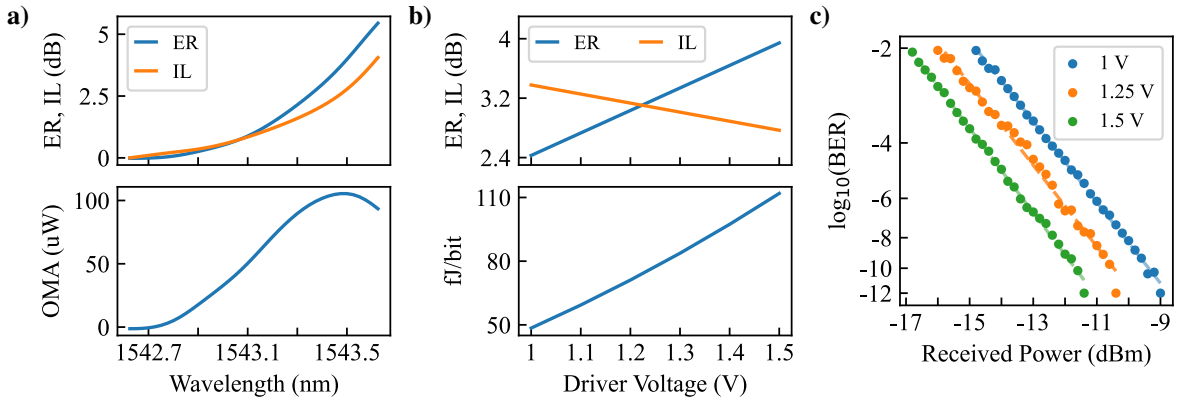

Fig. 3. (a) Extinction ratio (ER), insertion loss (IL), and optical modulation amplitude (OMA) as wavelength is swept into the modulating resonance. (b) ER, IL, and energy consumption (fJ/bit) with driver voltages between 1-1.5 V. ER and IL are recorded at maximum OMA. (c) Bit-error rate (BER) curves of transmitted data received by a commercial receiver at 1, 1.25, and 1.5 V driver voltage.

4. Conclusion

This work demonstrates 800 Gb/s transmission out of a CMOS chip through high-efficiency parallel optical channels in 0.15 mm^2 for a record 5.3 $Tb/s/mm^2$. This integration can seamlessly scale to higher per fiber bandwidths by cascading more micro-disks on fewer buses, enabling the next generation of computing with unrestricted communication bandwidths.

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