Experimental Demonstration of Integrated Low-Cost High-Precision Timing Solution for Optical Transport Networks Supporting 5G

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Abstract:
We successfully integrated FPGA-based low-cost high-precision timing scheme into an optical transport network solution. 16.2 ps synchronisation precision has been achieved across two devices while network-wise setup can sustain up to 21.2 ps precision.

1. Introduction

Precise timing is an essential concept in Optical Transport Networks (OTNs), and it has been used in time synchronisation, delay monitoring and time-sensitive control of the network. With the merge of the 5G Networks, the requirement for precise timing has become necessity due to the time-sensitive new powerful RAN technology. Moreover, the distributed nature of the 5G RAN deployment, a low-cost and precise timing solution is desirable in Open Distributed Units (O-DUs) and Open Radio Units (O-RUs) in 5G Fronthaul [1].

Traditionally, IEEE Precise Time Protocol (PTP) or Network Time Protocol (NTP) [2,3] are utilised as a timing method in OTNs and time stamping is achieved via Global Navigation Satellite System (GNSS) or Global Positioning System (GPS). However, GNSS or GPS based time stamps have limited resolution, and their precision is in the nanosecond range. To push to precision further, Synchronised Ethernet Protocol (SyncE) has been introduced and algorithms such as White Rabbit (WR), achieved precision below 10 ps [4, 5]. Although WR is precise, due to the multiple hardware (PTP and SyncE) and complex circuitry requirements, it is not a cost-effective solution for the 5G Fronthaul.

Time-to-Digital Converters (TDC) have been used for precise time measurement in science and engineering applications. TDCs can digitise events happening in the time domain with high-precision and generate time stamps for input triggers with respect to the edge of its master clock [6]. There are many TDC schemes such as delay lines, Vernier methods, wave unions, and they have achieved high-precision around 10 ps by using low-cost hardware such as Field Programmable Gate Arrays (FPGA) [6]. Modern FPGAs are packed with many reconfiguration options with high capacity Physical (PHY) and Medium Access Control (MAC) network layer interface capabilities such as 10G/100G Ethernet subsystems, and they are commonly found in DU and RU hardware in 5G Networks. Hence, a precise timing solution could be integrated within the FPGA fabric as part of the 5G Network hardware to reduce deployment costs.

Previously in [7–9], we have demonstrated reconfigurable, key slicing QKD-enabled hardware encryption and network resilience within our network solutions. In this paper, we propose a low-cost, high-precision timing solution, which could be integrated into a transport network solution to be employed in a 5G Fronthaul deployment. In this research, we are introducing time-stamping modules for each client and a time-synchronisation module that handles the sync channel between the network nodes. This solution has successfully achieved 11.4 ps precision on a single FPGA chip and a synchronisation channel between 2-FPGAs was established with a precision of 16.2 ps. Also, our solution managed to synchronise the nodes with a precision of 21.2 ps.

2. Integrated Low-Cost High-Precision Timing Solution Network Architecture

Our timing solution and its deployment in our testbed network can be seen in Fig.1. Each node of the network accommodates the Xilinx VCU108 FPGA board (Xilinx Virtex Ultrascale FPGA) and connects up to 16 $\times$ 10G clients and 1 $\times$100G between two network nodes. Clients are connected to the FPGA via 10G Small Form-Factor Pluggable (SFP) transceivers. 100 G Link has been implemented via utilising Quad Form-Factor Pluggable (QSFP). Connection with the Software-Defined Networking (SDN) controller has been established via PCI-E bus.

Time Stamper logic measures the arrival time of the frames precisely from the 10G Media-Independent Interface (XGMII) of the Physical Coding Sublayer (PCS) / Physical Medium Attachment (PMA) Layer for improved latency and accuracy. TDC module is similar to the architecture described in [10], a delay-line has been utilised to subdivide the clock period in to smaller time bins to implement the fine timing and a master clock has been used for generating the coarse counter. For the master clock 312.5 MHz low-jitter 100G transceiver clock has been utilised. TDC has been implemented by using 1024-bit Xilinx CARRY8 primitive-based carry chains. The resolution of

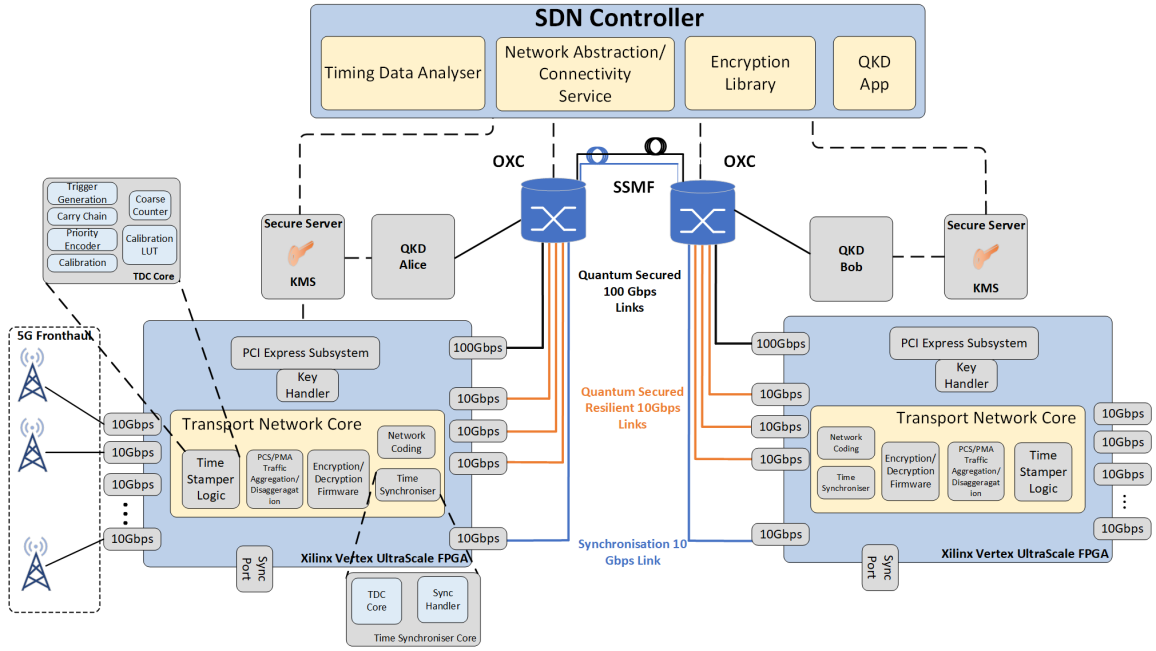

Fig. 1. Integrated low-cost high-precision timing in a transport network solution architecture

the TDC (T_{Res}), can be calculated like $T_{Res} = \frac{T_{clk}}{N} = \frac{3.2\ ns}{1024} = 3.12\ ps$, where T_{clk} is the clock period and N is the number of delay elements. A priority encoder generates a 10-bit value for a 1024-bit delay line thermometer code. Code Density Testing based calibration has been employed to address the non-linearity issues of the delay line, and a Look Up Table (LUT) of calibrated time stamps has been created within the FPGA.

Time synchronisation generates time stamps for the rising edges of the external reference by using a TDC and time stamps exchanged between FPGAs via 10G Sync Link. The external trigger is a free-running clock at 1 MHz and is distributed to both nodes. The time difference between time stamps for the external trigger is used to calculate the OFFSET between two FPGAs, and the most recent OFFSET is used for syncing the time stamps of network nodes.

3. Experimental Results

To assess the precision of the TDC, a timing jitter measurement was conducted by feeding the module with a periodic input trigger, and the time differences between each measurement step were recorded. In Fig.2, TDC architecture used in this implementation, 1 and 2-FPGA-based timing jitter measurements can be seen. 1-FPGA precision experiment was conducted by employing a wave function generator (Rigol DG4102) and feeding the system through the sync port with 1 MHz square waves. 10000-time stamps were generated and transferred to the PC via PCI-Express bus. In MATLAB environment, by using the histogram and standard deviation (σ) function, the spread of time differences were analysed. As it can be seen from Fig. 2 b) Full-Width-Half-Maximum (FWHM) of the spread was 37.4 ps and σ = 16.2 ps. Single-Shot Precision (SSP) ($\frac{\sigma}{\sqrt{2}}$) was calculated as 11.4 ps.

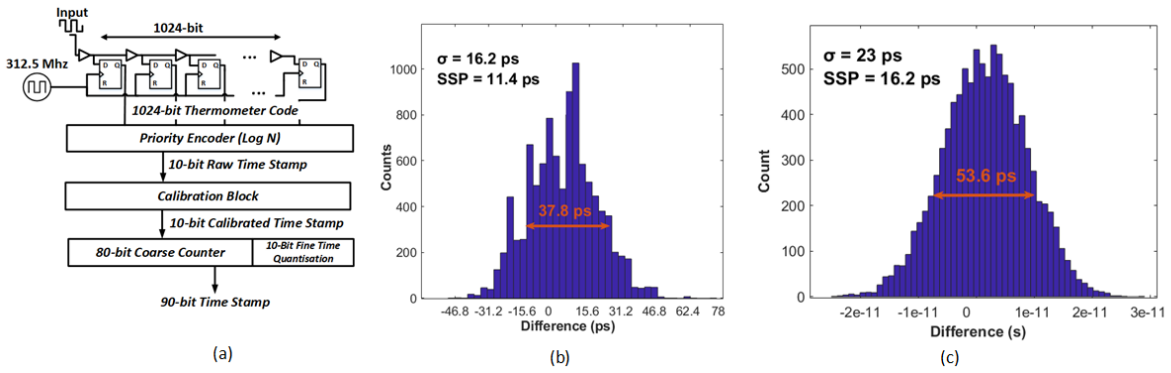

Fig. 2. a) TDC architecture, b) 1-FPGA timing jitter measurement, c) 2-FPGA timing jitter measurement

To determine the precision across 2 FPGAs, the same timing jitter measurement experiment was repeated with 2 FPGA boards. The generated time stamps were transferred from SLAVE to MASTER FPGAs via Sync link and the Time OFFSET between the two devices was measured. In Fig.2 c) , the timing jitter of 2-FPGAs can be seen; this information also reveals the precision of the synchronisation OFFSET. σ of OFFSET has been measured as 23 ps, FWHM was 53.6 ps and SSP was 16.2 ps, so, the precision of the sync channel has been measured as 16.2 ps.

To identify the scheme's precision in a scenario similar to the 5G Network deployment, we measured the precision of the time stamps generated for the frames in both devices. In this test, a server computer was used to generate time stamps at a rate of 1 million frames per second and output via 10G SFP. In order to duplicate the frames and direct them to the client side of both FPGAs, a third FPGA was utilised. SLAVE device added OFFSET value to its time stamps which were sent via synchronisation link from the MASTER. After 10000-time stamps were generated, time stamps were transferred to the PC for analysis. In Fig.3, the time differences between the two devices' time stamps in a histogram can be seen. It should be noted keeping the frame arrival times periodic and consistent for a long time is not possible in a network scenario due to a large amount of hardware and software processing. Thus, the timing difference between frame arrival times kept changing and multiple timing patterns were observed. In Fig.3, the frame arrival times demonstrated 7 correlated timing patterns, which resulted in 7 Gaussian Peaks. As it can be seen in Table 1, when the peaks were analysed, the σ values were between 30.7 ps - 63.5 ps, FWHM between 72.4 ps-149.7 ps and SSPs between 21.2 ps - 44.9 ps. Thus, the highest precision achieved for synchronisation of the Ethernet frames between multiple devices was 21.2 ps.

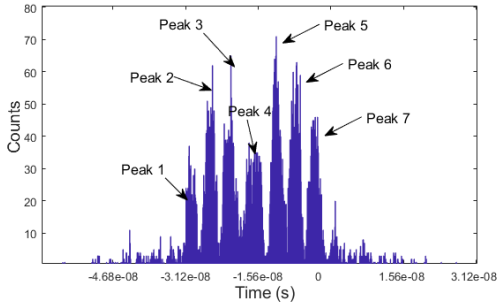

Fig. 3. Timing jitter of a network traffic

Table 1. Experimental Results

Peak	σ (ps)	SSP (ps)	FWHM (ps)
1	30.7	21.2	72.4
2	53.9	38.1	127
3	44.3	31.3	104.4
4	32.3	22.8	76
5	63.5	44.9	149.7
6	57.9	41	136.5
7	47.3	33.4	111.2

4. Conclusion

To sum up, we have successfully implemented an FPGA-based low-cost and high-precision timing solution which could be easily integrated into a transport network solution and can be a part of the 5G Network deployment. In a single FPGA, a precision of 11.4 ps has been recorded. Two node synchronisation has been observed as 16.2 ps. Finally, synchronisation has been utilised in network traffic, and the time stamps generated across two devices have been observed to be in sync with up to the precision of 21.2 ps.

Acknowledgements

This work was funded by a EU funded project 5G-COMPLETE (871900) and a DCMS funded project Future RAN: Proteus. Part of the research leading to this work was supported by the Quantum Communication Hub funded by the EPSRC grant ref. EP/T001011/1.

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