

# Self-Homodyne Coherent Transmission with All-Optical Clock Synchronization for DSP-Free Co-Packaged Optics

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**Abstract:** Utilizing the all-optical clock delivery and synchronization, we successfully achieved baud-rate sampled 40-Gbaud DP-16QAM self-homodyne transmission with 1.92 Tbps aggregated capacity over 3.5-km MCF, yielding a promising solution for the DSP-free coherent co-packaged optics. © 2023 The Author(s)

## 1. Introduction

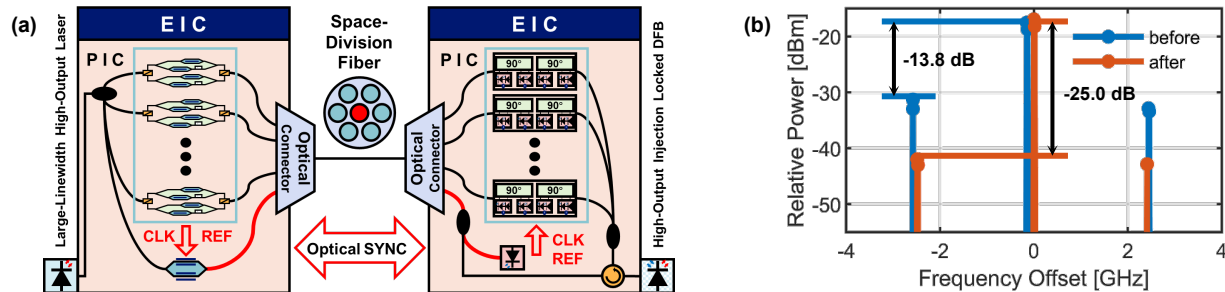
Recently, the Ethernet speed of data center optics is anticipated to pace from 400 G to 800G/1.6T and even beyond. Shortly, the bottleneck of traditional pluggable optics will be revealed with an increased interface speed. This is because the ultra-high-speed radio-frequency connections between the pluggable optical transceivers and the electrical switching ASICs suffer from severe impairments, generating much greater power dissipation [1]. The co-packaged optics (CPO) solutions can cope with this problem by integrating the electronic ICs (EIC) and the photonic ICs (PIC) as close as possible and switching optically. Owing to the high spatial density of the co-packaged optics, the power consumption must be strictly restrained, especially for the DSP. The self-homodyne coherent detection (SHCD) can achieve supreme capacity density per connector with considerable power efficiency for CPO applications [2]. However, even with the significantly simplified DSP, the SHCD still requires the digital clock recovery thus hinders the progress towards DSP-free. In [3,4], optical clock synchronizations (O-SYNC) in IMDD schemes were demonstrated to achieve sub-nanosecond clock recovery by occupying one lane to parallelly distribute the optical clock.

In this paper, we propose to all-optically recover the clock tone by remotely delivering clock-embedded local oscillator (LO) in the SHCD. Clear constellations can be acquired by the baud-rate sampling ADCs without any DSP. Further, with a simple DSP operating at baud-rate sampling, we successfully realize baud-rate sampled 40-Gbaud DP-16QAM SHCD reception at a BER of  $1.0 \times 10^{-2}$ . With an extremely simplified DSP operating at twice the baud rate, an aggregated capacity of 1.92 Tbps over a 3.5-km 7-core MCF is achieved. The promising DSP-free coherent co-packaged optics scheme can be facilitated constructively.

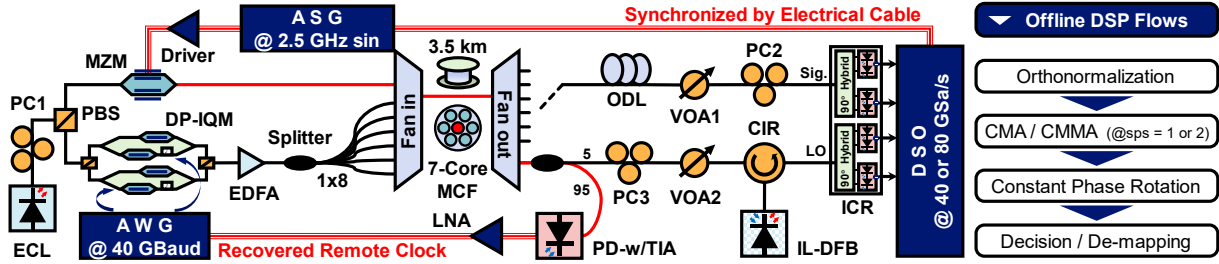
## 2. Architecture and Principles

The proposed optically synchronized CPO architecture is shown in Fig. 1 (a). The optical reference clock is loaded into the remotely delivered LO light by an intensity modulator, propagating along with the signal light through the fiber link. At the Rx-end, the clock-loaded LO is detected by a photodetector and converted to electrical clock pulses for synchronization. In the proposed structure, the optical modulators or receivers are integrated into one PIC chip, so they naturally share the reference clock. One branch of the optical clock signal will simultaneously synchronize all Tx and Rx units. The delay-matched SHCD link will ensure that the sampling clock is aligned with the data signal.

However, the clock-loaded LO will interfere with the data signal thus an injection-locked FDB laser (IL-DFB) is introduced to erase the intensity fluctuation of the interference and to regenerate the LO with high power and low noise for SHCD. As shown in Fig. 1 (b), the 2.5-GHz clock impairment is reduced from -13.8 dB to -25 dB by the IL-



**Fig. 1** (a) The proposed O-SYNC SHCD structure for CPO. (b) The clock interference on LO is reduced by the IL-FDB.



**Fig. 2** Experimental setup and the simplified DSP flows. ASG: Analog signal generator; MZM: Mach-Zendel modulator; ECL: External-cavity laser; PC: Polarization controller; PBS: Polarization Beam Splitter; DP-IQM: Dual-polarization I/Q modulator; MCF: Multicore fiber; ODL: Optical delay line; CIR: Circulator; ICR: Intradyne coherent receiver; AWG: Arbitrary waveform generator; LNA: Low-noise amplifier; PD-w/TIA: Photodiode with transimpedance amplifier; DSO: Digital sampling oscilloscope; CMA: Constant modulus algorithm; CMMA: Cascaded multi-modulus algorithm

DFB. The erasing effectiveness will be enhanced with higher clock frequency and lower modulation depth, because of the narrow-bandwidth filtering property of IL-DFB.

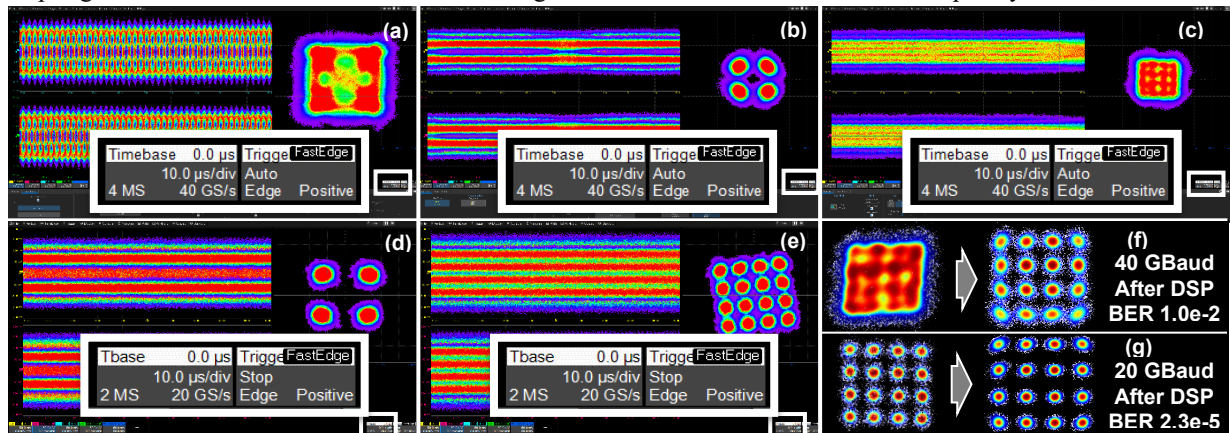
### 3. Experimental Setup

In our offline lab experiment, the synchronization based on the reference clock signal depends on the phase lock loops (PLL). The locking frequency of the PLL in the DSO (LeCroy Lab Master 36-Zi) is invariable, but the one in the AWG (Keysight 8196A) is variable from 10 MHz to 17 GHz. For this reason, the 2.5-GHz reference clock must be sent reversely from the Rx-end to the Tx-end in this experiment. As the *red lines* shown in Fig. 2, the ASG is electrically synchronized with the DSO and generates a synchronized 2.5-GHz sinusoidal analog signal to drive the MZM. After propagating to the end of the link, the optical clock is detected and amplified by the PD and LNA. Even though, strictly, there is a 35- $\mu$ s (7-km) delay between the AWG and the DSO, the phase noise of two PLLs is negligible, and results in tiny timing jitter.

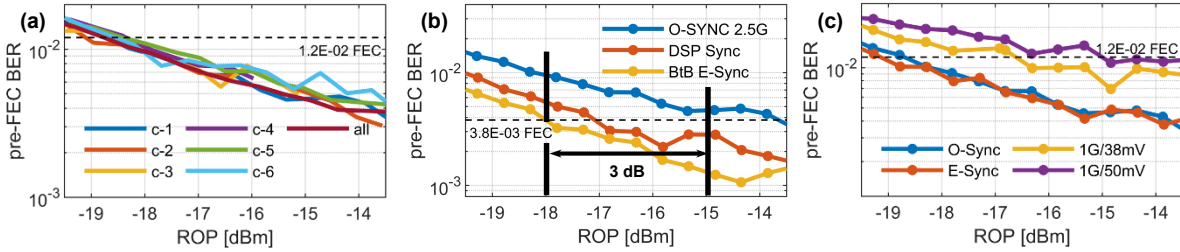
For the SHCD transmission, a space-division multiplexing scheme is adopted, as Fig. 2 shows. The PC1 and the PBS are used to split the laser source into 2 beams with a certain carrier-signal power ratio (CSRP). One of them is modulated with 40-Gbaud DP-16QAM signals and the other one is used as clock-loaded LO. The EDFA compensates for the insertion loss of the 1x8 splitter. 6 copies of the modulated beams and the clock-loaded LO are coupled into the 7-core MCF. Propagated by 3.5 km, 95% of the clock-loaded LO is split to recover the clock. Only 5% of the clock-loaded LO is injected into the IL-DFB to regenerate the LO. The input and output power of the IL-DFB are about -20 dBm and 13 dBm respectively. The PC3 was set to impose the polarization fading effect of LO, but we found it does not matter in this system. The DSO operates at 40 GSa/s (for single baud-rate sampling) or 80 GSa/s. The DSP flows include orthonormalization, CMA/CMMA for polarization demultiplexing and channel equalization (with 1 or 2 samples per symbol), constant phase rotation, and decision. There is no digital clock recovery in the flows.

### 4. Experimental Results and Discussions

The single baud-rate reception results are shown in Fig. 3. When no synchronization between the Tx and the Rx, the sampling clock is mismatched with the transmitting clock. With about 450-kHz clock frequency offset, the baud-rate



**Fig. 3** The screen captures of the oscilloscope when baud-rate sampling. When no optical clock synchronization, the timing jitter makes the constellation unrecognizable, shown in (a). After the proposed synchronization, the real-time constellation become much better at 40 Gbaud (b, c) and 20 Gbaud (d, e). Utilized the single-SPS DSPs, the results are shown in (f, g).



**Fig. 4** (a) The performance of the 6 cores after 3.5-km transmission. (b) Comparison of the effectiveness of the different clock synchronization schemes. (c) Analysis for the cost of the optical clock synchronization.

sampling constellation is a total mess, as shown in Fig. 3 (a). With the O-SYNC, the polarization demultiplexing of the 40-Gbaud QPSK and 16QAM signal can be implemented by PC2 by hand, shown in Fig. 3 (b, c). When the transmitting rate drops to 20 Gbaud, the dispersion effect is negligible, hence the constellation is much clearer. The QPSK signal is even free of error (100- $\mu$ s duration, BER < 5e-7), as shown in Fig. 3 (d, e). Applied with the baud-rate operating DSP, the 40-Gbaud DP-16QAM signal can meet the 1.25e-2 FEC threshold, shown in Fig. 3 (f, g).

The transmission experiments are under an 80-GSa/s sampling rate. Each core meets the 1.25e-2 FEC threshold at about -18.5-dBm received optical power (ROP). When 6 cores are launched at the same time, the cost is negligible compared to separately launched, as shown in Fig. 4 (a). The total capacity is  $0.32 \times 6 = 1.92$  Tbps.

## 5. Discussions on the Performance

However, erasing the clock still results in about 3-dB penalty compared to the back-to-back electrical synchronization by cable (E-SYNC), as shown in Fig. 4 (b). In comparison, the cost of the offline DSP of retiming (Gardner) is about 1 dB. Even though the performance of the O-SYNC scheme is worse than the retiming DSP by 2 dB, the cost is possible be compensated or mitigated. That is because the 3-dB cost of O-SYNC is induced by the phase distortion of the IL-DFB, rather than the jitter of the optical clock. The test results are shown in Fig. 4 (c). The blue line is the case when applying 2.5-GHz O-SYNC, and the red line is the case applying the E-SYNC when the LO is clock-loaded and regenerated by IL-DFB. Both lines are almost overlapped, which can tell the synchronization performances of the two schemes are the same.

We shall briefly analyze the causes of the phase distortion of the IL-DFB. When the injecting ratio (the ratio of the input power to the output power) of the IL-DFB varies, its output phase offset varies accordingly [5]. As a result, the loaded clock makes the injecting power fluctuate, thus leading to the additional periodic phase distortion of LO. To reduce the phase distortion of the IL-DFB, it is feasible to increase the optical clock frequency or decrease the modulation depth of the clock signal. As shown in Fig. 4 (c), when the clock frequency is 1 GHz and the modulation magnitude is 50 mV-RMS (the same as that of the 2.5-GHz case), the penalty by phase distortion is 3 dB. When the modulation magnitude decreased to 38 mV-RMS, the penalty is only 2 dB. Following this trend, if the clock frequency is increased to 10 GHz or higher, the phase distortion cost will be much less, even approaching the performance of the E-SYNC.

## 6. Conclusions

We propose an ultra-simplified architecture of SHCD structure for the DSP-free co-packaged optics. By using optical clock synchronization, we successfully realize baud-rate sampled 3.5-km-propagated 40-Gbaud DP-QPSK reception without any DSP. With the simplified DSP operating at baud rate sampling, the 40-Gbaud DP-16QAM signal can achieve the BER of 1.0e-2. Also, we demonstrate the transmission experiment with an aggregated capacity of 1.92 Tbps over a 3.5-km 7-core MCF. In this way, the promising DSP-free coherent co-packaged optics scheme can be constructively facilitated.

## Acknowledgments

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## References

- [1] C. Minkenberg, R. Krishnaswamy, A. Zilkie, and D. Nelson, *IET Optoelectron.*, vol. 15, no. 2, pp. 77–91, 2021, doi: 10.1049/ote2.12020.
- [2] T. Gui *et al.*, in *2022 Optical Fiber Communications Conference and Exhibition (OFC)*, Mar. 2022, Th4C.1.
- [3] K. A. Clark and Z. Liu, *J. Light. Technol.*, vol. 40, no. 6, pp. 1681–1689, Mar. 2022, doi: 10.1109/JLT.2021.3130955.
- [4] Z. Zhou, K. A. Clark, C. Deakin, and Z. Liu, *J. Light. Technol.*, vol. 40, no. 6, pp. 1735–1741, Mar. 2022, doi: 10.1109/JLT.2022.3148776.
- [5] Z. Liu and R. Slavik, *J. Light. Technol.*, vol. 38, no. 1, pp. 43–59, Jan. 2020, doi: 10.1109/JLT.2019.2945718.