Optical RAM and Optical Cache Memories for Computing

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Abstract: In this paper, we present the recent progress and achievements of optical RAM technologies expanding from single RAM cells up to fully functional optical cache memory implementations for future Computing architectures.
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1. Introduction

Over the past years, the growing demand for high-bandwidth processing has highlighted an evolving gap between processor performance and data bandwidth also known as Memory Wall problem[1]. This bottleneck has in turn raised new serious concerns on the applicability of future computing processing progress since it is directly linked to two different critical problems: (a) the limited speed performance of state-of-the-art electronic random-access memory (RAM) with clock speeds of a few GHz [2] hat severely affects latency-sensitive information processing applications and (b) the limited bandwidth offered by the processor-main memory electrical interconnects, where wiring density and its associated power dissipation sets an upper limit to the achievable data throughput[2]. To cope with this situation, designers have adopted deep memory hierarchies, occupying unfortunately more than 40% of the CPU chip real estate [3] with on-chip cache memories and their associated interconnects. Within this frame, the research community has resorted to optics for delivering high-bandwidth and energy-efficient photonic integrated memories that could revisit the traditional Von Neumann computing architectures. A complete set of novel optical latching mechanisms has been launched [4]-[8] providing high-speed operation[5] with credentials to reach up to 40Gb/s[7], decreased footprint[6], and energy efficiency[8]. Significant demonstrations have also indicated that using Wavelength Division Multiplexing (WDM) -enabled high-speed optical interconnects and optical memories together can be rather beneficial to disintegrate CPU processing from storage through alternative off-chip memory schemes [8],[9]. The migration, however, to practical optical RAMs in a future viable roadmap should satisfy a demanding framework covering performance metrics, functional system-level organization, and application perspectives at the same time.

In this paper, we present a holistic overview of the recent progress achieved in the area of optical RAM technologies expanding from single compact RAM cells [10] exploiting simple generic broadband latching elements to facilitate capacity scaling up to WDM-enabled multi-bit RAM bank implementations [11]-[13] with advanced organization functionalities where seamless and transparent cooperation between RAM subsystems is achieved and ending up to complete fully-functional off-chip optical cache memory hardware[14] implementation suitable computing applications. The proposed schemes reveal how WDM technique -only available in optics- can transform traditional memory setups to novel configurations with increased simplicity and energy efficiency through hardware sharing. All critical performance metrics of the proposed schemes are also discussed outlining that record-high speed capabilities and sub-μm^2 footprints can be achieved by optics [8], in combination with bitrate-transparent power consumption that cancels the trade-offs between access time and energy efficiency witnessed in electronics.

2. Optical RAM technology and architecture

A simple generic broadband latching element for single bit storage that simultaneously facilitates ease of capacity scaling and simplicity in large-scale optical memory implementations has been for long the main goal in the research community [8]. In this frame, we have designed and validated a novel photonic integrated circuit (PIC) as shown in Fig.1 that was initially tested as a standalone device and then used as the main building block in the following advanced WDM-enabled optical RAM architectures. The device relied on a typical master-slave coupled switch configuration [4]-[8] and exploited cross-phase modulation (XPM). The GDS mask layout is illustrated in Fig.1a). The monolithically integrated InP PIC was fabricated by HHI and optically and electrically packaged by PHIX to facilitate easier system level testing. The fully packaged device is shown in Fig. 2 (b). The device was evaluated as a high-speed optical RAM cell at 5Gb/s using an external hybridly integrated SOA-MZI as the single Access Gate (AG) mechanism achieving successfully Read/Write operation. Experimental results of Write operation including time pulse traces and eye diagrams at 5Gb/s are depicted in Fig.1c).

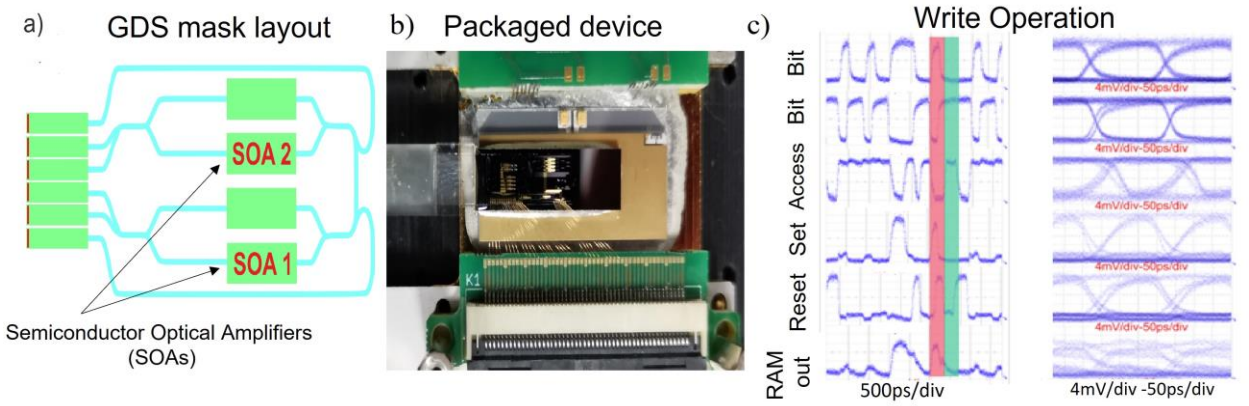

Fig. 1. a) GDS mask layout of the fabricated optical XPM-based FF, b) The packaged InP monolithic FF device and c) (left) Time trace for the principle of operation of an optical RAM cell at 5Gb/s Write functionality. Time scale at 500ps/div. (Right) The respective eye diagrams. Time scale at 50ps/div.

3. Towards 2D multi-bit RAM with decoding functionalities

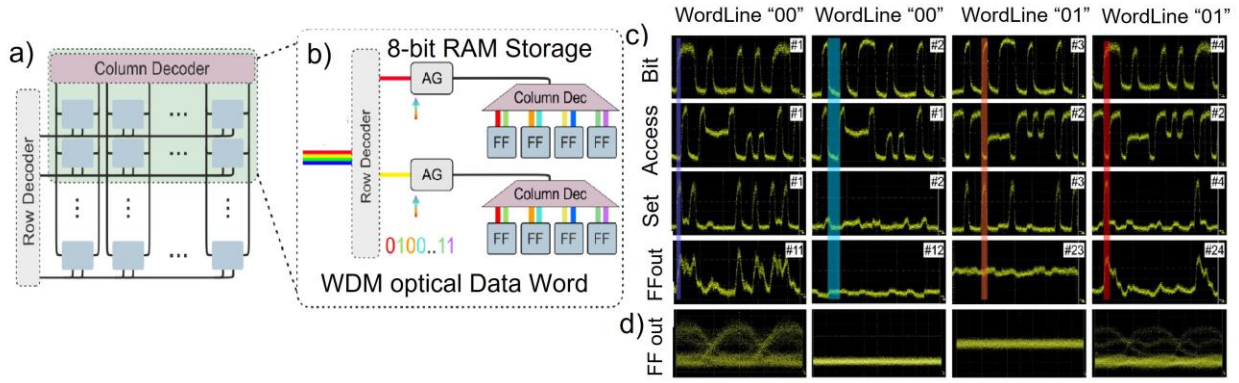

Fig. 2. a) Concept of a 2D optical RAM Bank and b) 8-bit optical RAM unit with Row and Column decoder stages. (b) Experimental results of the 8-bit optical RAM , the Write operation with (c) pulse traces for proof of operation are represented indicatively for four out of the eight FFs, for Word Line '00' FF11 and FF12 outputs and for Word Line '01' FF23 and FF24 (d) respective eye diagrams.

The next step was to evaluate several 2-dimension (2D) RAM concept enriched with decoding capabilities [11]-[13]. A recent implementation[12] of an optical RAM bank with a capability of 8-bit storage organized in two RAM Rows together with the necessary optical Row and Column Decoder circuitry is shown in fig.2(a)-(b) incorporating two multi-wavelength AGs for the two RAM rows. The evaluation of the 8-bit optical RAM storage included all 2×4×5Gb/s incoming WDM-formatted NRZ data streams forming the two 4-bit WDM Data words and the obtained experimental synchronized time traces are illustrated in Fig. 2(c)-(d). For simplicity reasons only four out of the eight FF outputs are presented, namely the FFs 1-2 from WL "00" and FFs 3-4 from WL "01". The respective eye diagrams obtained were all clear and featured an extinction ratio (ER) of 2.6dB.

4. Off-chip optical cache hardware architecture

Exploiting the aforementioned WDM-enabled RAM concepts, an optical cache memory hardware prototype was implemented including four Cache Lines (CLs) with 2 Flip Flops (FFs) per line, a passive Row/Column Decoder circuit and a Tag Comparator circuit, forming together the necessary all-optical peripheral toolkit required in complex high-scale cache architectures. The architecture [14] was successfully tested for Write/Read operation of WDM-enabled optical Data words with a 10 Gb/s memory throughput. The 4x2-bit optical RAM bank is addressed via a passive filter-based Optical Row Decoder (RD) and a passive demux-based Column Decoder (CD). Every CL incorporates two discrete fully packaged monolithic integrated InP optical FFs connected via an AWG-based CD circuit to a single multi-λ SOA-MZI Access Gate (AG). Cache hit or miss is decided directly in the optical domain by means of an optical Tag Comparator. Experimental validation is achieved for an aggregate CL throughput of 2×5Gb/s, demonstrating. The respective eye diagrams obtained for Write and Read outputs are shown in Figs. 2(d) and (f), were clear and featured an extinction ratio (ER) of 2.6dB.

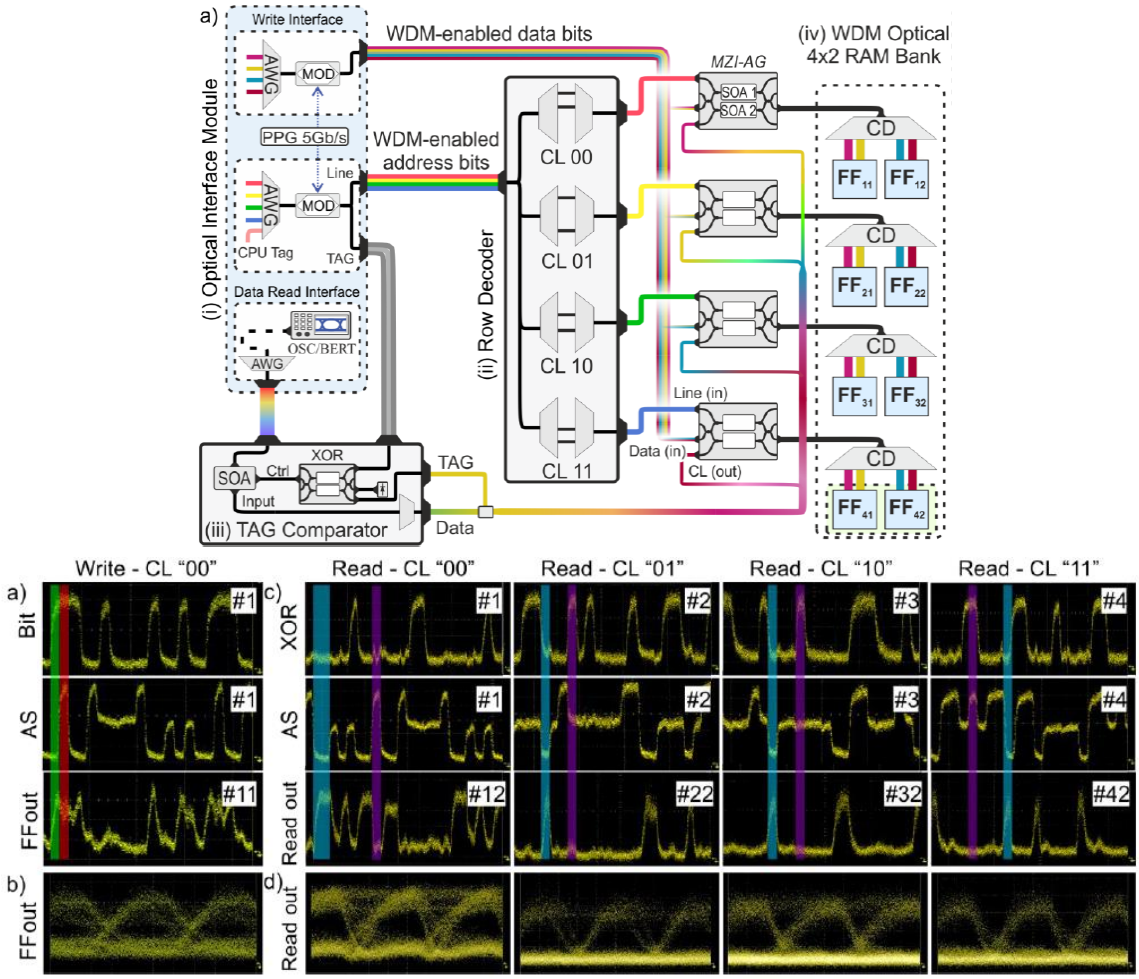

Fig.3 (a) Experimental setup of thee 8-bit cache memory evaluation at 10 Gb/s, Pulse traces of the 8-bit cache memory b) for Write operation of FF11 in CL "00", c) the respective eye diagram, d) traces for Read operation and e) the respective eye diagrams. Time scale is at 500ps/div for traces and 50ps/div for eye diagrams.

5. Conclusion

The developments in optical RAM and cache memories for computing deployments have been reviewed, outlining the main experimental results and key performance metrics towards releasing new architectural and technology paradigms capable to overcome the main bottlenecks in today's computational settings.

Acknowledgements

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