# Power dissipation bounds for photonic analog to digital converters

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**Abstract:** We present the first power dissipation bounds for a generalised class of photonic analog to digital converters, and estimate their achievable power efficiency compared to conventional electronic designs. 

## 1. Introduction

Analog to digital converters (ADCs) are ubiquitous devices found in any system that requires the digital processing or storage of continuous time signals. The speed, accuracy and efficiency of ADCs can profoundly impact system architectures and overall performance across a huge variety of applications, including optical and wireless communications, electronic warfare, medical imaging, and instrumentation. In optical and wireless communications systems, the accuracy of the high speed ($>1$ GHz) ADCs required to digitise high baudrate signals is often limited by clock jitter or comparator ambiguity, which can limit spectral efficiency and modulation format flexibility.

This well known trade-off between sampling speed and digitisation accuracy, characterised by signal to noise ratio (SNR) or effective number of bits (ENOB), is a key challenge in ADC design. Many have proposed photonic designs to combat this trade-off [1]: optics based samplers and converters that exploit the high bandwidth and low jitter of optical sources, with a wide variety of published photonic ADC architectures demonstrating performance well in excess of state of the art electronic ADCs (e.g. 7 bits ENOB at 40 GHz [2, 3]). Despite this impressive performance there has been, to the best of our knowledge, little to no discussion of the power efficiency of photonic ADCs. Power dissipation and efficiency are critical factors in determining the performance of ADCs, especially in communications systems that are designed to minimise the energy consumption or cost per bit transmitted [4, 5]. Therefore, assessing the power consumption and efficiency is essential to determining whether the impressive speed-resolution performance afforded by photonic ADCs can translate into real-world improvements in network capacity and efficiency in energy sensitive applications [6].

In this paper, we derive lower bounds on the power consumption of photonic ADCs. We discuss how the main active components required to implement a photonic ADC impact the overall energy per sample, and compare the power efficiency performance of common photonic ADCs to conventional electronic ADCs in terms of the widely used Schreier figure of merit, $\mathrm{FOM}_S = \frac{\Delta f \times \mathrm{SNR}}{P}$ [4, 7], for Nyquist bandwidth $\Delta f$ and power consumption $P$.

## 2. Power dissipation bounds

Although photonic ADCs have been demonstrated with a wide variety of architectures [1], most of the best performing designs can be described as a variation of the generalised model shown in Fig. 1(a) [2, 3, 9, 10]. This model is generalised in the sense that it contains the minimum active components required to implement a photonic ADC: a pulsed laser source as the optical sampling device, an electro-optic modulator to map the input signal onto the optical pulse train, followed by a bank of $N$ channels containing a photoreceiver and electronic sub-ADC

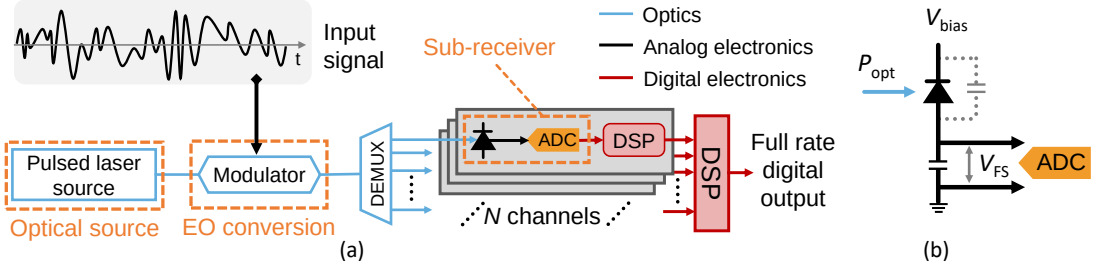



Fig. 1. (a) Generalised model of a photonic ADC, with principal active components highlighted in orange. (b) Sub-receiver model: the illuminated photodiode switches an ADC input, represented as a capacitive load, to the full scale voltage $V_{FS}$ [8].

that detect subsets (either in the time [2, 9] or frequency [3, 10] domains) of the incoming signal in parallel at a fraction of the aggregate sampling rate. The signal is then reconstructed digitally to obtain the full rate signal at the much higher resolution offered by such optical techniques. The power consumption contribution of the required restitching digital signal processing (DSP) is not considered here since it is the same for interleaving electronic ADCs, which are the most common designs at high sampling rates, so is not relevant for comparison.

Considering the highlighted active components in Fig. 1, we can derive an expression for the energy per sample of a photonic ADC digitising an input signal defined only by its peak to average power ratio (PAPR)

$$P/f_s = \frac{P_{\text{opt}}}{f_s}\left[\underbrace{\frac{4\pi^2 R V_{\text{bias}}}{\text{PAPR}}}_{\text{sub-receiver}} + \underbrace{\frac{1}{\eta_{\text{WPE}}}}_{\text{laser source}}\right] + \underbrace{\frac{f_s V_{\Delta f}^2}{4Z_0 \times \text{PAPR}}}_{\text{modulator}} \tag{1}$$

for sampling rate $f_s = 2\Delta f$, photodiode responsivity $R$, photodiode bias $V_{\text{bias}}$, laser wall plug efficiency $\eta_{\text{WPE}}$. The modulator is assumed to be a travelling wave Mach-Zehnder modulator of input impedance $Z_0$ and $V_\pi = \Delta f V_{\Delta f}$, where $V_{\Delta f}$ is the modulator $V_\pi$ per Hz bandwidth (in volts per Hz), which is driven such that the peak value of the input signal is equal to the full modulation depth of the modulator (hence the PAPR factor in (1)). It is assumed that the modulator nonlinearity can be compensated through simple digital compensation [11]: the factor $4\pi^2$ comes from the linearized modulator transfer function. Note that actual photonic ADCs will contain additional passive components: e.g. a pulse interleaver [2], filters and gratings [10] or dispersive elements [9] that are not shown in the generalised model of Fig. 1. In terms of power consumption, the effect of these passive components is to simply reduce the effective wall plug efficiency of the optical source. Some may even have multiple optical sources [3, 10], which will simply increase the value of the optical power term.

The required optical source power $P_{\text{opt}}$ is set by the power required to achieve a desired SNR, given the noise limits set by shot and thermal noise for optical frequency $\nu$ and Planck constant $h$

$$P_{\text{opt}}/f_s = \frac{\text{PAPR}}{4\pi^2}\left[\underbrace{\frac{h\nu}{2} \times \text{SNR}}_{\text{shot noise}} + \underbrace{R\sqrt{C_{\text{Rx}} 8 k_B T \times \text{SNR}}}_{\text{thermal noise}}\right]. \tag{2}$$

Here, the thermal noise floor is set by the minimum optical energy to switch a capacitive load $C_{\text{Rx}}$ at the desired SNR within a single sampling period, including the photodiode junction capacitance, as shown in Fig. 1(b) [8]. The best performing photonic ADCs are usually (or designed to be) jitter limited, in which case the SNR follows the well known upper bound of $\text{SNR} = (2\pi\sigma f_{in})^{-2}$ for root-mean-square jitter $\sigma$ and input frequency $f_{in}$.

Fig. 2(a) plots the modulator energy per sample as a function of $f_s$ (assuming Nyquist rate sampling) for PAPR = 3 dB (i.e. a sine wave). Although 10 GHz/V is typical for commercially available modulators, recent results have demonstrated modulators approaching 100 GHz/V performance [12], which Fig. 2(a) shows has a potential to significantly reduce the energy per sample. Also plotted is the thermal noise limited sub-ADC power consumption in the scenario that the ADC is jitter limited: note here that energy per sample increases with improved jitter, since more accurate sub-ADC digitisation is needed to detect the higher SNR signal. On the other hand, increasing frequency for a fixed jitter decreases the power consumption as the SNR decreases. Fig. 2(b) shows how a higher SNR increases the energy per sample due to the increase in optical power needed to overcome shot and thermal

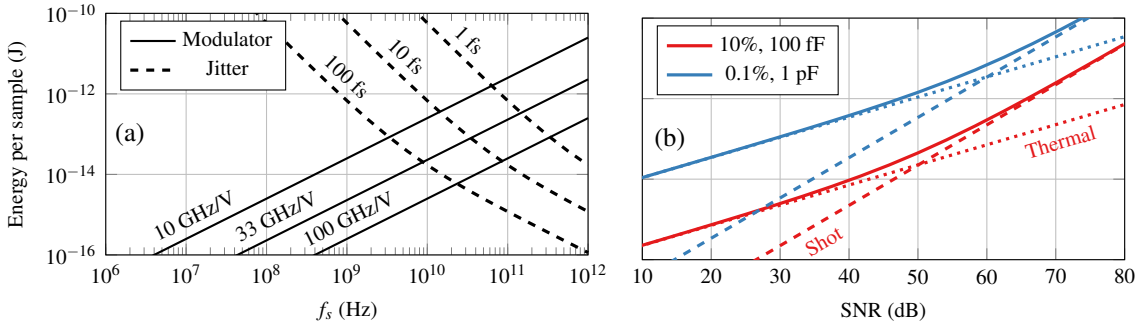
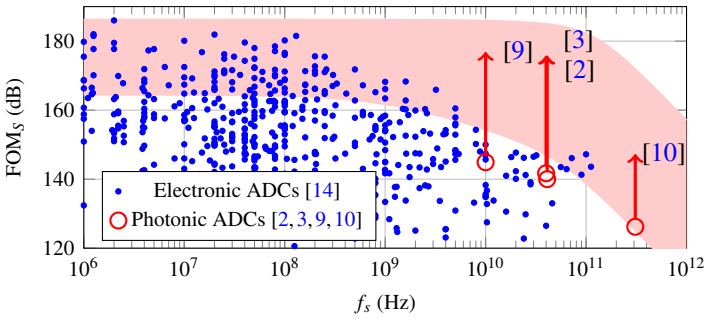



Fig. 2. (a) Modulator and jitter limited energy per sample scaling with $f_s$. (b) Optical power limited energy per sample scaling with SNR: dashed and dotted lines indicate the shot and thermal noise limits respectively for each case. For all cases in both plots: $Z_0 = 50\ \Omega$, $V_{\text{bias}} = 3$ V, $R = 1$ A/W, $\nu = 192$ THz, $T = 300$ K.




(b)

| Parameter | Worst | Best |
|---|---|---|
| $1/V_{\Delta f}$ | 10 GHz/V | 100 GHz/V |
| Jitter | 1 ps | 1 fs |
| Loss | 20 dB | 0 dB |
| PAPR | 10 dB | 3 dB |
| $Z_0$ | 50 | 50 |
| $\eta_{\text{WPE}}$ | 1% | 10% |
| $R$ | 0.5 A/W | 1.25 A/W |
| $V_{\text{bias}}$ | 3 V | 1 V |
| $C_{\text{Rx}}$ | 1 pF | 100 fF |

Fig. 3. (a) FOM$_S$ estimation for photonic ADCs (red circles) compared to published results from electronic ADCs [14]. The red shaded area indicates the achievable FOM$_S$ for generalised photonic ADCs based on (1)/(2) and the parameters in (b). The red arrows extending from the photonic ADC results indicate the maximum estimated FOM$_S$ for each architecture.

noise, as per (2). Two cases are plotted: $\{\eta_{\text{WPE}} = 0.1\ \%, C_{\text{Rx}} = 1\ \text{pF}\}$ (blue) and $\{\eta_{\text{WPE}} = 10\ \%, C_{\text{Rx}} = 100\ \text{fF}\}$ (red) with the limits imposed by shot and thermal noise indicated for each case. Clearly, shot and thermal noise limit are the dominant contributions to the energy per sample for high and low SNR respectively. Recent results have demonstrated microcomb sources with wall plug efficiencies up to 3.4% [13].

## 3. Power efficiency comparison with electronic ADCs

We also estimate a range for the achievable FOM$_S$ in Fig. 3(a). The red shaded region indicates the achievable FOM$_S$ for photonic ADCs calculated from (1)/(2) based on the best and the worst case parameters in Fig. 3(b). The blue dots are the measured FOM$_S$ from published electronic ADC results [14]. Red circles indicate the estimated FOM$_S$ for various photonic ADCs, based on the published frequency/SNR result and best estimates of the power consumption of the components used. Since these published photonic ADCs results were likely designed without regard for power consumption, we have also estimated the maximum achievable FOM$_S$ based on the minimum estimated power (using the 'best' parameters in Fig. 3(b)) required to achieve the presented result, which is indicated using an arrow for each result. While even in the best scenario our estimates for photonic ADCs FOM$_S$ barely exceeds published electronic ADC results for $f_s < 10^8$ Hz, the red shaded area in Fig. 3(a) clearly indicates that photonic ADCs may outperform their electronic ADC counterparts on an FOM$_S$ basis at higher frequencies due to their superior jitter performance.

## 4. Conclusion

We model and estimate the power consumption lower bounds of photonic ADCs and compare them with electronic ADCs for the first time. We show that photonic ADCs may outperform electronic ADCs on a FOM$_S$ basis in high ($f_s > 10^{10}$ Hz) frequency scenarios due to their superior jitter performance. Note that the results presented here are theoretical bounds, which represent the best achievable results for practical designs.

## References


1. G. C. Valley, "Photonic analog-to-digital converters," Opt. Express **15**, 1955–1982 (2007).
2. A. Khilo *et al.*, "Photonic ADC: overcoming the bottleneck of electronic jitter," Opt. Express **20**, 4454–4469 (2012).
3. C. Deakin and Z. Liu, "Frequency interleaving dual comb photonic ADC with 7 bits ENOB up to 40 GHz," in *CLEO: Science and Innovations,* (Optica Publishing Group, 2022), pp. STh5M–1.
4. B. Murmann, "A/D converter trends: Power dissipation, scaling and digitally assisted architectures," in *2008 IEEE Custom Integrated Circuits Conference,* (IEEE, 2008), pp. 105–112.
5. B. Razavi, "Design considerations for interleaved ADCs," IEEE J. Solid-State Circuits **48**, 1806–1817 (2013).
6. R. S. Tucker, "Green optical communications—Part I: Energy limitations in transport," IEEE J. Sel. Top. Q. Elec. **17**, 245–260 (2010).
7. S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters* (IEEE Press, 2017).
8. D. A. Miller, "Attojoule optoelectronics for low-energy information processing and communications," J. Light. T. **35**, 346–396 (2017).
9. S. Gupta and B. Jalali, "Time-warp correction and calibration in photonic time-stretch analog-to-digital converter," Opt. Lett. **33**, 2674–2676 (2008).
10. D. Fang *et al.*, "320 GHz analog-to-digital converter exploiting kerr soliton combs and photonic-electronic spectral stitching," in *2021 European Conference on Optical Communication (ECOC),* (IEEE, 2021), pp. Th3C1–PD2.2.
11. T. Clark, M. Currie, and P. Matthews, "Digitally linearized wide-band photonic link," J. Light. T. **19**, 172–179 (2001).
12. C. Wang *et al.*, "Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages," Nature **562**, 101–104 (2018).
13. B. Stern *et al.*, "Battery-operated integrated frequency comb generator," Nature **562**, 401–405 (2018).
14. B. Murmann, "ADC performance survey 1997-2022," http://web.stanford.edu/~murmann/adcsurvey. [Online].