Beyond 200-GBd QAM Signal Detection Based on Trellis-path-limited Sequence Estimation Supporting Soft-decision Forward Error Correction

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Abstract: We proposed and experimentally demonstrated a trellis-path-limited sequence estimation method combining the log-likelihood ratio from minimum-mean-square-error equalizer-enabled signal detection with soft-decision -FEC decoding under severe bandwidth limitations, achieving 1.35-Tb/s 256-GBd 16QAM and 1.65-Tb/s 208-GBd 64QAM. © 2023 The Author(s)

1. Introduction

Digital coherent transceivers with a high-symbol rate and multi-level quadrature amplitude modulation (QAM) signals are necessary for the next-generation large-capacity optical transport networks to accommodate exponentially increased internet traffic. Thanks to ultra-wideband analog frontend devices and sophisticated digital signal processing (DSP), a capacity per wavelength are dramatically increasing. A net bitrate of >2-Tb/s 176-GBd probabilistically constellation-shaped (PCS)-144QAM signal transmission was achieved by using an ultra-wideband indium phosphide (InP) double-heterojunction bipolar transistor (DHBT) electrical amplifier module with an~80-GHz bandwidth (BW) arbitrary waveform generator (AWG) [1]. To further improve the capacity per wavelength, increasing the symbol rate is essential. Figure 1 shows the results of previous digital coherent experiments of a symbol rate over 200 GBd [1-4]. BW enhancement of the transceiver at such ultra-high symbol rate is challenging since severe bandwidth limitations degrade the signal quality.

Maximum likelihood sequence estimation (MLSE) is promising for detecting the symbols at severe BW limitations for hard-decision (HD) forward error correction (FEC) [5]. To support soft-decision FEC (SD-FEC), which is generally used in a digital coherent transceiver, maximum a-priori (MAP) sequence estimation based on Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm [6] is required to calculate the log-likelihood ratio (LLR). Faster than Nyquist 220-GBd 692-Gb/s quadrature phase-shift keying (QPSK) was also demonstrated by digital coherent transceiver with sequence estimation [4]. For multilevel signals, the number of states increases exponentially with memory length with this algorithm. A scheme to reduce the number of states was proposed for intensity-modulation and direct-detection and digital coherent transceivers [7, 8]. However, the performance of SD-FEC decoding degrades with a small number of states due to the infinite LLR [8]. Therefore, a sequence-estimation supporting the SD-FEC that does not cause performance degradation is necessary even when the number of states is small.

We propose a trellis-path-limited sequence-estimation method combining the bit-wise LLR from a minimum-mean-square-error (MMSE) equalizer for high-symbol rate QAM signals. The proposed method results in no performance degradation in SD-FEC decoding even when the number of candidate state is small due to combining the bit-wise LLRs calculated from MMSE equalized symbol and symbol-wise LLR calculated from trellises-path-limited sequence estimation. We also demonstrated 1.35-Tb/s net-bitrate 256-GBd 16QAM and 1.65-Tb/s net-bitrate 208-GBd 64QAM signal decoding by using the proposed method.

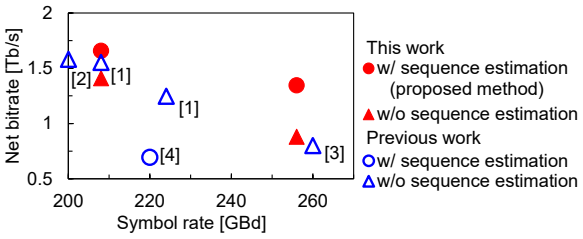

Fig. 1. Results of digital coherent experiments with symbol rate over 200 GBd.

2. SD-FEC Supported Trellis-path-limited Sequence Estimation

Figure 2(a) shows a block diagram of the proposed method. The method combines the bit-wise LLR $L_i(k)$ and candidate symbol-wise LLR $\lambda_j(k)$ from trellis-path-limited sequence estimation, where $i, j, and\ k$ denote bit-level, candidate symbol index, and time index, respectively. The $L_i(k)$ is the same as a conventional bit-wise LLR without sequence estimation because $L_i(k)$ is calculated from a recovered symbol $r(k)$ output from an adaptive equalization

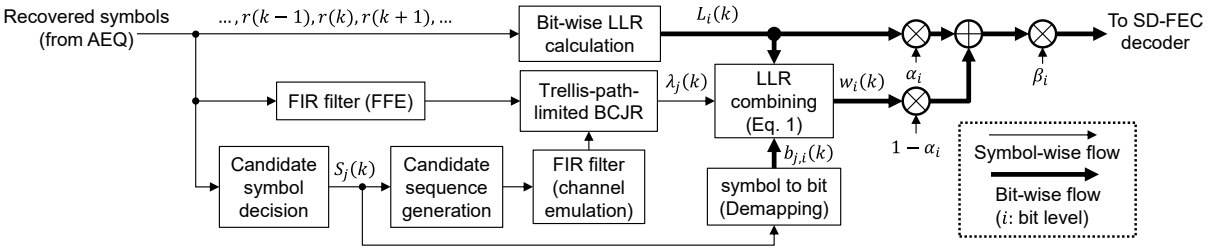

Fig. 2. Block diagram of proposed SD-FEC supported Trellis-path-limited sequence estimation for multi-level modulation format.

(AEQ) based on MMSE equalization. Thus, the $L_i(k)$ is able to be easily implemented by simple approximated calculation or a look-up table. The $\lambda_j(k)$ is calculated by candidate symbol sequence on the basis of tentative decision and the trellis-path-limited BCJR algorithm. The candidate symbol is determined by the Euclidian distance between $r(k)$ and replicas in each time index k. The candidate symbols $s_j(k)$ are assigned the candidate symbol index j in order of proximity from $r(k)$, where the maximum number of $s_j(k)$ is M. The candidate sequences with memory length N are then generated using $s_j(k)$. Finite-impulse response (FIR) filters for a feed forward equalizer to whiten the noise contained in $r(k)$ and channel emulation filter for the candidate sequences are used. Therefore, the number of states in the BCJR algorithm is M^{N-1}, which can reduce the trellis-path by decreasing M. The BCJR algorithm calculates $\lambda_j(k)$ among the candidate symbols, where the max-log-MAP algorithm is used instead of the probability-domain BCJR algorithm to reduce computational complexity. The combining of the $L_i(k)$ and $\lambda_j(k)$ is the important in the proposed method. The $L_i(k)$ of the i_{th} bit-level corresponds to subtraction of $\lambda_j(k)$ where the i_{th} bit is zero for $s_j(k)$ and that where the i_{th} bit is one. Therefore, $b_{j,i}(k)$ corresponding to $s_j(k)$ are used for the selection of both the bit-level reflecting the bit-wise LLR derived from $\lambda_j(k)$ and sign of the LLR. If $b_{j,i}(k)$ corresponding to the i_{th} bit-level are all the same, the $L_i(k)$ is selected as the i_{th} bit-level combined bit-wise LLR $w_i(k)$. The LLR-combining equation is written as

$$w_i(k) = \sum_{m=1}^{M-1} \prod_{j=1}^{m} \{1 - |b_{1,i}(k) - b_{j,i}(k)|\} \{b_{m+1,i}(k) - b_{1,i}(k)\} \{\lambda_1(k) - \lambda_{m+1}(k)\} + \prod_{j=1}^{M} \{1 - |b_{1,i}(k) - b_{j,i}(k)|\} L_i(k). \quad (1)$$

The $w_i(k)$ and the original $L_i(k)$ are calculated by weighted addition with a constant coefficient α_i. By optimizing α_i at each condition, a lower bound of the performance is guaranteed for $L_i(k)$ even when the number of candidate states is small. Finally, the normalization coefficient β_i is multiplied to be normalized for the for SD-FEC decoding.

3. Experiments for Beyond 200-GBd QAM Signal Demodulation

Figure 3 shows the experimental setup for the performance evaluation of proposed method for beyond 200-GBd QAM signal. The configurations of the transmitter (Tx) and receiver (Rx) were the same as those for the >2-Tb/s signal transmission [1]. At the Tx-DSP, 256-GBd uniform 16QAM and 208-GBd uniform 64QAM signals with symbol length of 2.62×10^5 and 8.51×10^5 including 0.7874% QPSK pilot symbol were generated. The symbols were upsampled by using a root-raised-cosine filter with a roll-off factor of 0.1. Then linear pre-emphasis filter was used to compensate for the frequency response of the AWG and electrical amplifier. The high-speed radio frequency signal generated from the AWG with ~80-GHz BW and InP DHBT amplifier module with 110-GHz BW [9] applied to the lithium-niobate (LN) in-phase-and-quadrature modulator (LN-IQM) with 35-GHz BW. A carrier signal was fed using a ~10-kHz linewidth (LW) laser diode (LD) amplified using an erbium-doped fibre amplifier (EDFA). Polarization division multiplexing (PDM) was emulated using a 35-m delay line (175-ns delay) and variable optical attenuator. An

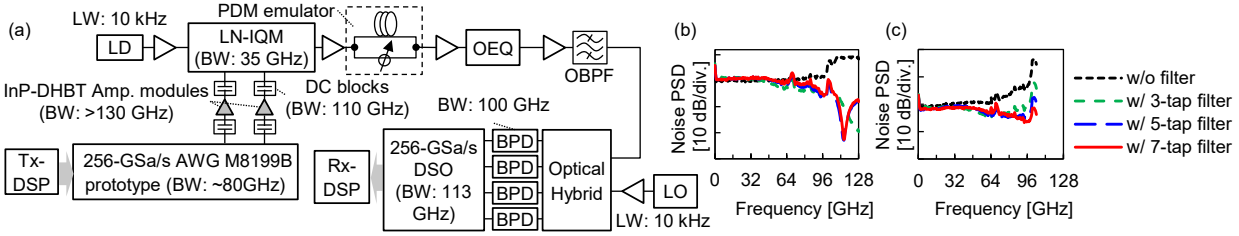

Fig. 3. (a) Experimental setup for beyond 200 GBaud QAM signal demodulation. Noise power spectrum density of (b) 256-GBd 16QAM and (c) 208-GBd 64QAM signal.

optical equalization (OEQ) compensated for the frequency response of the LN-IQM. After an optical bandpass filter (OBPF), the signals were detected using a coherent receiver composed of an optical hybrid, local oscillator (LO), and balanced photo detectors (BPDs). A 256-GSa/s digital storage oscilloscope (DSO) digitized the received signal. The Rx-DSP simultaneously compensated for the linear responses in the Tx and Rx, frequency offset compensation, and carrier phase recovery using a frequency domain 8×2 multi-input and multi-output (MIMO) AEQ [10] with a pilot-based digital phase-locked loop using pilot QPSK symbol every 128 symbol deration. After decomposing recovered PDM complex-IQ symbols to real valued four lane signals, the recovered symbols were fed into the demodulation block of the proposed method for each lane. The coefficients of both the feed forward equalizer and channel emulation filters at the proposed method were updated by using the recursive least square (RLS) algorithm [5]. Figures 3 (b) and (c) show the noise power-spectrum-density (PSD) with and without the filters for 256-GBd 16QAM and 208-GBd 64QAM signals. We found the noise enhancement suppression with the filters at the high frequency region.

Figure 4 (a) shows the normalized generalized mutual information rate (NGMI) as a function of memory length N for the 256-GBd 16QAM signal. The proposed method, when $M = 3$, performance well with small NGMI degradation compared with conventional full state BCJR algorithm without trellis-path limitation. When the memory length was five, the state number of the trellis decreased from 256 ($= 4^{5-1}$) to 81 ($= 3^{5-1}$), although the 0.01 NGMI decreased compared with that the conventional method. The improvement of NGMI without sequence estimation (see N = 1) was 0.22 when M=3 and N=7. Figure 4 (b) shows NGMI versus memory length for the 208-GBd uniform 64QAM signals. The proposed method was able to improve NGMI at an even high order modulation format. The NGMI improvement without sequence estimation (see N = 1) was 0.06 when M=3 and N=7. Finally, we evaluated the decoding performance of low-density parity check (LDPC) codes using the offline evaluation scheme [11]. We used a family of DVB-S2 LDPC codes [12] with a puncturing method [11] to determine the required code rate for error-free decoding assuming the outer HD-FEC with the code rate of 0.9922 and bit error rate (BER) threshold of 5×10^{-5} [13]. Figure 4 (c) shows the post-LDPC BER as a function of the LDPC overhead. We examined over 7.76×10^5 bits for LDPC decoding. We confirm that the required LDPC overhead for error-free decoding decreased when using the proposed method. The net bitrate of the 256-GBd 16QAM signal with and without the proposed demodulation were 0.88 and 1.35 Tb/s (total code rates were 0.4334 and 0.6688), respectively. The net bitrate of 208-GBd 64QAM with and without the proposed method were 1.40 and 1.65 Tb/s (total code rates were 0.5687 and 0.6688), respectively. The proposed method achieved 1.35-Tb/s 256-GBd 16QAM and 1.65-Tb/s 208-GBd 64QAM after LDPC decoding.

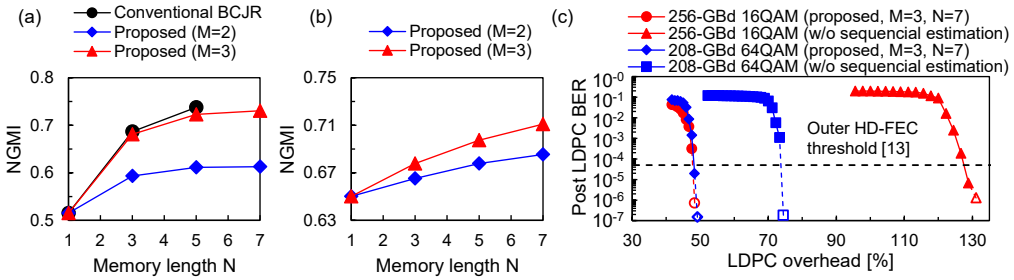

Fig. 4. Experimental results of memory length dependencies on NGMI for (a) 256-GBd 16QAM and (b) 208-GBd 64QAM signals, and (c) Post LDPC BER versus LDPC overhead for with and without proposed demodulation.

4. Conclusion

We proposed a trellis-path-limited-sequence-estimation method SD-FEC based on the combination of the bit-wise LLR calculated from MMSE equalized symbol for high-symbol rate QAM signals. We also evaluated the proposed method for beyond 200 GBd QAM signals based on 130-GHz BW ultra-wideband InP-DHBT amplifier with 80-GHz-BW AWG. Then, the proposed method achieved 1.35-Tb/s 256-GBd 16QAM and 1.65-Tb/s 208-GBd 64QAM after LDPC code decoding.

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References

[1] M. Nakamura, *et al*., ECOC2022PDP, Th3C.1.
[2] X. Chen, *et al*., OFC2021PDP, F3C.5.
[3] F. Pittalà, *et al*., ECOC2020PDP, Th3A.3.
[4] H. Mardoyn, *et al*., ECOC2022PDP, Th3C.2.
[5] H. Taniguchi *et al*., ECOC2022, We2D.1
[6] L.Bahl, *et al*., IEEE Trans. Inf. Theory, IT-20(2), 284, 1974.
[7] D. Che *et al*., ECOC2021, Th3C2-PD1.6
[8] D. Che *et al*., OFC2022, Th2A.33
[9] T. Jyo, *et al*., IEEE BCICTS2021 1b1.1
[10] M. Nakamura, *et al*., OFC2022, M3H.1
[11] T. Yoshida, *et al*., OFC2018, M4E.5.
[12] ETSI, EN 302 307-1, v.1.4.1, 2014.
[13] D. S. Millar, *et al*., J. Lightw. Technol., 34 (6), 1453 (2016).