Hitless Transmission Baud Rate Switching in a Real-Time Transponder Assisted by an Auto-Negotiation Protocol

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Abstract: We propose a novel coherent receiver architecture that allows an instantaneous and hitless variable baud rate transmission. This solution is demonstrated in a real-time experiment. We also show how the baud rate variation can leverage an in-line auto-negotiation protocol.

1. Introduction

For Elastic Optical Network (EON), it is of prime importance to have fast and easy reconfigurable elements available capable to react quickly to a network health or operation change, assisted by intelligent monitoring capability, ideally without any traffic interruption. Today, some commercial transponders are already able to change their modulation format and/or symbol rate operation, but an interruption of traffic due to long reconfiguration time is still inevitable. In a field trial with commercial transponders, a ~35 seconds duration was demonstrated to switch from 100 Gbit/s to 200 Gbit/s [1]. In [2], a FPGA-based real-time transmitter prototype was shown with baud rate switching time lower than an OTU4 frame duration. Recent works focus on autonomous transponders where distributed decisions are made at the receiver side to react faster to network conditions [3-4]. The communication between two transponders is proposed in [4] with an auto-negotiation protocol. At the receiver side, to the authors' knowledge, no hitless architecture has been proposed for baud rate switching. Indeed, to accommodate a lower baud rate, one would need to adapt the receiver i) by lowering the Analogue to Digital Converter (ADC) sampling frequency to feed the Digital Signal Processing (DSP) with two samples/symbol (SPS) and also the DSP processing frequency to adapt to the reduction of data flow to be processed, or ii) by keeping the ADC sampling frequency and then inserting at the beginning of the DSP a decimation or averaging function to continue feeding the DSP with 2 SPS data, which still implies reducing the DSP frequency. Changing the operating frequency forces the inner functions and components of receivers to be reset for a new initialization procedure. For example, the high-speed serial interfaces between ADC and DSP logic may need several hundreds of µs to accommodate a new frequency. Also, coherent receiver DSPs use algorithms which needs time to converge to find a new operating point. During these periods, the receiver becomes unavailable to process the incoming signal leading to a traffic interruption.

In this paper, we propose a novel architecture for the DSP offering hitless baud rate switching, and we demonstrate its performance with a complete experimental setup including flexible and real-time transmitter and receiver. We also show how the symbol rate adaptation automation can be leveraged with an assisting auto-negotiation protocol.

2. Real-time receiver with hitless baud rate switching

A coherent transmission receiver is composed of an optical mixer followed by a set of four photodiodes, four ADC cores for the electrical sampling of the successive T-length symbols and finally a DSP unit that recovers the emitted bits. After a signal clock recovery and channel pre-compensation, DSPs generally include an adaptive T/2 spaced filter function using a blind Constant Modulus Algorithm (FIR-CMA) for polarization demultiplexing and channel equalization, a Carrier Frequency Estimator (CFE), a Carrier Phase Estimator (CPE) and a symbol de-mapper and Forward Error Corrector (FEC) [5]. In this paper, we neglect the FEC block without loss of generality and we assume a usual 2 SPS input data flow. In high-speed transponders, each of the DSP functions must be processed using parallelism due to frequency limitation constraint. In particular, the usual FIR-CMA is decomposed (see Fig. 1(a)) in N-parallelized FIR-CMAs, where N is the number of consecutive symbols processed at once. All N-FIR-CMAs include the same common four M-taps filters set whose coefficients are updated one time per N symbols by a single error function computed with one of these N symbols.

To accommodate hitless rate switching, it is important to keep the DSP chain unchanged as well as its operating frequency. To this end, it is of interest to select a new baud rate being a submultiple of the highest supported baud rate. When the baud rate is divided by two, each symbol becomes sampled 4 times and is then processed by two consecutive FIR- CMAs with the same tap multiplier values. We denote by 'S_k-left' (respectively 'S_k-right') the first two samples (resp. the 3rd and 4th samples) of the k^{th} symbol. We simulated this configuration with 4 SPS data numerically generated from Dual-Polarization Quaternary Phase Shift Keying (DP-QPSK) experimental data sampled with a high-sampling rate oscilloscope after a front-end coherent receiver, and also with simple emulated 4SPS QPSK data. The DSP results are illustrated in Fig. 1(a): in case of 4 SPS data processed by a usual FIR-CMA architecture, only the 4 QPSK phases of the Sk-left are correctly recovered whereas the Sk-right appear with many additional intermediate levels.

We therefore propose a new DSP architecture capable of operating in two different baud rates leveraging a novel FIR-CMA architecture, while the rest of the DSP processing remains unchanged. More generally, this architecture relies on interleaving of B independent sets of FIR-CMAs able to process any symbol rate divided by B. This arrangement is shown in Fig. 1(b) for B = 2, where the blue set of FIR- CMAs is used for recovering 'S_k-left' and the yellow one for 'S_k-right'. We observe in Fig. 1(b) the simulated results with the same data set as used in Fig. 1(a) where the 4 phases of both 'S_k-left' and 'S_k-right' are now well recovered. This FIR-CMA architecture has been implemented in a real-time coherent receiver prototype for experimental validations.

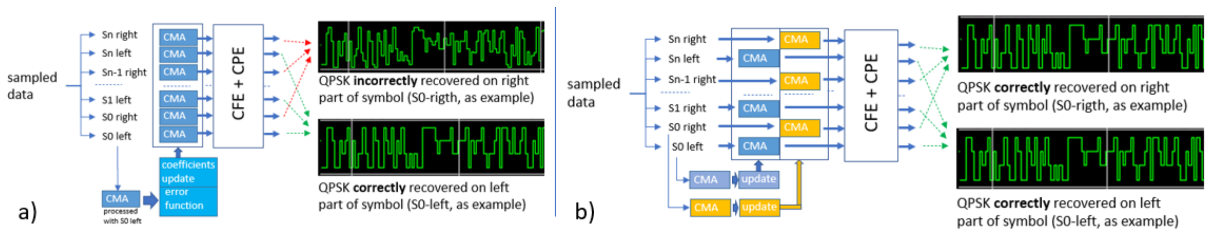


Fig. 1. Comparison of FIR-CMA architectures used at 4SPS: (a) Usual architecture: QPSK pattern recovered correctly only for Sk-left symbol, (b): Proposed architecture: QPSK patterns are recovered correctly for all Sk-left and Sk-rigth symbols.

3. Experimental test and application with an auto-negotiation protocol

The real-time experiment (Fig. 2) aims to demonstrate the implementation feasibility of the adapted DSP to hitless baud rate change and to characterize the dynamic response of the receiver after the baud rate switching. Also, we show an application leveraging an auto-negotiation protocol [4].

The transmitter [2] uses a Xilinx Virtex 7 FPGA in which embedded ROM store frames consisting of a 64-bits header and 127x64 bits Pseudo-Random Binary Sequence (PRBS) at 7 and 14 GBd at respectively 2 and 1 SPS. Four high-speed FPGA transceivers serialize these data, and are used to create an optical DP-QPSK signal up to 56 Gb/s. The receiver prototype includes a 28 GSa/s-8bits-4cores ADC interconnected through 96 x 11.3 Gb/s lanes with a Virtex-7 FPGA hosting the coherent receiver DSP with the proposed interleaved FIR-CMA architecture. The real-time DP-QPSK decoded bit sequences are sent to a FPGA-based extension board for frame processing.

The rate change is triggered by a bidirectional and inline auto-negotiation protocol which synchronizes both the transmitter and the receiver. This protocol relies on short messages inserted in the header of frames in the transmitter and receiver. An alert signal informs the transmitter that the rate must be adapted upon the detection of soft failures like frequency shift or frequency tightening that can be identified by features available at the receiver DSP [6]. Once the alert message is received, the transmitter sends a request message to the receiver to check if the change can occur and, if it is possible, in how many frames. When ready, the receiver returns an acknowledge message with the waiting duration. When received, the transmitter waits for this delay, then activates the new baud rate.

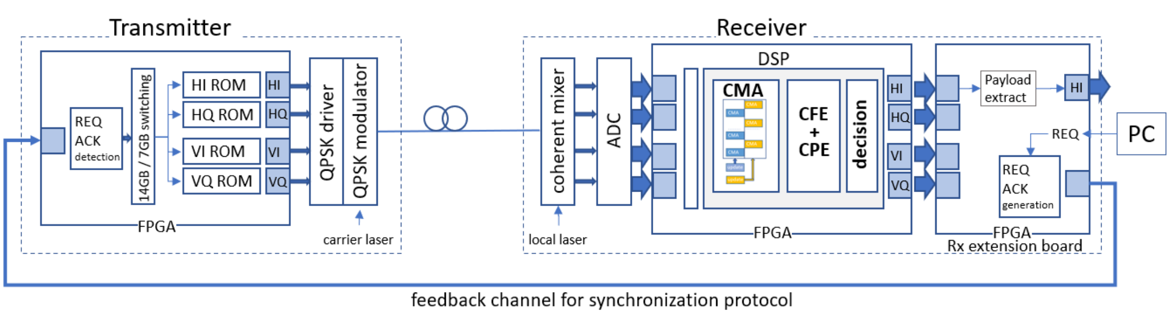


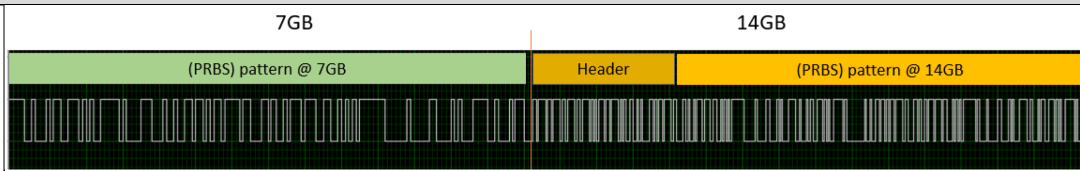
Fig. 2. Experimental setup for variable baud rate transmission with an auto-negotiation protocol.

4. Experimental results

We start from a steady-state 7GBd optical transmission at high optical signal-to-noise ratio in quasi back-to-back configuration keeping the reception bit error ratio (BER) below 1E-9 to be able to detect potential error due to the receiver reaction to the symbol rate switching. The described protocol is then activated to switch to 14 GBd. The transmitter immediately switches to 14 GBd after the end of a 7 GBd frame. Once the header of the first 14 GBd frame is detected inside the receiver, we trigger an integrated logic analyzer (ILA) implemented inside the receiver FPGA to download 32768 consecutive decoded bits captured around the baud rate switching event, for a detailed bit by bit analysis. The results are shown in Fig. 3 where the "TX" line details the two last 32b words of the 7GBd transmitted sequence, followed by the header and the two first 32-bits words of the following 14 GBd frame. In the "RX" line we reconstructed the serial bit sequence showing the transition to the doubled baud rate regime, and the corresponding two first 32-bits word received sequence. This shows the exact matching of the transmitted and received sequence without any loss all along the baud rate switching operation.

	7GBd transmission		14GBd transmission
TX	x0F3030FF - x03300F0	64b-Header	x081FD533 - xBA58DED6

RX



RX	x0F3030FF - x03300F0	64b-Header	x081FD533 - xBA58DED6

Fig. 3. TX): left/right: last/first four 32b-word sequence sent by the Tx before/after the baud rate switching, RX): decoded bit sequence, captured during the baud rate switching, under is the corresponding 32b-word received sequence

Also, we compared the received first 32x697 bits of the 14 GBd PRBS payload with a calculated PRBS sequence and no bit error was detected. This demonstrates that the proposed DSP offers a perfect hitless reception of the transmitted signal, meaning without any interruption nor any error insertion, while experiencing a sudden baud rate switching forced by the transmitter.

In Fig. 4, we observe inside of the transmitter the messages exchanged with the receiver during the auto-negotiation protocol. An 'alert' message is first received, then an acknowledge returned by the receiver is captured and the new baud rate is activated after two frames keeping frame integrity.

Fig. 4: Protocol messages captured in an ILA at the transmitter side

5. Conclusion

We proposed an interleaved architecture for the FIR-CMA function of coherent receiver DSP that we demonstrate to be able to operate an optical signal with a symbol rate being a submultiple of its nominal one. With this solution, we demonstrate that a sudden change of baud rate transmission is processed hitlessly, without any data loss nor bit error insertion. Although tests were performed only with a baud rate division by two, we believe that any integer subdivision of the FIR-CMA parallelization number can be used. Even if less flexible than a current approach using different sampling and DSP frequencies, this solution allows a continuity of traffic for EON. Also, we showed that the baud rate reconfiguration can be negotiated and executed at several µsec-scale using an SDN compatible inline auto-negotiation protocol.

6. References

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