Broadband, Low-Crosstalk and Power-Efficient 32×32 Optical Switch on a Dual-Layer Si_3N_4-on-SOI Platform

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Abstract: We demonstrate a 32×32 optical switch on a dual-layer Si_3N_4-on-SOI platform with low fiber-to-fiber insertion loss (9.61~14.51 dB), low crosstalk (~-35 dB), broad 3-dB bandwidth (~57 nm) and low power consumption (~0.83 W). © 2022 The Author(s)

1. Introduction

With numerous new applications such as cloud computing, Internet of things, and multimedia streaming bursting out, optical switching is considered as a promising candidate to satisfy the ever-growing demand of data traffic in the datacenters due to the merits of large-bandwidth, power-efficiency, and low-latency [1]. Large-scale, low-cost, and power-saving optical switch fabrics are essential in the optical switching networks. Recently, several optical switch fabrics on the silicon photonics platform have been demonstrated, which inherit the features of compact size and complementary metal-oxide-semiconductor (CMOS) compatibility [2-4]. The highest radix of proposed silicon optical switch fabric has reached 240×240 based on the micro-electro-mechanical-system (MEMS) technology [5]. However, it cannot be provided by the standard silicon photonic foundries. Instead, silicon optical switches based on Mach-Zehnder interferometers (MZIs) have been extensively studied by several groups [6-9]. Various 32×32 silicon MZI optical switch fabrics have been demonstrated with the path-independent insertion-loss (PILOSS) [6-7], Benes [8], and dilated-Benes [9] architectures. Among them, the PILOSS switch fabrics have shown the lowest fiber-to-fiber insertion loss along with a small path-dependent insertion loss. However, the unsuppressed 1st-order crosstalk degrades the switch performance.

In this work, we demonstrate a 32×32 broadband optical switch fabric based on a switch-and-select (S&S) topology. The S&S structure is known as a strictly non-blocking switching topology with totally suppressed 1st-order crosstalk. However, large numbers of in-path waveguide crossings severely degrade path-dependent insertion loss. Here, leveraging a dual-layer Si_3N_4-on-SOI platform, we realize a 32×32 MZI switch chip with low path-dependent insertion loss, low crosstalk, and low power consumption.

2. 32×32 Optical Switch Chip

Figure 1(a) depicts the structure of the 32×32 switch fabric. It contains thirty-two 1×32 optical switch arrays at the both input and output stages, connected by a passive waveguide-crossing network. Each 1×32 optical switch is composed of thirty-one 1×2 MZI silicon switch elements arranged in a binary-tree. Thus, there are totally 1984 MZI-switches in the fabric, and each optical routing path contains 10 MZI switches. The 1×2 MZI switches are based on thermo-optic (TO) effect with a TiN microheater imbedded in one of the MZI arms in each. To further decrease the power consumption, deep trenches with undercut structures are designed around the TO phase shifters, as is shown in Fig. 1(b). For the 32×32 S&S switch, there are at least 0 and at most 961 (31^2) waveguide-crossings in the routing paths. Typical planar silicon waveguide crossings with an insertion loss of ~ 0.05 dB would introduce around 50 dB extra loss, which dramatically degrades the switch performance. Instead, the passive waveguide-crossing network is constructed by 1024 silicon and top-layer Si_3N_4 waveguides vertically crossing to form thousands of interlayer waveguide crossings. Figure 1(d) shows the structure of the interlayer waveguide-crossings. The top-layer Si_3N_4 waveguide is separated by 850 nm with the silicon ridge waveguides to achieve ultra-low crossing loss. However, it would cause large transition loss when light transmitted between these two waveguides. Therefore, a middle-layer Si_3N_4 waveguide is introduced as shown in Fig. 1(e). Two interlayer waveguide-couplers for the silicon to middle-layer Si_3N_4 waveguide connection, and the middle-layer to top-layer Si_3N_4 waveguide connection are designed based on linear tapered structures.

The chip was fabricated by Advanced Micro Foundry (AMF). Figure 1(c) shows the fabricated switch chip with a footprint of 18 mm × 24 mm. Spot-size converters with suspended structures were used for efficient coupling with standard single-mode fibers (SMFs) [10]. Figure 1(f) shows the packaged chip. The high-density electrodes were firstly fanned out to an organic interposer by wire-bonding, and then mounted to a low-density printed circuit board (PCB) via ball gate arrays (BGAs). A pair of polarization maintaining fiber arrays (PM-FAs) was used to couple the light in/out of the chip. UV-curable glue was used to attach the PM-FAs. As the index-matched oil was not used, the estimated coupling loss is ~2.8 dB/facet. The entire packaging was finished by SJTU-Pinghu Institute of Intelligent Optoelectronics. Figure 1(g) shows the driver boards for the switch fabric, which can generate 1984 electrical pulse-width-modulation (PWM) signals (4.7-V amplitude, 1 MHz repetition). The switching states were automatically calibrated by maximizing the output power of each routing path by a one-dimensional optimization algorithm. It takes less than 3 minutes for each path without on-chip detectors, limited by the sampling rates of the power meters and the communication speed of the serial interfaces.

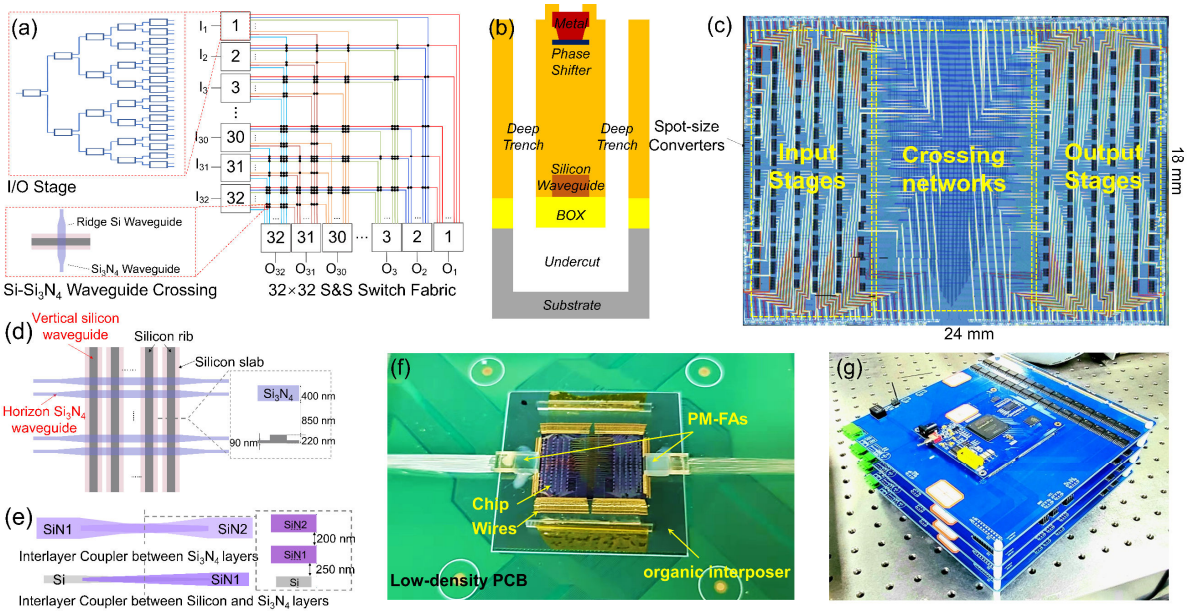

Fig. 1 (a) Schematic of the 32×32 S&S switch fabric. (b) Cross-section of phase shifter and waveguide. (c) Fabricated switch chip. (d) Structure of the passive waveguide-crossing network. (e) Structure of the interlayer couplers. (f) Photo of the packaged chip. (g) PWM signal driver boards.

3. Experiment Results

We first measured the characteristics of the passive devices. The insertion loss of single waveguide crossing with light transmitting in the bottom silicon and the top Si_3N_4 waveguide is 5.5 mdB and 4.6 mdB at 1580 nm, respectively. The transition loss when light transfers from the bottom silicon waveguide to the top Si_3N_4 waveguide is 0.133 dB at 1580 nm. Higher loss at 1520 nm wavelength is due to the residual absorption from the N-H bonds. We also characterize the 1×2 MZI element, which shows the insertion loss of ~0.3 dB and the extinction ratio ~22.5 dB at 1580 nm.

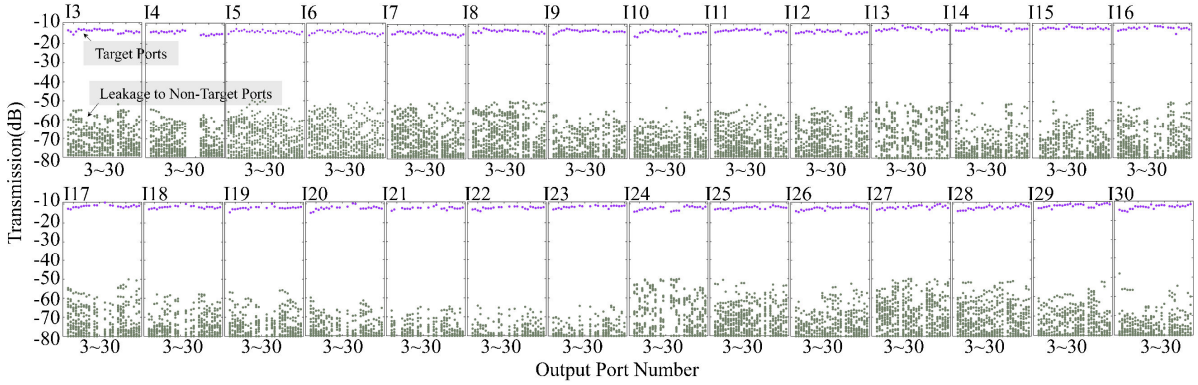

Fig. 2. Measured transmission for all routing paths and leakages to the non-target ports at 1580 nm.

Due to the mask layout mistakes, the spot-size converter intersects with a bending waveguide at four input (output) ports (#1, #2, #31 and #32), which induces extra loss and deteriorates extinction ratio. Besides, several MZI elements cannot be driven because of broken gold-wires or damaged interfaces of PWM-driven boards. Therefore, we just present the measured results from the rest working paths. Figure 2 shows the measured output transmission and leaked power when the routing paths are established at 1580 nm. In these measured paths, the maximum and minimum numbers of the in-path waveguide crossings are 92 and 616. The fiber-to-fiber insertion loss ranges from 9.61 dB to 14.51 dB, with an average of 11.76 dB. The worst loss is from path I_{30}-O_3, which can break down as ~3.6-dB from 10 MZIs, ~3.11 dB from 616 waveguide-crossings, ~0.26 dB from 2 interlayer couplers, ~5.6-dB from fiber-chip coupling, and ~1.94 dB from connecting waveguides. Relatively larger loss variation than expected may come from the difference in the coupling. The crosstalk is less than -35 dB.

Figure 3(a) presents the measured spectra when input ports #7 are routed to all the 28 output ports. At 1580 nm, the insertion loss varies from 10.94 dB to 13.94 dB and the crosstalk is less than -39.45 dB. The average 3-dB optical bandwidth reaches 57 nm. Figure 3(b) shows the power consumption for establishing each routing path of the switch. The average power of single path including 10 MZIs is 26.03 mW. Thus, the total power consumption is ~0.83 W when the entire chip is working. The rise and fall time of the switching temporal response is 374.7 μs and 348 μs, as shown in Fig. 3(c).

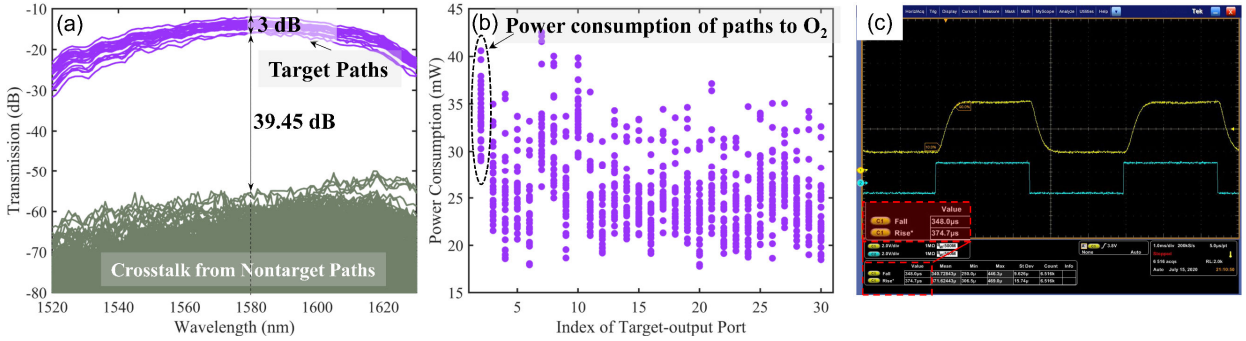

Fig. 3. (a) Transmission spectra of all paths from in ports #7. (b) Power consumption for each routing path. (c) Response-time of the switch chip.

4. Conclusion

We have demonstrated a 32×32 MZI-based S&S optical switch fabric on the dual-layer Si_3N_4-on-SOI platform. Benefits from the ultralow loss interlayer waveguide crossings, the switch shows a low average fiber-to-fiber insertion loss of 11.76 dB, with a loss variation of 4.9 dB for all the measured paths. Besides, the crosstalk is lower than -35 dB, the 3-dB optical bandwidth is 57 nm, and the total power consumption is ~0.83 W. This optical switch chip exhibits excellent performance and has the potential to be applied in the next generation optical switching networks.

5. References

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