Path-Independent Insertion-Loss (PILOSS) 8 × 8 Silicon Photonics Switch with <8 nsec Switching Time

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Abstract: We demonstrate strictly non-blocking and 8 × 8 silicon photonics switch with 10-90% switching time of <8 nsec, on-chip loss of 3.8±0.19 dB independent of path settings, and 20-dB crosstalk bandwidth of ~30 nm. © 2022 The Author(s)

1. Background

Optical switches are considered to play important roles in next-generation datacenter networks in which high-bandwidth communications between a large number of nodes are required. Fully disaggregated datacenters, in which hardware such as CPU and memory are dynamically allocated, would require switches with not only high bandwidth transmission but also fast reconfiguration time to reduce the latency [1]. By considering the future latency requirement of <100 nsec [1] and receiver's phase-locking time of 2.6 to 18.5 nsec [2,3], the requirement of the response time for the future optical switches would range from ~nsec to several tens of nsec. Silicon (Si) photonics-based Electro-optic (EO) switches would be one of the most suitable candidates to realize such high-speed and high-radix optical switches, because they have an ultra-small footprint and mass productivity by utilizing a CMOS process line, and high reliability. Previous demonstrations of Si EO optical switches have employed Beneš [4] or Double-Layer Network (DLN) topology [5]. However, there is a disadvantage in the Beneš topology because it is rearrangeably non-blocking, *i.e.*, all connections must be shut down when assigning a new path. This would cause increased latency for phase locking. Moreover, the above two topologies have "path-dependent" insertion loss because the number of "ON" Mach-Zehnder Interferometers (MZIs), or "lossy" MZIs, differs between paths. This causes non-uniform transmission power, making it difficult to secure the link power budget. Here, we propose to utilize path-independent insertion-loss (PILOSS) topology [6] for Si EO optical switches. This topology is strictly non-blocking in which connections live when assigning a new path. Moreover, the topology, when used with EO MZIs, has exactly the same number (one) of "ON" MZI, leading to constant insertion loss regardless of the path settings. Low-loss characteristic is also expected because there is only one "ON" (lossy) MZI on a path.

In this paper, we demonstrate 8 × 8 PILOSS silicon photonics switch using both EO and Thermo-optic (TO) phase shifters. We used TO phase shifters to trim out initial phase errors so that no excess losses are induced. We then used EO phase shifters to switch the light with a fast 10-90% rising time of <8 nsec. The on-chip insertion loss (IL) was 3.8 ± 0.19 dB for all paths. We consider that the fluctuations in the ILs were caused by chip-to-fiber coupling, which can be reduced by flattening the chip edge.

2. Chip design and fabrication

Figure 1(a) shows the schematic of the fabricated PILOSS 8 × 8 Si EO switch. We integrated 8 × 8 = 64 MZIs on a chip. In each MZI, we have two EO phase shifters based on a lateral p-i-n junction on a rib-type waveguide and two TO phase shifters based on a thin TiN heater on top of a channel-type waveguide, on each arm. The optical transition between these two types of waveguides was done by using an adiabatic taper structure. The EO phase shifters are used to switch the MZI states and the TO phase shifters are used to compensate for the initial phase errors caused by the fabrication errors. In the PILOSS topology, any optical path contains $N - 1$ *cross* state MZIs and one *bar* state MZI where N is the port count. These two states can be switched by adding π phase shift between

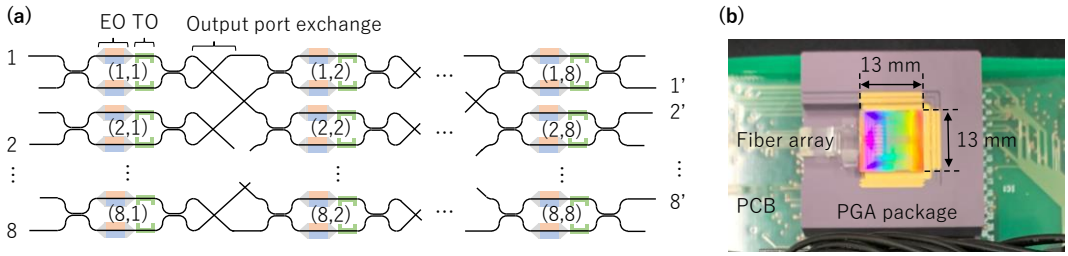

Fig. 1. (a) Schematic of the fabricated PILOSS 8 × 8 EO Si switch. (b) Photograph of the switch package.

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the upper and the lower arms. We first set all the MZIs to be *cross* state by using the TO phase shifters. Then, for each *N* paths, we turn-on one EO phase shifter by injecting current to the p-i-n junction to switch the MZI to *bar* state. Thus, in contrast to Beneš and DLN topologies, insertion loss of the PILOSS EO switch is independent of the path setting. After each MZI, the two output ports are exchanged in order to suppress the crosstalk between paths [7]. If we set π phase shift to the EO phase shifter, it also adds loss due to free-carrier absorption (FCA). This causes unbalanced interference at the output coupler of the MZI, resulting in the leakage to the untargeted port. Though this increases the optical crosstalk in the Beneš and DLN topologies, this does not affect to the crosstalk in the PILOSS topology because the untargeted port is always guided to one of terminated idle ports at the output edge (Fig. 1(a)).

We designed and fabricated the PILOSS 8 × 8 EO Si switch in AIST's 300-mm SOI wafer CMOS process line. After the dicing of the wafer, the chip was bonded on a 304-pin PGA ceramic package. A 20-fiber array was glued on the chip edge to couple the high-Δ optical fiber modes to the spot-size converters (SSCs) on the Si switch chip. The 304-pin PGA package was then inserted on a socket on a fanout PCB (Fig. 1(b)).

3. Measurement results and discussion

Figure 2(a) shows the schematic of the measurement setup. Wavelength-tunable LD was used as a light source. Input port was selected by using a 1 × 8 switch. Because the chip was designed only for TE-like mode, the input polarization was adjusted by using fiber polarization controllers (FPCs). The TO phase shifters on the chip were driven by 128-ch. current sources. Two voltage pulse generators were used to input fast and synchronized signals to drive EO phase shifters on a chip. Output optical power was monitored by using 8-ch. power monitors or by using fast (12.5 GHz) photoreceivers.

First, we measured the on-chip IL of all path settings on the fabricated 8 × 8 EO Si switch. For each 8 × 8 = 64 combinations of input and targeted output, we measured the target-port transmission and the leakages to the untargeted ports. The results are shown in Fig. 2(b). The wavelength and the power of the input CW light were set to be 1550 nm and +7 dBm, respectively. In this figure, each panel corresponds to each input port and the *x*-axis corresponds to the output ports. Each color corresponds to the target output settings. We ensured all EO/TO phase shifters on the chip were working and any path settings were possible with the on-chip loss of 3.8 ± 0.19 dB. The leakages were suppressed by more than 25 dB. The fiber-to-fiber loss was approximately 10 dB including the chip-to-fiber coupling loss of 3.05 dB per a facet. We note that the chip-to-fiber coupling loss can be further reduced by applying polishing to the chip edge [8]. The minimum on-chip loss of 3.3 dB includes the carrier absorption loss at the "ON" MZI of 1 dB, on-chip waveguiding loss of ~1.5 dB and passive ("OFF" state) MZI loss of ~0.1 dB each.

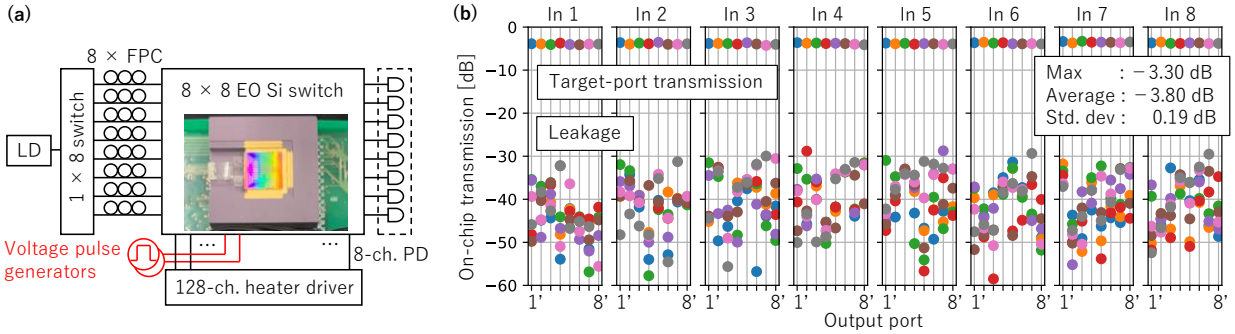

Fig. 2. (a) Schematic of the measurement setup. (b) Results of all-path IL measurement.

Next, we measured the switching speed from a path state (1-8') to a path state (1-6') as shown in Fig. 3(a). Positive edge with the height of 1.6 V, offset of −0.4 V was applied to the MZI of row 7 and col. 7. At the same time, a negative edge with the height of 1.62 V, offset of −0.42 V was applied to the MZI of row 8 and col. 8. The measured output optical power at output 6' and 8' are shown in Fig. 3(b). From these results, 10-90% rising time of 6.3 nsec was observed. We note that the negative offset is required to quickly remove the remaining free-carriers in the intrinsic region of the p-i-n junction. We consider that the difference in the amplitudes of the two waveforms in Fig. 3(b) is originated from the coupling efficiency between the fibers and the photodetectors. Next, we input negative edge to the MZI of row 7 and col. 7, and positive edge to the MZI of row 8 and col. 8 as shown in Fig. 3(c). The results are shown in Fig. 3(d). As shown in this figure, a falling time of 7.2 nsec was observed. From these results, a switching time of <8 nsec was observed. We note that the PCB used for this device was not impedance matched. Therefore, by carefully re-designing the PCB and signal transmission lines, further improvement of the switching speed is possible by reducing the electronic signal reflections observed in Figs. 3(b) and (d).

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We then measured the crosstalk spectrum of the 8 × 8 switch. The switch state was set to one of the worst crosstalk paths, which is (1-4'), (2-8'), (3-2'), (4-6'), (5-5'), (6-7'), (7-3'), and (8-1'). We first measured the transmission spectrum of the main path (6-7') as shown in the orange lines in Fig. 3(e). Other blue lines along the orange lines show targeted transmissions of the other ports, showing flat transmission similar to the main path. After that, the leakages from the other paths to the output port 7' were measured as shown in lower blue lines in Fig. 3(e). The crosstalk spectrum was then calculated by the division of the sum of the leakages by the main path transmittance as shown in Fig. 3(f). As seen from this figure, the crosstalk was suppressed by more than 20 dB for the wavelength range of 1535 nm to 1566 nm. We note that the crosstalk can further be suppressed by using double-MZI configuration as proposed in silica platform [9], with a small cost of <1 dB total loss increase [10]. Recently, by applying this configuration to Si platform, we have demonstrated 30 dB crosstalk suppression with very broad bandwidth of 110 nm [10]. We consider that the same configuration could be applied for the EO switch.

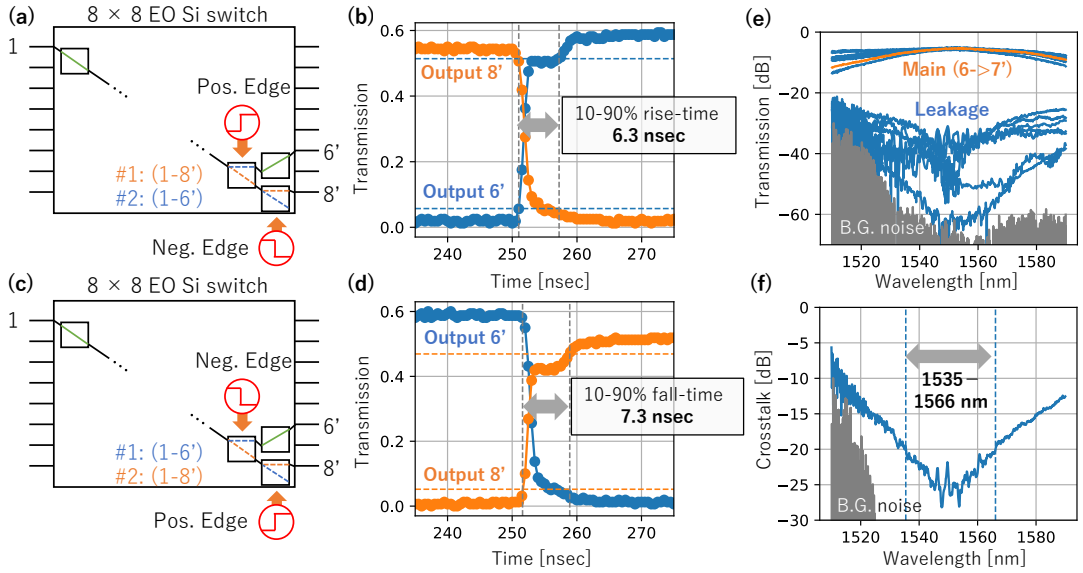

Fig. 3. (a), (c) Schematic of the switching experiments between (1-8') and (1-6'). (b), (d) Measured optical power from outputs 6' and 8'. (e) Raw data of the measured transmittance of the main path and the leakages to the main path with one of the worst-case crosstalk settings. (f) Calculated worst-case crosstalk spectrum of the 8 × 8 switch.

We finally discuss the future scaling of our device. Fiber-to-chip coupling loss of 1.4 dB / facet will be possible by using PLC connectors as shown in [8]. Therefore, by simply scaling the measured device up to 32 × 32, the fiber-to-fiber insertion loss of ~8.5 dB (0.1 dB × 32 for MZI, 1 dB for FCA, 1.4 × 2 dB for the coupling, and 1.5 dB for routing) can be expected. Moreover, the loss is independent of the path settings. For example, if we designed this switch using Beneš (DLN), the path with a minimum loss would have zero "ON" MZIs while the path with a maximum loss would have (2×) $\log_2 N - 1$ "ON" MZIs. In this case, these paths would have ~4 (~9) dB difference in their losses. Therefore, PILOSS-based EO switches would have merits as discussed in the introduction.

Acknowledgements

This paper is partly based on results obtained from a project, JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

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