

Improved Soft-aided Error-and-erasure Decoding of Product Codes with Dynamic Reliability Scores

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Abstract: We propose a novel soft-aided low-complexity decoder for product codes based on dynamic reliability scores and error-and-erasure decoding. We observe coding gains of up to 1.2 dB compared to conventional hard-decision decoders. © 2022 The Author(s)

1. Introduction

Product codes (PCs) [1] are powerful code constructions with high net coding gains (NCGs) suitable for high-speed optical fiber communications. Soft-decision decoding of PCs, also known as turbo product decoding (TPD) [2], delivers excellent error-correcting performance at the cost of a very high internal decoder data flow with soft message-passing. In contrast, hard-decision decoding (HDD), in particular the ubiquitous iterative bounded distance decoding (iBDD) decoder, reduces the data flow significantly at the expense of a performance penalty. Recently, various hybrid algorithms have been proposed that use a certain amount of soft information to improve the coding gain of HDD while keeping the decoder data flow manageable. A promising approach to improve the decoding performance of PCs is to use error-and-erasure (EaE) decoding, e.g., [3] and [4]. A third channel output symbol, the “erasure”, provides an elegant way to represent and update the bits with very low channel reliability. However, the additional coding gain is small, mostly because of the lack of miscorrection control. The BEE-PC [8] decoder uses EaE decoding with a relatively complex miscorrection control to improve the coding gain of PCs. A simpler approach to miscorrection-detection is to make use of the conflict between row/column decoding results and the bits that are considered very likely to be correct. These bits are called anchor bits in anchor decoding (AD) [5] and highly-reliable bits (HRBs) in soft-aided bit marking (SABM) decoding [6]. The latter is improved to SABM with scaled reliabilities (SABM-SR) in [7] for PCs. The difference between the two families of algorithms lies in the marking of these bits. For AD, no channel reliability is used, the decoder sets all successfully decoded bits as anchor bits together with a back-tracking mechanism. In SABM, the HRBs are set according to the channel reliability during the initialization of decoding. Both algorithms provide good miscorrection-detection. Several other schemes have been proposed for PCs with varying degrees of performance-complexity trade-off [9–11].

In this paper, we improve EaE decoding from [3] by introducing a simple and low-cost miscorrection control which resembles a combination of AD and SABM. We show coding gain improvements of 0.2 dB to SABM-SR decoding with significantly reduced complexity.

2. Preliminaries

We consider PCs of rate $r = k^2/n^2$ whose each row/column vector \mathbf{x} is a codeword of an (n, k, t) component code \mathcal{C} , where \mathcal{C} is either a $(2^v - 1, k_0, t)$ binary Bose–Chaudhuri–Hocquenghem (BCH) code or its $(2^v - 1, k_0 - 1, t)$ even-weight subcode able to correct t errors. Let d_{des} ($d_{\text{des}} \leq d_{\text{min}}$) be the design distance of \mathcal{C} and $t = \lfloor (d_{\text{des}} - 1)/2 \rfloor$. The codewords are transmitted over a binary-input additive white Gaussian noise (BI-AWGN) channel which outputs $\tilde{y}_i = (-1)^{x_i} + n_i$, where n_i is (real-valued) AWGN with noise variance $\sigma^2 = (2rE_b/N_0)^{-1}$. To obtain the discrete channel output $y_i \in \{0, ?, 1\}$, the values $\tilde{y}_i \in [-T, +T]$ are declared as erasures “?”, where T is a configurable threshold. Values outside this interval are mapped to 0 and 1 by the usual HDD rule.

We define $\mathcal{S}_t^3(\mathbf{c}) := \{\mathbf{y} \in \{0, ?, 1\}^n : 2d_{\sim E(\mathbf{y})}(\mathbf{y}, \mathbf{c}) + E(\mathbf{y}) < d_{\text{des}}\}$, as the Hamming sphere in $\{0, ?, 1\}^n$ for a codeword $\mathbf{c} \in \mathcal{C}$ where $E(\mathbf{y}) := |\{i : y_i = ?\}|$ is the number of erasures of \mathbf{y} and $d_{\sim E(\mathbf{y})}(\mathbf{y}, \mathbf{c})$ is the Hamming distance between \mathbf{y} and \mathbf{c} at the unerased coordinates of \mathbf{y} . We use the following EaE decoder (EaED) which is a modification of [12, Sec. 3.8.1]. Let $\mathbf{y} \in \{0, ?, 1\}^n$ be the received row/column vector and $\mathbf{w} := \text{EaED}(\mathbf{y})$. If $E(\mathbf{y}) \geq d_{\text{des}}$, we do not decode and return $\mathbf{w} = \mathbf{y}$. If $E(\mathbf{y}) < d_{\text{des}}$, the erasure positions of \mathbf{y} are first filled with two complementary random vectors in $\{0, 1\}^{E(\mathbf{y})}$, resulting in two words $\mathbf{y}_1, \mathbf{y}_2 \in \{0, 1\}^n$. Note that the use of distinct random vectors is crucial for the performance of the decoder. Then, two bounded distance decoding (BDD) steps are performed. Let $\mathbf{w}_1 := \text{BDD}(\mathbf{y}_1)$ and $\mathbf{w}_2 := \text{BDD}(\mathbf{y}_2)$ and let $d_1 = d_{\sim E(\mathbf{y})}(\mathbf{y}, \mathbf{w}_1)$ and $d_2 = d_{\sim E(\mathbf{y})}(\mathbf{y}, \mathbf{w}_2)$. If both BDD steps fail, set $\mathbf{w} = \mathbf{y}$. If $\mathbf{w}_i \in \mathcal{C}$ for exactly one \mathbf{w}_i , set $\mathbf{w} = \mathbf{w}_i$. If both BDD succeed then $\mathbf{w} = \mathbf{w}_1$ if $d_1 < d_2$ and $\mathbf{w} = \mathbf{w}_2$ if $d_1 > d_2$; If $d_1 = d_2$, one of the codewords \mathbf{w}_i is chosen at random. Such an EaED is able to correct any joint EaE pattern if $\mathbf{y} \in \mathcal{S}_t^3(\mathbf{c})$ [3, Theorem 1]. Moreover, EaED can correct some joint EaE patterns for $2d_{\sim E(\mathbf{y})}(\mathbf{y}, \mathbf{c}) + E(\mathbf{y}) \geq d_{\text{des}}$ because all (or most) of the erasures may possibly be filled with a correct value when generating \mathbf{y}_1 and \mathbf{y}_2 . Thus, EaED has potentially higher error-correcting capabilities than a one-step EaE decoder [14] but is also more prone to miscorrections without the constraint that $\mathbf{w} \in \mathcal{S}_t^3(\mathbf{y})$.

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3. Proposed Algorithm

We introduce a *dynamic reliability score (DRS)* for all the bits. The DRSs are stored in an additional register. The DRS reflects the reliability of a bit from both its channel output reliability and its behavior during the decoding. The DRS is defined by an integer in the range $[0, 31]$

such that it can be represented with 5 bits. We manually set a threshold T_a . Following [5], all bits with a $DRS > T_a$ are classified as anchor bits during decoding and are not allowed to be flipped by a component code decoder.

Figure 1 depicts the block diagram and workflow of the proposed decoder. At the initialization, the received PC word \tilde{Y} is fed to two paths. In the upper path, for all bits in \tilde{Y} , the absolute values $\{|\tilde{Y}_i| : i \in \{1, 2, \dots, n^2\}\}$ are sorted ascendingly and then evenly divided into 16 groups (allowing the last group to have fewer entries than the others if n^2 does not divide 16). To each group, we assign a DRS in the range of $[9, 24]$ accordingly. The bits with lowest $|\tilde{Y}_i|$ will have DRS 9 while the bits with highest $|\tilde{Y}_i|$ will have a DRS of 24. This initial DRS value is stored in the DRS register. In the lower branch, erasures are marked if $|\tilde{Y}_i| < T$, with T (defined in Sec. 2) an optimizable threshold. For non-erased bits, a usual hard-decision is performed. The values in $\{0, ?, 1\}$ are passed to the iterative row and column decoder.

Iterative row and column decoding is performed with an EaED for the component codes. Additionally, after every decoding step, the miscorrection detection unit evaluates whether an anchor bit is flipped by the decoding decision. In this case, this decision is discarded and the DRS for all the anchor bits in conflict is reduced by one. If a decoding step does not flip any anchor bit, this decision will be accepted while the DRS of all flipped bits is reduced by one. If a vector is already a codeword and thus no decoding is performed, the DRS of every bit in it is increased by one. In the case of a decoding failure, neither the codeword nor the DRS is changed. In addition, the threshold T_a is increased by 1 every five decoding iterations, such that a small penalty is given for words that fail to decode consistently. With the update of DRSs, the anchor bits are reevaluated every iteration. A simple yet elegant updating of both the unreliable (via erasures) and highly-reliable bits (via DRSs) is achieved. We call this new algorithm dynamic reliability score decoder (DRSD).

During the decoding, only hard messages are passed. For EaED, ternary messages are used. For the communication between the DRS register and the decoder, binary messages are sent from the DRS register to the EaED representing whether a bit is an anchor or not and from the EaED to the DRS register representing an increase/decrease of the DRS. However, the information flow is still higher than iBDD. The major computational overhead of our algorithm comparing to iBDD is the usage of EaED, where two BDD steps are performed with the presence of erasures for every row/column decoding. This increases the total number of BDDs, especially in the first few iterations, before the erasures are resolved. Words without erasures can be decoded with conventional BDD. The additional storage for DRSs is relatively small as well, as the DRSs are stored with 5-bit integers.

4. Simulation Results

For simulation, we consider the two cases with 10 or 20 decoding iterations. For 10 iterations, we decode with 8 iterations of DRSD first, followed by 2 simple EaED iterations not using the DRS register; For 20 iterations, we use 16 iterations of DRSD followed by 4 plain EaED iterations. This eliminates the influence of erroneous bits with high DRS. We also simulate an *ideal* EaED with a genie-aided miscorrection detection where miscorrections are always discarded to benchmark our results.

In Fig. 2, the noise threshold gain of DRSD (opaque markers) for a target bit error rate (BER) at 10^{-4} over iBDD is shown for various component codes as well as the respectively optimal erasure thresholds T (T_{opt}). We allow 20 iterations for both decoders. The noise thresholds are estimated by a Monte Carlo method along with a binary search. We observe that slightly varying T (within $\pm 10\%$) does not degrade the performance severely. The initial value of the anchor threshold T_a is set to be 9 for $t = 2$, 10 for $t = 3$, and 12 for $t = 4$, except for the (127, 4) component codes where $T_a = 14$. The transparent markers stand for ideal EaED with 16 iterations (the optimal threshold T may differ but is not plotted for the sake of clarity). One can see that the larger the t and the higher the code rate, the closer the DRSD performs to an ideal EaED, which means our decoder is nearly miscorrection-free. Unfortunately, both decoders show smaller gains in this region.

In Fig. 3, we compare the residual post-FEC BER after 10 decoding iterations for different decoders (we additionally show the DRSD performance after 20 iterations). We use even-weight subcodes of BCH codes as component codes denoted by $C_1(127, 112, 2)$ and $C_2(255, 238, 2)$ with PC rates of 0.78 (28% overhead) and 0.87 (15% overhead), respectively. For reference, we show the results of TPD and SABM-SR with the data points

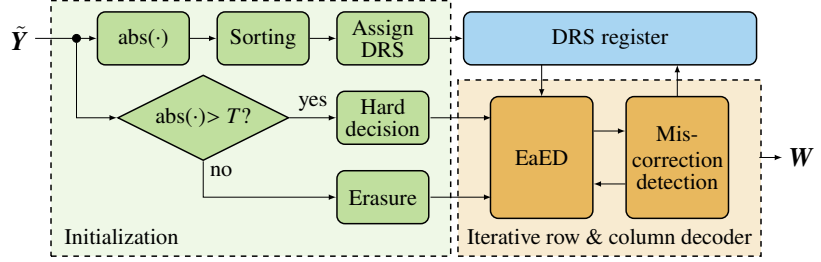


Fig. 1: Block diagram of the proposed DRSD

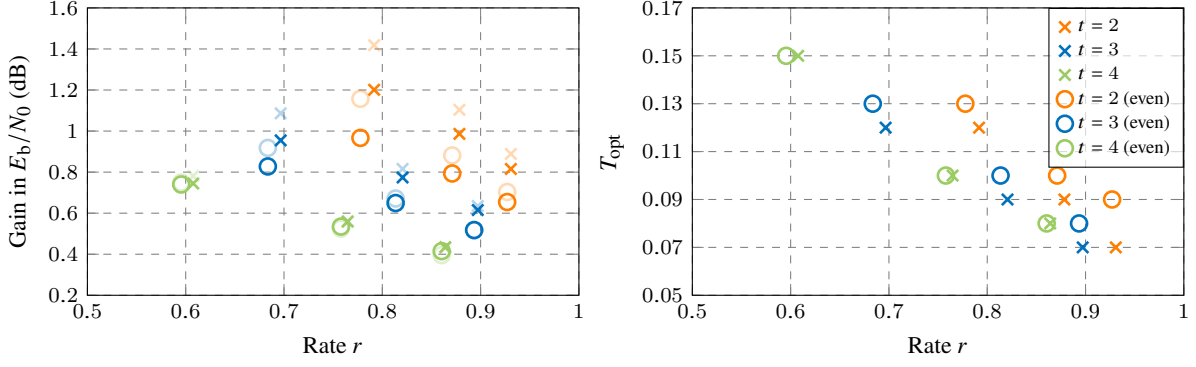


Fig. 2: Simulation results of the parameter analysis: The noise threshold gain that the DRSD achieves compared to iBDD is plotted on the left and the corresponding optimal threshold T_{opt} for erasures on the right. The component codes are (n, k, t) -BCH code with $n \in \{127, 255, 511\}$ and $t \in \{2, 3, 4\}$ or their even-weight subcodes. The transparent markers corresponds to the respective ideal EaED.

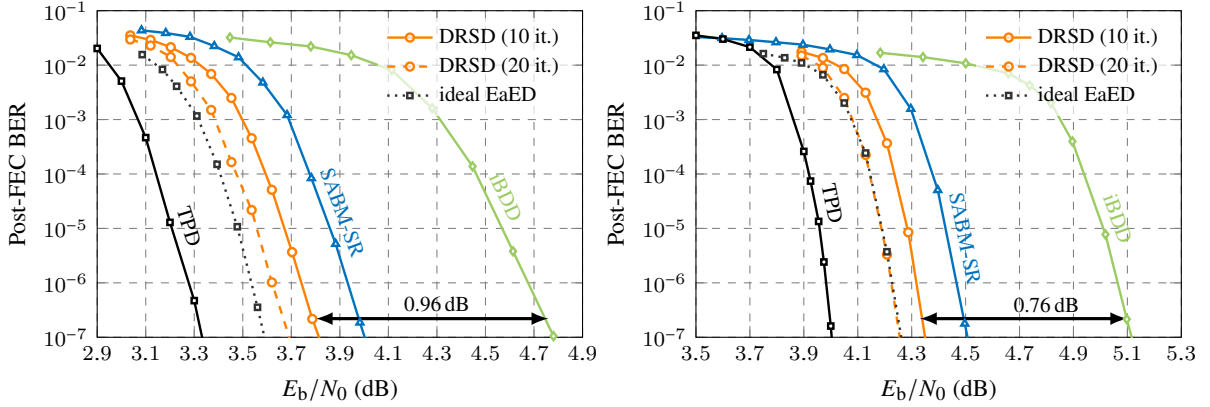


Fig. 3: BER vs. E_b/N_0 (in dB) curve for product codes of rate 0.78 (28% overhead, left plot) and 0.87 (15% overhead, right plot).

provided in [7] where the component codes are singly-extended BCH codes with parameters $(128, 113, 2)$ and $(256, 239, 2)$ (hence with a small, negligible rate difference compared to our codes). For both PCs, an obvious gain compared to iBDD can be observed and the performance is further improved by running 20 iterations. With twice the iterations, our decoder behaves very closely to an ideal EaED and has only a small gap to the significantly more complex TPD. For the rate 0.78 PC, we estimate at a residual BER of 10^{-15} a NCG of 10.88 dB (10 iterations) and 11.03 dB (20 iterations). For the rate 0.87 PC, the conjectured NCGs are 10.51 dB and 10.59 dB respectively.

5. Conclusions

The proposed DRS decoder outperforms other soft-aided HDD schemes with a near miscorrection-free EaE decoding keeping the complexity similarly low as conventional iBDD. The NCGs make this scheme a promising candidate for future low-complexity optical communication systems. Future research directions include the extension of this scheme to staircase codes [13].

References

1. P. Elias, "Coding for noisy channels," in *IRE Convention Record, Part IV*, (1955).
2. R. M. Pyndiah, "Near-optimum decoding of product codes: Product turbo codes," *IEEE Trans. Commun.* **46**, (1998).
3. L. Rapp and L. Schmalen, "Error-and-erasure decoding of product and staircase codes," *IEEE Trans. Commun.*, early access (2021).
4. D. K. Soma, A. K. Pradhan, and K. Narayanan, "Errors and erasures decoding of product codes for optical transport networks," *IEEE Communications Letters* (2021).
5. C. Häger and H. D. Pfister, "Approaching miscorrection-free performance of product codes with anchor decoding," *IEEE Trans. Commun.* **66**, (2018).
6. Y. Lei, B. Chen, G. Liga, X. Deng, Z. Cao, J. Li, K. Xu, and A. Alvarado, "Improved decoding of staircase codes: The soft-aided bit-marking (SABM) algorithm," *IEEE Trans. Commun.* **67**, (2019).
7. G. Liga, A. Sheikh, and A. Alvarado, "A novel soft-aided bit-marking decoder for product codes," in *Proc. ECOC* (2019).
8. A. Sheikh, A. Graell i Amat, and A. Alvarado, "Novel high-throughput decoding algorithms for product and staircase codes based on error-and-erasure decoding," *J. Lightw. Technol.* (2021).
9. A. Sheikh, A. Graell i Amat, G. Liva, and A. Alvarado, "Refined reliability combining for binary message passing decoding of product codes," *J. Lightw. Technol.* (2021).
10. A. Sheikh, A. Graell i Amat, G. Liva, C. Häger, and H. D. Pfister, "On low-complexity decoding of product codes for high-throughput fiber-optic systems," in *Proc. ISTC* (2018).
11. A. Sheikh, A. Graell i Amat, and G. Liva, "Binary message passing decoding of product-like codes," *IEEE Trans. Commun.* **67**, (2019).
12. T. K. Moon, *Error Correction Coding - Mathematical Methods and Algorithms* (John Wiley & Sons, Inc., 2005).
13. B. Smith, A. Farhood, A. Hunt, F. Kschischang, and J. Lodge, "Staircase codes: FEC for 100 Gb/s OTN," *J. Lightw. Technol.* (2012).
14. G. Forney, "On decoding BCH codes," *IEEE Trans. Inf. Theory* **11**, (1965).