Investigation of Potential FEC Schemes for 800G-ZR Forward Error Correction

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Abstract: With a record 400Gbps 100-piece-FPGA implementation, we investigate performance of the potential FEC schemes for OIF-800GZR. By comparing the power dissipation and correction threshold at 10^{-15} BER, we proposed the simplified OFEC for the 800G-ZR FEC.
OCIS codes: (060.1660) Coherent communications; (060.2330) Fiber optics communications

1. Introduction

Motivated by the fast-growing data-center interconnection market needs, Optical Internetworking Forum (OIF) initiate the development of an implementation agreement (IA) for 800G ZR, of which forward error correction (FEC) is a cornerstone. Several competitive potential FEC schemes, including the CFEC, OFEC and MLC codes of a concatenated Low-Density Parity-Check (LDPC) and Turbo Product Code (TPC), are proposed. Up to now, it does not reach an agreement for the 800G-ZR FEC and is necessary to investigate the power dissipation and the correction threshold, especially at 10^{-15} BER, before the agreement reached.

Because of the fine trade-off between the power dissipation and correction threshold, the concatenated staircase and Hamming code (CFEC) with correction threshold at 1.21e-2 proposed by Inphi are adopted by the standard FEC of 400G ZR OIF [1] and 80km distance transmission scenes of G.709.3 [2]. In the middle of the soft decision FEC (SD-FEC) and enhanced FEC (EFEC), the CFEC adopted a concatenated simplified non-iterative Soft-in Hard-out (SIHO) Hamming inner code and iterative Hard-in Hard-out (HIHO) staircase outer code, which is compatible lower power dissipation and higher correction performance. In order to accommodate with the further distance transmission, the Open FEC (OFEC) with correction threshold at 2e-2 proposed by Acacia is adopted by the standard FEC of the 400G Open ROADM Multi-Source Agreement (MSA) [3] and 450km distance transmission scenes of G.709.3. The OFEC has better correction performance than CFEC, whereas the power dissipation of the OFEC is more than three times that of the CFEC, which is unacceptable for 800G ZR. In order to maintain the balance the power dissipation and correction performance, Fujistu [4] proposed the MLC code with correction threshold at 1.8e-2 that is a concatenated spatially-coupled LDPC and HIHO TPC. For the MLC scheme, the inner LDPC code correct the higher bit error bits for 16QAM constellation, the residual error of higher bit error bits and the error of lower bit error bits are corrected by the outer TPC code.

Due to the data and baud rate doubled, the CFEC performance is not enough for 800G ZR in all application scenario. According to our previous experience[5], the CFEC has an error flare around 10^{-10} BER lowering the BER threshold from 1.25e−2 as predicted in the OIF proposal to 1.21e−2. So it is meaningful to investigate the error floor of the OFEC and LDPC code with the record 400Gbps 100-piece-FPGA platform. Meanwhile, we compare the three potential FEC schemes for the power dissipation.

2. FPGA Implementation of the OFEC Code

The OFEC is a convolutional TPC structural code, which comprises a block-code-based encoder and iterative SD decoder with 11.6 dB Net Coding Gain (NCG) and 2.0e-2 correction threshold at 1e-15 post-FEC with 16QAM after 3 SD iterations and 2 hard decision (HD) iterations. Figure 1 shows the schematic of the FPGA platform for emulating the OFEC schemes.The implementation employs 100 pieces of Xilinx ultrascale-XCVU125 FPGA clocked at 125 MHz. On each of the 100 FPGA chips, the implementation occupies 420K configurable logic blocks, 864 on-chip block memories (36K bits/block), and 705 multipliers.

On the transmitter side, a pseudo random generator (PRG) composed of 32 linear-feedback shift register (LFSR) feed parallel PRBS streams into OFEC encoder. After block interleaving, the bit stream modulated into 16QAM symbols. Then the BM GVG [6] adds 16-lane uncorrelated GV with up to 27-bit accuracy. The SNR is configurable using a register with a tuning resolution of 0.005dB [5]. On the receiver side, the received noisy 16-QAM symbols are demodulated and converted into 6-bit log-likehood-ratios (LLR) as soft decisions. The subsequent de-interleaver uses to randomize error distribution for next decoding step which include *s* times SISO decoder and *h* times HIHO decoder. In each SISO decoder, it comprises least reliable position (LRP) finder, *tp* times BCH decoder, candidate codewords selector and extrinsic data calculator modules.

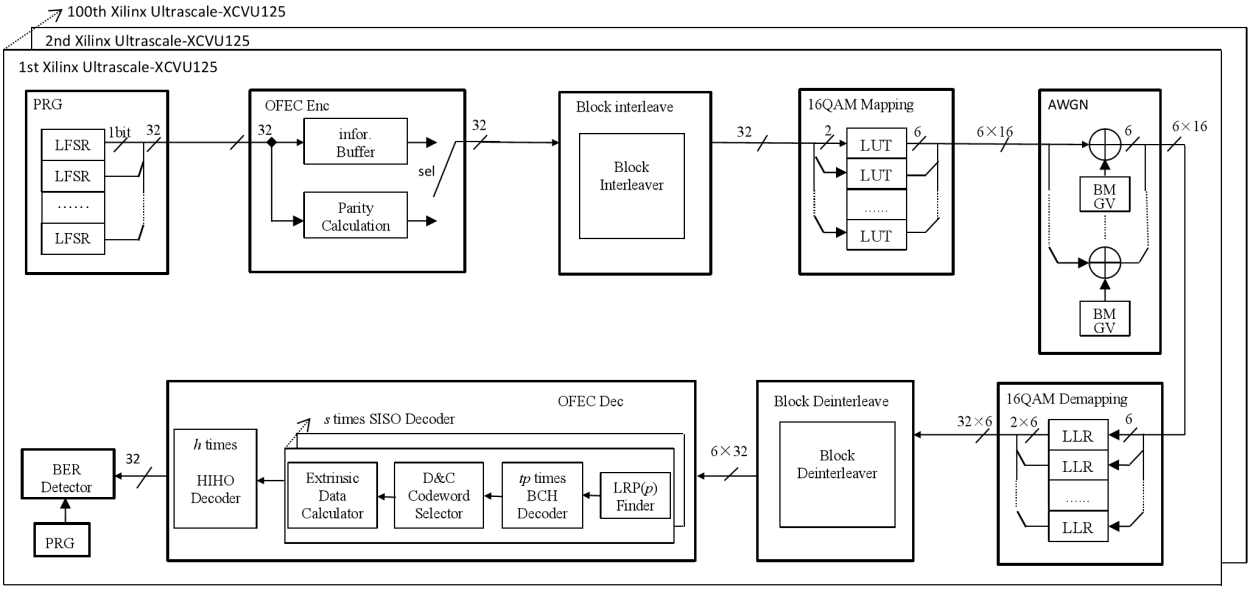

Figure 1: FPGA implementation of the OFEC verification system

Clocked at 125 MHz, the decoding rate with 100-piece-FPGA achieves 400Gbps. A bit error detector is tested based on the same PRBS as generated at the transmitter side to measure the post decoding BER. For measurement, at least 100 errors are observed for BER above 10^{-14}, otherwise the minimum error observations is set at 10. Thus even with the record 400Gbps throughput rate, it takes 7 hours to obtain a measurement point at 10^{-15} BER.

3. Power dissipation investigation for CFEC, OFEC and LDPC codes

The computation complexity of CFEC is mainly dependent on Hamming SD decoder and staircase HD decoder, whose computation complexity and correction threshold are decided by the number of staircase blocks and iteration. When the number of staircase blocks equals five and iteration numbers equals six, the power dissipation of CFEC is approximately 400mW in 7nm CMOS technology [1]. Similarly, the computation complexity and correction threshold of OFEC is mainly dependent on the number of SISO decoder and the number of *p* and *tp* parameter in each SISO decoder as shown in Fig. 1. When the number of SISO decoder equals three, *p* equals 8 and *tp* equals 93, the power dissipation of OFEC is approximately 1350mW in 7nm CMOS technology [7]. In the MLC scheme, only a quarter of data feed in the LDPC encoder and decoder, so the the mainly power dissipation of MLC code is composed of a quarter of LDPC decoder and a complete TPC decoder, which is approximately 450mW in 7nm CMOS technology [4].

It is the disadvantage of CFEC that the performance is not enough for 800G ZR in all application scenario. The disadvantage of MLC is that it is not compatible with previous standard. These two concatenated code schemes are hard to extend to farther distance application. There is no these trouble for OFEC, but the power dissipation of OFEC is unacceptable. In order to reduce the power dissipation of the OFEC scheme, we investigate the power dissipation proportion of each block in one SISO decoder with *p* equals 8 and *tp* equals 93 as shown in Tab. 1. It is a effective way to reduce the power dissipation that decreasing the *p* and *tp* because these two parameter decide the computation complexity of each SISO decoder. Meanwhile, Tab. 2 reveals the FPGA resources in different parameter of *p* and *tp* with the FPGA implementation in Figure 1. The FPGA resources of *tp* equals 15 is less than half of the FPGA resources of *tp* equals 93.

Table 1: power dissipation proportion in one SISO decoder

	LRP Finder	BCH Decoder	Candicate Codeword Selector	Extrinsic Data Calculator	other
Proportion	13.70%	27.20%	28.50%	19.90%	10.70%

Table 2: FPGA resources in different *tp*

	LUT	LUTRAM	FF	BRAM	DSP
tp=93	140026	4536	207631	288	235
tp=42	114024	3648	125363	226	85
tp=15	75557	3344	86431	190	85

4. Performance Investigation with the FPGA Platform

Fig. 2 plots the OFEC performance with different number of iterations and *p*. It shows that the correction threshold is 2e-2 for 3 SISO with *tp* equals 93 and 2 HIHO. When the number of SISO decreased, the error floor emerged. However, it also exists severe error floor when the number of SISO with *tp* equals 42 increased to four appending

with only one HIHO. It seems that it is necessary to investigate the potential FEC correction threshold at 10^{-15} BER before casting a ballot for criterion, especially for the LDPC code because of its severe error floor[8].

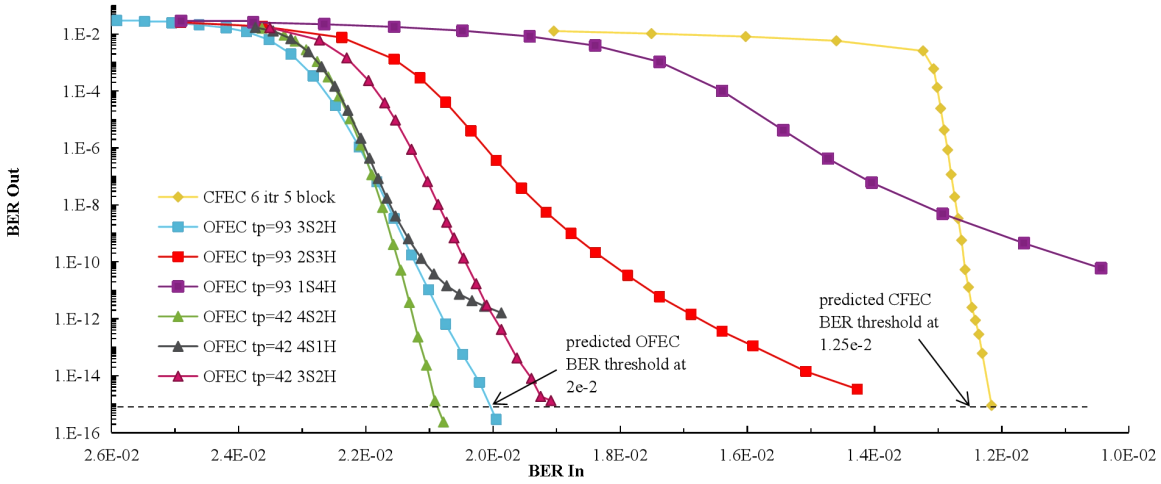

Figure 2: OFEC performance with different number of iteration and *tp*

As shown in Fig. 3, the performance of three SISO iterations with different *tp* and two HIHO iterations is investigated. The *tp*=42,15,15 means that the number of *tp* equals 42, 15, 15, respectively, for the first, second and third SISO iteration. It reveals that the correction threshold is 1.81e-2 for this simplified OFEC and it is easy to improve performance to support future network. Meanwhile, the power dissipation of this scheme is half of OFEC [7], namely 675mW which seems a good choice for 800G-ZR.

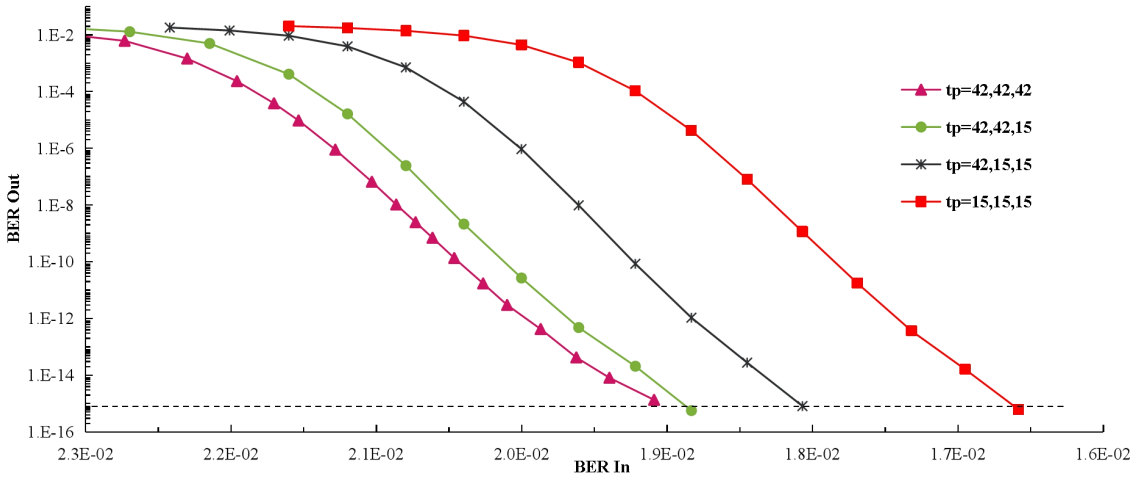

Figure 3: OFEC performance with different *tp*

5. Conclusions

A timely verification on the OFEC to be chosen as potential OIF 800G-ZR FEC is performed with an FPGA implementation at record 400Gbps. We investigate the power dissipation and correction threshold for different OFEC with different iteration numbers and test patterns in each SISO. The optimal number of iterations and test patterns is proposed and the correction threshold is 1.81e−2. In consideration of extend the farther distance application for future, we proposed the simplified OFEC for the 800G-ZR FEC.

6. References

[1] A. Farhood, *et al.*, OIF 400G ZR, oif2017.364.00, 2017.
[2] ITU-T G.709.3/Y.1331.3 (2018), Flexible OTN long-reach interfaces.
[3] 20181217a Open-ROADM-MSA-specification-ver-3-00.
[4] Junichi Sugiyama, *et al.*, oif2021.217.00, 2021.
[5] Y. Cai, *et al.*, OFC'2018, postdeadline paper Th4C.2, 2018.
[6] A. Alimohammad, *et al.*, Trans. on VLSI Sys., vol. 16, no. 5, 2008.
[7] M. Weber, *et al.*, CD11-M03r2, 2019.
[8] Y. Cai, *et al.*, ECOC'2019, paper M.2.D.1., 2019.