PON Virtualization Including PHY Softwarization

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Abstract: This paper summarizes studies on passive optical network (PON) virtualization, including the softwarization of physical-layer (PHY) coding and digital signal processing (DSP), as well as PON abstraction, which provide flexibility and agility to access networks.
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1. Introduction

The optical access network based on passive optical networks (PONs) is continually evolving and various specifications have been standardized to meet market driven diversity in speed, distance, etc. Moreover, the role of central offices (COs) is being expanded from providing fiber to the home (FTTH) services to accommodating the rapidly increasing 5G/6G radio access network (RAN) and other brand-new services. In order to realize systems that can meet these diverse demands, the flexibility and agility offered by network function virtualization (NFV) and software-defined network (SDN) are crucial.

We depict the traditional architecture, cutting-edge architecture and expected future architecture of access systems in Fig. 1. The traditional architecture sets a complete set of functions including PHY, media access control (MAC) and management in chassis-type optical line terminals (OLTs), which makes flexible function changes difficult. As the cutting-edge architecture, SDN-enabled broadband access (SEBA) makes connected access network devices look like SDN programmable switches to the SDN controller by using a common application programmable interface (API) to abstract multiple kinds of devices [1]. The functionality of management and abstraction is implemented on general-purpose servers, and physical-layer (PHY) processing and MAC are implemented by dedicated circuits inside whitebox OLTs. The OLT functions are public as open source software (OSS). It also tries to support agile development of upper-layer network functions and edge computing by re-architecting COs as data centers. Its challenge is abstraction including technology profile as well as bandwidth profile that allows OLT to be controlled via PON technology and vendor-agnostic API. Regarding the future architecture, we target the architecture that softwarizes the complete set of OLT functions including PHY processing in general-purpose servers [2]. This maximizes flexibility and agility of OLTs; speeds and protocols can be flexibly and instantly switched to support a variety of services. The challenge is to softwarize PHY processing, which has high computation loads and to design an architecture that supports high-speed transfer. This paper summarizes this architecture based on virtualization including abstraction that supports various PON technologies and further softwarization of PON PHY.

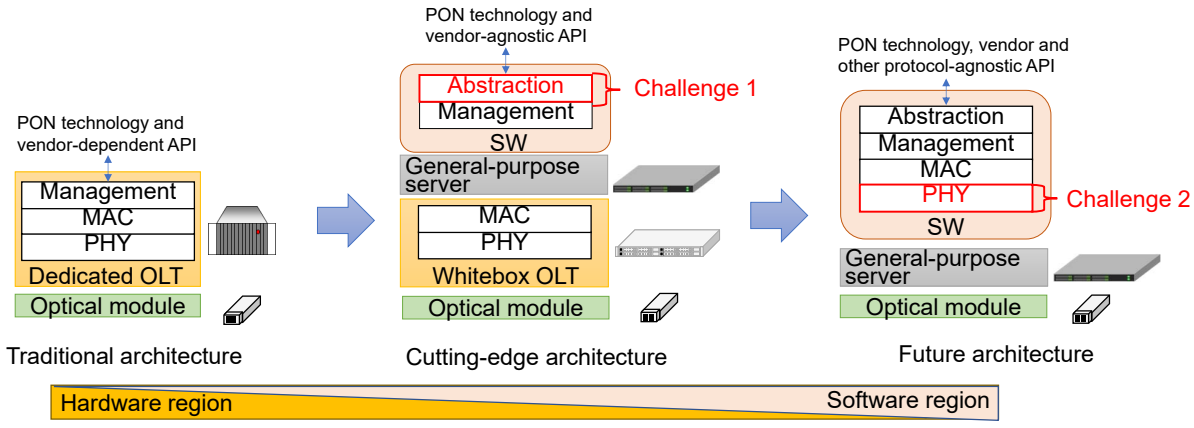

Fig. 1. Evolution of PON architecture based on virtualization.

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2. PON abstraction

The first essential technique for virtualized PON is abstraction; SEBA is being developed worldwide and has begun to be deployed in real environments. Figure 2 (a) presents the PON abstraction architecture based on SEBA-related OSS. SEBA is a platform that implements virtualized access functions, and realizes common management that does not depend on access specification or vendor. SEBA is composed of adapter, virtual OLT hardware abstraction (VOLTHA), SDN controller called open networking operating system (ONOS) and network edge mediator (NEM). The adapter sends management commands to the whitebox OLT via vendor-dependent application programming interface (API) as instructed by the VOLTHA core, and passes OLT/ONU information to the VOLTHA core. The containerized adapter can be switched with other-type adapter. ITU-T PON ONU is managed via the ONU Management Control Interface (OMCI) while IEEE PON is managed via extended operation, administration, maintenance (eOAM). The adapter for ITU-T PON can be switched with the adapter for IEEE PON as well as those for other vendors corresponding to each OLT/ONU hardware. VOLTHA core is the key component that provides PON technology and vendor-agnostic API, and manages OLT/ONU status based on the information obtained from adapters. It enables the SDN controller to operate OLT/ONUs as programmable Ethernet switches. VOLTHA has key value store that stores PON-specific setting information called the technology profile. This profile includes PON type, DBA settings, QoS settings and encryption setting, all of which depend on PON specification. It can be switched depending on the specification of hardware utilized, and setting parameters are stored in variables of VOLTHA according to the structure of the technology profile [3]. SDN controller is responsible for setting bandwidth and port status to VOLTHA core via OpenFlow. NEM mainly provides the functions that mediate between VOLTHA API and element management system (EMS), while also providing zero touch provisioning (ZTP) for OLT/ONU. The ZTP requires workflows that permit automation from configuration input to authentication completion detection to OLT / ONU activation. Due to the difference in authentication method between ITU-T PON and IEEE PON, different workflows are implemented and can be switched [4].

3. PON PHY softwarization

The second challenge for maximizing the merit of SDN/NFV is to softwarize the entire set of OLT functions including PHY. We are tackling the softwarization of 10G-EPON physical coding sublayer (PCS) and the softwarization of DSP as essential functions for higher-speed PON systems.

Figure 2 (b) shows a verification platform for 10G-EPON PCS softwarization [2]. 10G-EPON PCS is implemented on the platform consisting of a general-purpose server with GPUs. 10G-EPON PCS mainly consists of PON frame synchronization/framer, Reed-Solomon (RS) (255, 223) encoding/decoding, 64b66b scrambler/descrambler. To prototype and verify a service node interface (SNI), an Ethernet framer/deframer is implemented and network interface card (NIC) is connected to a server. 10G-EPON frames are treated by an IF board. At the moment, an idle signal is inserted between PON frames, and only PCS processing performance is verified using continuous signals. Both upstream and downstream 10G-EPON PCS are verified. 10G Ethernet frames generated by network tester are converted into 10G-EPON frames and the 10G-EPON frames are looped back. The returned 10G-EPON frames are decoded and input to the network tester as 10G Ethernet frames. There are three

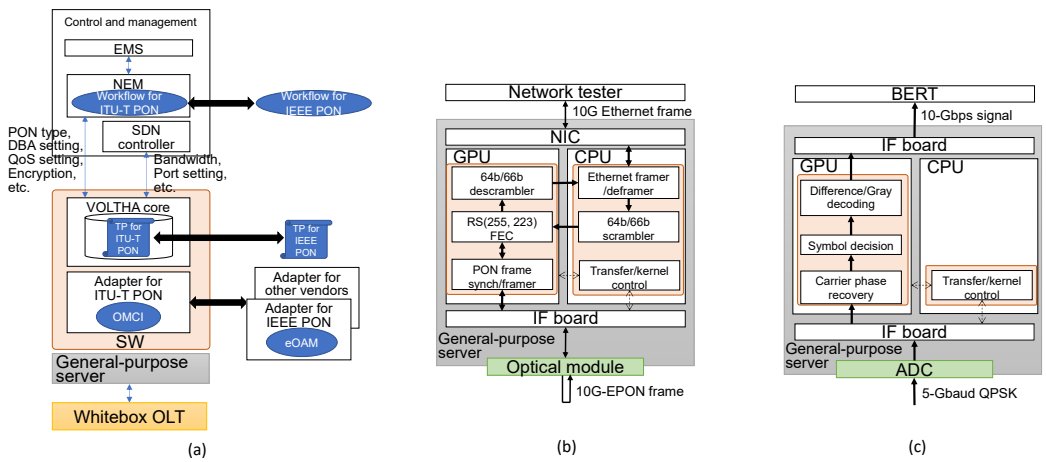

Fig. 2. (a) PON abstraction based on VOLTHA, (b) verification architecture for 10G-EPON PCS softwarization and (c) verification architecture for DSP softwarization.

primary challenges to achieve this softwarization. First is data transfer to the accelerators GPUs. Conventional GPU acceleration transfers data via CPU memory, which causes large delay. Our direct transfer method from IF board to GPUs resolves this issue; GPU direct transfer is realized by setting the physical address of the GPU memory as the transfer destination of the IF board and configuring a ring buffer [5]. Second challenge is the high computational loads of PON frame synchronization, which is processing that detects burst delimiter (BD) at the beginning of each PON frame. Although it requires bit-level calculation, the amount of calculation is reduced by thinning out the calculations. Given that PON frames have a long repeating synchronization pattern, BD is detected after rough matching via the synchronization pattern [6]. Third challenge is speeding up sequential processing. The 64b66b scrambler uses sequential processing that cannot be processed in parallel. We have proposed a CPU-GPU cooperative architecture in which the 64b66b scrambler is implemented by a CPU that specializes in sequential processing, and parallel processing is processed by a GPU that specializes in parallel processing [7].

We are aiming for softwarization together with future higher-speed PON systems. Since DSPs are used in many studies on high-speed PON systems, we have been studying DSP softwarization. Figure 2 (c) shows our verification platform for DSP softwarization. This platform receives 5-Gbaud quadrature phase shift keying (QPSK) via an analog-to-digital converter (ADC) and outputs the demodulated 10-Gbps signal to a bit error rate tester (BERT) [8]. Another 5-Gbps output platform has verified real-time finite impulse response (FIR) filter with differential detection [9]. The challenge is that unwrap in carrier phase recovery employs sequential processing. We have removed this dependency by using decision-aided phase unwrapping [10]. Another study has already verified the support of multiple modulation formats, quadrature amplitude modulation (QAM) and pulse-amplitude modulation (PAM), using the flexibility of softwarization for application to data center interconnection [11].

While the technology of PON Abstraction is maturing, PHY softwarization still has several issues. Further study items include improvement in latency performance and port scalability, burst signal reception, and modularization for function replacement.

4. Conclusion

This paper summarized studies on PON abstraction and the full softwarization of PCS and DSP. Since these enable management via common API and replacement of various PHY specifications, they are indispensable for building future access networks that maximize the flexibility and agility of SDN/NFV.

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