

High Performance Avalanche Photodiode in a Monolithic Silicon Photonics Technology

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Abstract: We demonstrate a waveguide-integrated germanium-on-silicon avalanche photodiode in a monolithic silicon photonics technology, with TE responsivity of 26 A/W at 1310 nm wavelength at -5 V operating bias with a 3-dB bandwidth of > 30 GHz. © 2022 The Author(s)

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1. Introduction

Silicon photonics has gained tremendous popularity for data center interconnects applications in recent times. This technology offers a promising prospect for short-reach optical interconnect application due to several advantages such as low fabrication cost with high yield, germanium epitaxy process flow, and compatibility with the complementary metal-oxide-semiconductor (CMOS) process [1, 2]. The development of next generation transceivers operating at 800 Gb/s and 1.6 Tb/s requires improvement of link margins, either by increasing the reach of the link or by reducing the number of lasers and their associated cost and power consumption [3]. Silicon-Germanium (Ge/Si) Avalanche photodiodes (APD), with internal multiplication gain and high sensitivity, is a crucial device to realize this distance extension and to meet all link budget challenges [1–3], with lower cost compared to semiconductor optical amplifier scheme. Another high-volume potential application for Si/Ge APD is 50G PON utilizing NRZ formats, where only APD could meet the challenging link budget. 50G PON has the possibility of being adopted by many countries as a direct upgrade of current low speed 10G PON [4].

In this work, we report a monolithic waveguide-coupled Ge/Si APD with TE responsivity of 26 A/W at -5 V operating bias with a 3-dB bandwidth of 32.3 GHz. To the best of our knowledge, this is the world's first demonstration of an avalanche photodiode operating at ultra-low bias in a monolithic CMOS compatible silicon photonics technology that achieves a record responsivity bandwidth product of 839.8 [(A/W) · GHz].

2. Device Structure

The waveguide coupled Ge/Si APD demonstrated in this work was fabricated in a standard 12-inch wafer with monolithic integration of high quality active and passive silicon photonics devices with high f_T CMOS transistors by utilizing dual silicon thicknesses and dual contact modules [2, 5]. The device uses similar structure as [3], with an epitaxially grown Ge waveguide-based absorption region, lightly p-type doped charge region and intrinsic multiplication region with narrower width than that reported in [3]. The structure is incorporated in the same Si device layer reported in [2]. Fig. 1(a) shows a 3D perspective and a 2D cross-sectional schematic of the fabricated device. The charge region doping profile in the APD is optimized to maximize the avalanche gain of the device. The APD is coupled to a Si waveguide and a TE-optimized grating coupler with peak coupling at 1310 nm enabling wafer-scale measurement. Fig. 1(b) illustrates a 2D view of a Transmission Electron Microscopy (TEM) cross-section of the device highlighting the Ge epi region, the recessed silicon under the Ge region, the passivation layers above the Ge, and the buried oxide under the Si layer.

3. DC Characteristics

DC current-voltage (IV) measurement results at 1310 nm and room temperature are shown in Fig. 2(a). The anode bias was swept from +0.8 V to -7 V. The input power at the APD was varied from -35 dBm to -5 dBm. The dark current of the APD reaches 10.8 μ A at around -6 V bias. A grating coupler was utilized to couple the single-mode

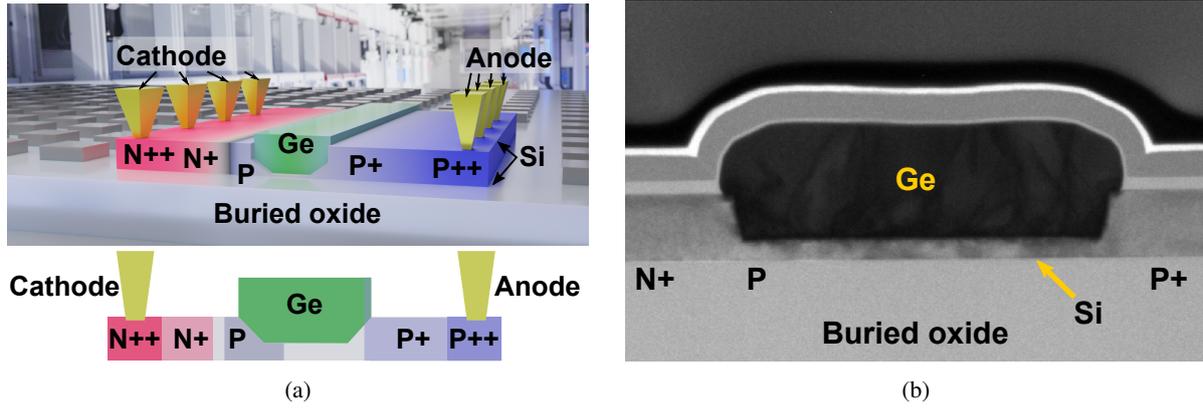


Fig. 1. (a) 3D perspective view and a cross section of the proposed APD, (b) TEM cross section of the Ge epi on Si.

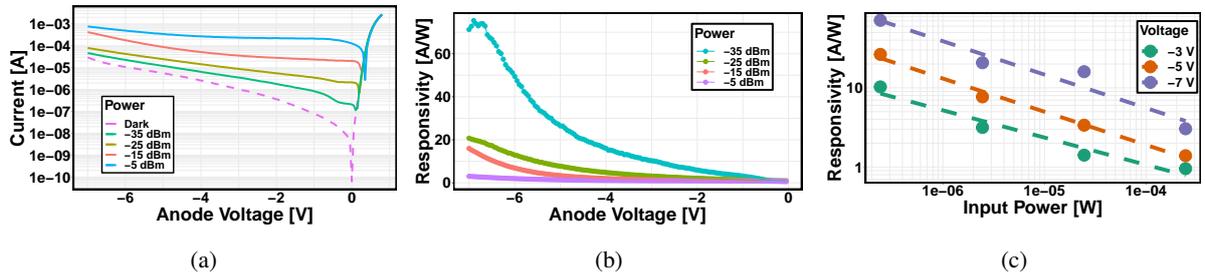


Fig. 2. DC characteristic of the APD: (a) total light response and dark current, (b) responsivity of the APD at room temperature for input optical power of -35, -25, -15 and -5 dBm, and (c) responsivity variation with respect to input optical power at three reverse bias voltage of -3, -5 and -7 V at 1310 nm.

TE light from a pigtail fiber to enable wafer-scale measurement as described in [6, 7]. Measured responsivity values for various biases are shown in Fig. 2(b). At 1310 nm the responsivity value at -6 V reverse bias is about 49 A/W and at -5 V it is about 26 A/W at -35 dBm input optical power. Due to the narrow charge and multiplication region in the device, a very high electric field is generated at lower bias voltages resulting in high responsivity and avalanche gain effect. Fig. 2(c) shows the responsivity variation to the input optical power of the APD for the bias voltages of -3, -5, and -7 V at 1310 nm. The reduction of responsivity with increasing optical power could be explained by the space charge screening effect as described in [8].

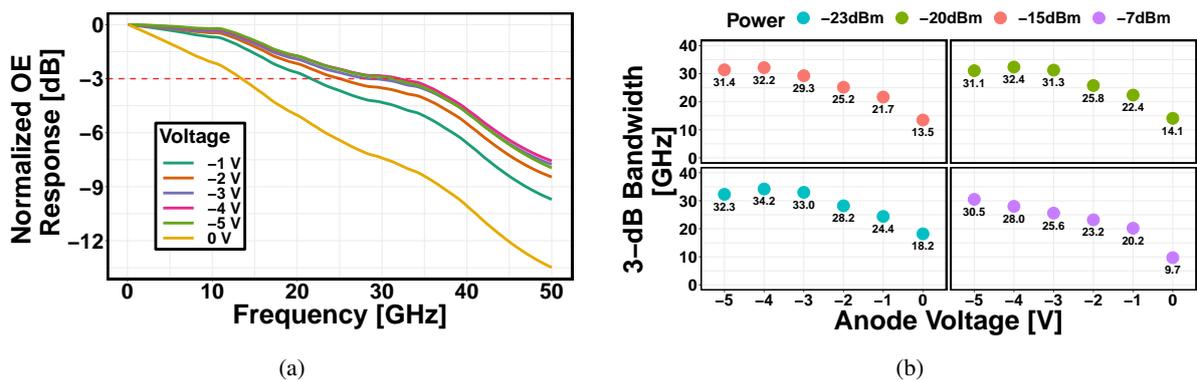


Fig. 3. (a) Opto-electric frequency response of the APD at -15 dBm optical input, (b) 3-dB cut-off frequency variation with respect to applied bias at various input optical power levels.

4. RF Characteristics

We performed APD RF measurements with GSG probes and a 50 GHz light-wave component analyzer (LCA). The measured normalized opto-electric frequency response curves are shown in Fig. 3(a) at -15 dBm input optical power and reverse bias voltage from 0 to -5 V at 1310 nm. The 0 V 3-dB bandwidth is about 13 GHz and increased up to 32 GHz at -4 V. Fig. 3(b) shows 3-dB opto-electric bandwidth at -23, -20, -15, and -7 dBm for reverse bias

Table 1. Comparison of recent APD in silicon photonics technology

Reference	Wavelength [nm]	Operation Voltage [V]	Dark Current [A]	Lowest Power [dBm] [†]	Responsivity [A/W]	Bandwidth [GHz]	Responsivity Bandwidth Product [(A/W) · GHz]
[9]	1550	5	1.00E-05	-11.4	7.2	18.9	136.08
[10]	1550	9	3.70E-05	-8	11.2	13	145.6
[4]	1310	18.3	6.60E-07	-23.2	5.5	32	176
[11]	1310	18	1.20E-07	-13	6	36	216
[12]	1550	31	2.70E-05	-28	54.5	6.24	340.08
[13]	1550	10	1.00E-05	-29.1**	26.4	25	660
[3]	1310	12	1.00E-04	-20	25	30	750
This work	1310	5	5.50E-06	-35**	26	32.3*	839.8

* measured at -23 dBm

** DC Measurement

[†] Eye diagram Measurement if not stated otherwise

voltage from 0V to -5V. The bandwidth characteristic is very similar at all measured input optical power levels below -7 dBm. The -7 dBm bandwidth reduction could be indicative of the space charge screening effect reducing the electric field inside the device [8].

5. Conclusion

High bandwidth and energy-efficient chip-to-chip optical interconnects are essential for large-scale data centers and high-performance computing infrastructure. Therefore, a high-sensitivity receiver is important to reduce the total link power consumption and relieve the link budget requirement. In this work, we demonstrated an ultra-low voltage APD operating at -5 V reverse bias with a responsivity of 26 A/W at -35 dBm, 3-dB opto-electric bandwidth of 32.3 GHz at -23 dBm at 1310 nm showing a record responsivity bandwidth product of 839.8 [(A/W) · GHz] compared to the recent published results shown in Table 1. The APD was fabricated in a state-of-the-art monolithic silicon photonics process that includes passive and active photonic components and high-performance CMOS field-effect transistors.

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